A Method for Automatically Finding Multiple Operating Points in Nonlinear Circuits

Leonid B. Goldgeisser, *Member, IEEE,* and Michael M. Green, *Member, IEEE*

***Abstract*—A new algorithm based on a SPICE-like simulator that searches for multiple operating points automatically, with no user intervention required, is presented. This algorithm, which exploits the asymmetrical properties of nonlinear mappings that describe multistable circuits, has been implemented into a program which automatically finds multiple (in most cases, all) operating points of a circuit. In addition to finding multiple operating points, this method offers another feature: it is capable of detecting the *stability* of a particular operating point. Another useful feature of this method is that it allows the user to gauge how close a particular circuit is to possessing multiple operating points. For circuits known to possess multiple operating points, this method allows the user to specify which operating point is encountered first. Unlike other continuation methods, circuit element models are not modified; only augmenting resistors are required. Hence, this approach lends itself well as an "add-on" to existing circuit simulators. A number of circuit examples are given.**

***Index Terms*—Circuit CAD, circuit simulation, circuit theory, multiple operating points (MOPs), nonlinear circuits, SPICE.**

I. Introduction

FINDING the dc operating points of a nonlinear circuit is one of the most important and difficult tasks in electrical circuit simulation. In the majority of circuit simulation programs the dc operating point is found (as in SPICE, for example) by using a Newton–Raphson-based iterative algorithm. Such algorithms have two shortcomings: First, convergence is in general not guaranteed unless the initial guess (specified by the user in SPICE by the `.nodeset` statement) is sufficiently close to the actual solution. Unfortunately the user either may not know the solution or cannot give a sufficiently accurate initial guess. Second, only one operating point can be found during a single analysis; neither location nor even existence of other operating points is known once the algorithm has converged to a particular operating point.

A better approach to finding a circuit's dc operating point (described by the solution of a set of nonlinear equations $F(x) = 0$, where $F : \mathcal{R}^n \rightarrow \mathcal{R}^n$ is smooth) is the use of a *continuation method*. In general, this method entails embedding a continuation parameter λ into a set of nonlinear equations $H(x, \lambda)$ where $H : \mathcal{R}^{n+1} \rightarrow \mathcal{R}^n, x \in \mathcal{R}^n$, and $\lambda \in [0, 1]$, which satisfies the following conditions.

1) $H(x, 1) = F(x)$.
2) The solution $x = a$ of $H(x, 0) = 0$, where $a \in \mathcal{R}^n$, is trivial or easily found.
3) There exists a continuous curve σ (called a "zero curve") in $\mathcal{R}^n \times [0, 1]$ such that $H(x, \lambda) = 0$ and the Jacobian matrix of H is full rank for every point on σ.

Since H gives a continuous deformation between the "easy" problem $H(x, 0) = 0$ and the "hard" problem $H(x, 1) = 0$, it is called a *homotopy*. In circuit simulation applications, $x \in \mathcal{R}^n$ is the vector of the circuit's node voltages, $F(x)$ gives the set of Kirchhoff's Current Law equations at each node[1], and the continuation parameter λ can be chosen to control a circuit component, such as a voltage source, a resistor, or a transistor parameter. The well-known "G-min stepping" and "source stepping" algorithms, found in many versions of SPICE, are simple examples of continuation methods.

A class of homotopies, known as "probability-one," has been found that can be applied to simulation of nonlinear circuits [2]. These homotopies have the following properties.

- The resulting zero curve does not exhibit a bifurcation for $\lambda \in [0, 1]$ (achieved by appropriate randomization of the equations).
- The zero curve remains bounded for $\lambda \in [0, 1]$ (achieved by ensuring that the "no-gain" property[2] holds for $\lambda \in [0, 1]$).
- The zero curve will not return to $\lambda = 0$ (achieved by arranging the operating point of the $\lambda = 0$ circuit to be unique).

Hence, in a probability-one homotopy the simulation is guaranteed to reach a solution at $\lambda = 1$. A number of implementations of such homotopies in existing circuit simulators have been reported [4]–[6].

An example of a zero curve (projected onto the V_k versus λ plane, where V_k is one of the circuit's node voltages) is shown in Fig. 1(a). The voltage at $\lambda = 0$ corresponds to the "easy" solution; the voltage at $\lambda = 1$ corresponds to the circuit's operating point. If a zero curve is tracked *beyond* $\lambda = 1$, it is possible for it to bend back and pass through $\lambda = 1$ more than once, as illustrated in Fig. 1(b). In this case, three operating points are found. This phenomenon is known as "λ-threading" and can be exploited to allow multiple operating points to be found in a

Manuscript received October 9, 2003; revised July 12, 2004. This paper was recommended by Associate Editor A. Ushida.

L. B. Goldgeisser is with the Synopsys Inc., Synopsys Technology Park, Hillsboro, OR 97124 USA (e-mail: leonidg@ieee.org).

M. M. Green is with the Department of Electrical Engineering and Computer Science, Universityof California, Irvine, CA 92697-2625 USA (e-mail: mgreen@uci.edu).

Digital Object Identifier 10.1109/TCSI.2005.844359

[1]Most versions of SPICE actually use the modified nodal analysis representation [1] which can accommodate floating voltage sources by including additional current variables.

[2]This property is similar to, but slightly stronger than, the well-known passivity property of all realistically modeled transistors [3].

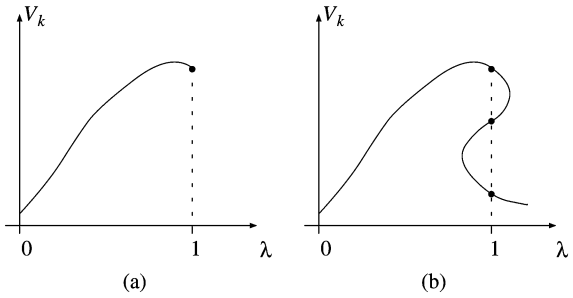

Fig. 1. (a) Example of zero curve projection; (b) example of λ-threading.

single simulation. This will be discussed extensively in the next section.

Over the years, there have been a number of algorithms proposed for finding multiple operating points of circuits [7]–[11]. However, all of these algorithms have the disadvantage of requiring piecewise-linear transistor models; moreover, little insight into the *qualitative* nature of these multiple operating points is given. Homotopy methods using standard continuous transistor models have also been reported. In [12] multiple operating points are found by using combinations of ideal diodes and current-controlled current sources. In [13] an algorithm based on the SPICE transient analysis is given where the user identifies feedback loops in order to search for multiple operating points. In [14] finding multiple operating points using a type of λ-threading is presented. In [15] a technique for finding multiple operating points by setting various initial points on a zero curve is presented.

In this paper, we discuss methods by which the likelihood of λ-threading can be increased, thereby increasing the chance of finding multiple operating points. We also discuss a fundamental relationship between the way operating points are encountered on a zero curve and the stability of these operating points.

II. Conditions for Lambda-Threading

A. No-Threading Property

Although λ-threading is a desirable characteristic, it is not guaranteed for all continuation methods. In this section we will derive sufficient conditions for λ-threading. Before doing this, we can gain some insight into this problem by first stating a simple condition under which λ-threading *cannot* occur:

No-Threading Property: Suppose a homotopy $H(x, \lambda)$ has the following properties.

1) The circuit being simulated is eventually passive for $\lambda \in [0, 2]$.
2) The solutions to $H(x, 0)$ and $H(x, 2)$ are unique.
3) $H(x, \lambda) = H(x, 2 - \lambda)$ (i.e., the homotopy is symmetric around $\lambda = 1$).

Then, λ-threading cannot occur.

Proof: We first note that, as proved in [16], any eventually passive circuit must possess an *odd* number of structurally stable operating points. Let us first suppose that the circuit being simulated possesses three structurally stable operating points A, B, and C. Then, assuming the homotopy has the global convergence conditions given above, the zero curve for $\lambda \in [0, 1]$ must consist of disjoint zero curves as shown in Fig. 2(a). One of these curves will connect $\lambda = 0$ to operating point A. The other curve cannot intersect $\lambda = 0$ (since the $\lambda = 0$ circuit has a unique solution) and therefore must connect operating points B and C.

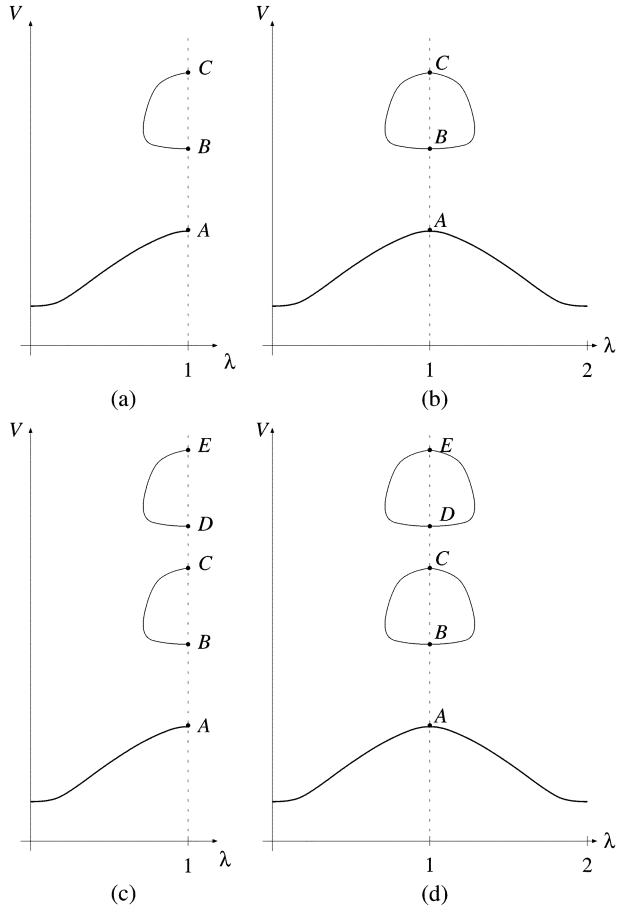

Fig. 2. Illustration of effect of symmetry on λ-threading.

If the homotopy is symmetric around $\lambda = 1$, then so must the zero curves, as illustrated in Fig. 2(b). Hence, the curve connecting operating points B and C must form a closed loop, which implies that, for $\lambda \in [0, 2]$, the curve that intersects operating point A cannot be connected to the other operating points, thereby preventing λ-threading from occurring. We can make the same statements in the case of circuits with higher numbers of operating points; the case for 5 operating points is illustrated in Fig. 2(c) and (d). □

Since we have shown that arranging the homotopy to be symmetric prevents the zero curve from threading, then we conjecture that making the homotopy *asymmetric* will allow the zero curve to thread. This idea will be explored shortly. However, we first need to make some statements regarding the relationship between operating point stability and order of operating points on a zero curve.

B. Zero Curve Bifurcations and Operating Point Stability

As mentioned in Section I, one of the requirements for global convergence is that the zero curve be free of bifurcations for $\lambda \in [0, 1]$. An example of a zero curve that contains a bifurcation

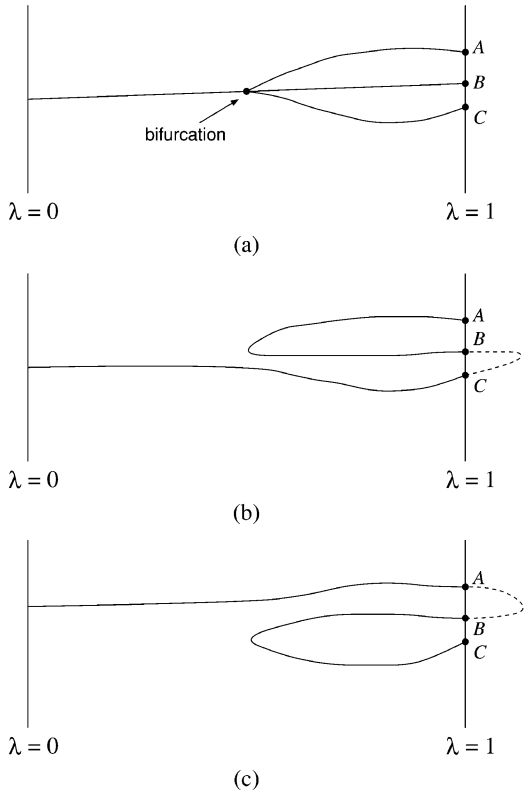

Fig. 3. (a) Zero curve with bifurcation. (b) Unfolded bifurcation after applying a small perturbation to the homotopy. (c) Unfolded bifurcation after applying a different small perturbation to the homotopy.

is shown in Fig. 3(a). Let us assume that this curve corresponds to a circuit that possesses three operating points A, B, and C. Furthermore, let us assume that operating point B is unstable of type $\mathcal{U}^o$. (This type of operating point instability is defined in [17]; any circuit that possesses three operating points must have exactly one $\mathcal{U}^o$ operating point.) It is proved in [18] that any small perturbation in the homotopy will cause an "unfolding" of the bifurcation, as illustrated in Fig. 3(b). In the continuation methods described in [2], voltage sources with random values are inserted into the circuit at $\lambda = 0$ to achieve this unfolding. We now assume that the unfolded zero curves shown in Fig. 3(b) connect as shown for $\lambda > 1$ so that λ-threading is achieved. It is proved in Lemma 2.1 of [19] that λ must *decrease* through a $\mathcal{U}^o$ operating point. Hence, the threading must occur in the order shown either in Fig. 3(b), or in Fig. 3(c). In both cases, operating point B is always the *second* operating point reached. In general, any operating point found after an *even* number of $\lambda = 1$ crossings is unstable (provided that the zero curve does pass through a bifurcation).

C. Criteria for Finding Multiple Operating Points

In an attempt to make a homotopy as asymmetric as possible in order to "encourage" λ-threading, we place the following conditions on a homotopy for $\lambda \in [0, 2]$.

1) The zero curve is bounded for $\lambda \in [0, 2]$.
2) There exists some $\eta_0 \in (0, 1)$ such that the circuit corresponding to any $\lambda \in [0, \eta_0]$ possesses a unique operating point.

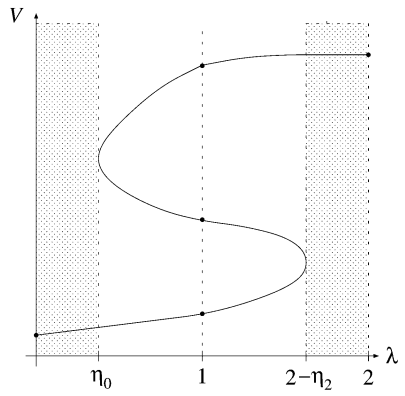

Fig. 4. Illustration of a zero curve passing through three operating points.

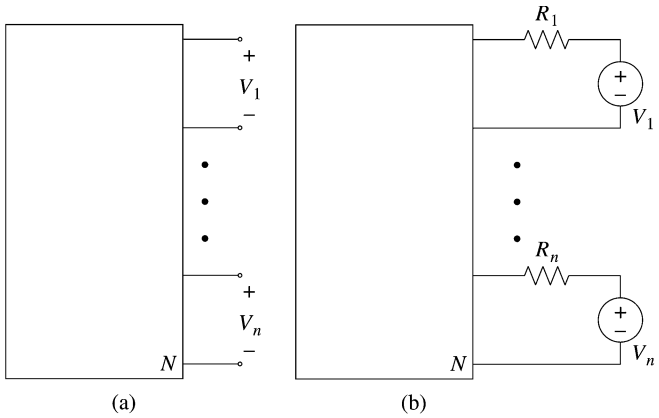

Fig. 5. Circuit illustrating a special type of homotopy.

3) The unique operating point of the circuit corresponding to $\lambda = 0$ is "close" to an operating point of the original (i.e., $\lambda = 1$) circuit.
4) There exists some $\eta_2 \in (0, 1)$ such that the circuit corresponding to any $\lambda \in [2 - \eta_2, 2]$ possesses a unique operating point.
5) The unique operating point of the circuit corresponding to $\lambda = 2$ is "close" to an operating point, different from the one in Condition 3, of the original circuit.

These properties are illustrated in Fig. 4. Condition 1 is easily realized by requiring that any circuit corresponding to $\lambda \in [0, 2]$ be passive. Conditions 2 and 4 are satisfied by requiring structurally stable operating points corresponding to $\lambda = 0$ and $\lambda = 2$. The shaded regions in Fig. 4 correspond to the homotopy's "regions of uniqueness." Under these conditions, the only possible zero curve that can exist must pass through $\lambda = 1$ at least three times as illustrated in Fig. 4. We will discuss "closeness" properties 3 and 5 in the next section.

III. New Homotopy

A. Closeness of Operating Points

To illustrate how two operating points can be close to each other (e.g., conditions 3 and 5 from Section II-C), we construct a simple homotopy as follows. Given a circuit with a specified stable operating point, suppose we measure a set of n port voltages $V_1, V_2, \ldots, V_n$ as illustrated in Fig. 5(a). We now consider the augmented circuit shown in Fig. 5(b) where each port

i is augmented with a series connection of a resistor R_i and a voltage source V_i, where V_i is the ith port voltage measured in the original Fig. 5(a) circuit. As discussed in [20], the port voltages will be constant for any $R_i \in [0, \infty]$. Let us consider a C^2 homotopy with the following properties.

1) $R_i = 0$ for $\lambda = 0$.
2) $R_i = \infty$ for $\lambda = 1$.

Note that $\lambda = 0$ corresponds to all ports connected directly to the voltage sources. Suppose that the circuit corresponding to $\lambda = 0$ has no feedback structures (as defined in [21]) and therefore must possess a unique operating point. For this homotopy, the resulting zero curve will exhibit nearly constant values of node voltages for all $\lambda \in [0, 1]$ and thus the arclength will be almost unity—the lowest possible value. We call this type of homotopy "arclength reducing." As long as this zero curve does not include a bifurcation, then a small perturbation in the homotopy (i.e., perturbations in voltage source values) will result in a small change to the zero curve.

It is cumbersome to insert a voltage source at each node; a more efficient approach would be to instead set the operating region of each transistor in the circuit. Moreover, it is also unrealistic to expect the node voltages to be available before the simulation has been run! A new homotopy described in the next section will dispense with both of these restrictions.

Unlike other homotopies previously reported, the implementation of the arclength reducing homotopy is based on simply augmenting the circuit being simulated with series combinations of resistors and voltage sources placed in appropriate locations. If the resistance of the augmenting resistor can assume both zero and infinite values then it allows us to model both short and open circuits, respectively. If we are simulating a circuit with transistors, it is convenient to augment the circuit corresponding to a set of expected transistor states. Using short and open circuits we can force selected transistors to be in certain states and thus control the overall circuit behavior. In order to work with transistor circuits we introduced the concept of a "pseudomodel." The augmenting resistor and the pseudomodel are two basic concepts upon which the arclength reducing homotopy is based. Those two concepts are briefly described in the next section. More detailed information can be found in [22], [23].

B. Pseudomodels

Using the augmenting resistors we can replace each transistor[3] in the circuit being simulated by one of the "pseudomodels" shown in Fig. 6. We have defined three general pseudomodels: low-current (corresponding to a transistor's cutoff state where all currents are near zero); low-voltage (corresponding to the saturation region for the bipolar junction transistor (BJT) or triode region for MOS); and high-impedance (corresponding to forward-active for BJT or saturation for MOS). In Fig. 6(a), these states are illustrated for bipolar and MOS transistors; extension to other types of transistors is straightforward. This replacement ensures that the operating point corresponding to $\lambda = 0$ is "close" to the chosen operating point of the circuit being simulated. For the high-impedance pseudomodel, the value of the augmenting voltage source is determined based on the transistor model and the expected value of current.

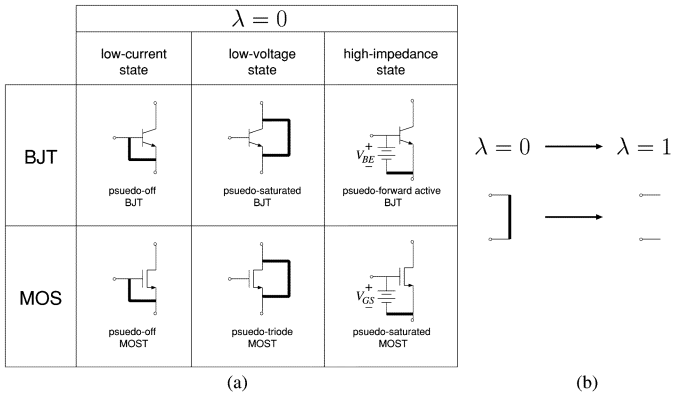

Fig. 6. (a) Augmented transistor pseudomodels corresponding to $\lambda = 0$. (b) Homotopy definition.

Notice that each of the pseudomodels is constructed simply by augmenting the transistor with either a short circuit or a voltage source. Moreover, since at $\lambda = 0$ every transistor is replaced by one of the pseudomodels[4], any feedback structure in the original circuit will be destroyed; hence, the circuit corresponding to $\lambda = 0$ must possess a unique operating point [21] which can easily be found using standard Newton–Raphson techniques. The homotopy itself is simply defined as shown in Fig. 6(b). Each augmenting short circuit at $\lambda = 0$ becomes an open circuit at $\lambda = 1$.

In order to realize a continuous deformation from a short circuit to an open circuit, a parametric representation of the augmenting resistors must be used. Assume the augmenting resistor has a voltage v across it and conducts a current i with the standard associated reference directions. Then, we can write

$$[a_i \cos\theta(\lambda)]i - [a_v \sin\theta(\lambda)]v = 0 \tag{1}$$

where a_i and a_v are positive constants and θ is a monotonically increasing function of λ such that $\theta(0) = \pi/2$ (corresponding to a short circuit) and $\theta(1) = 0$ (corresponding to an open circuit). We used the following function to realize this characteristic:

$$\theta(\lambda) = \frac{\pi}{2}\left[1 - \frac{1}{1 + (k(1-\lambda))^n} + \frac{(1-\lambda)^n}{1+k^n}\right], \qquad 0 \le \lambda \le 1. \tag{2}$$

Parameters n (a positive integer) and k (a positive real number) determine the location of the bend and the steepness of the nonlinear function θ. By adjusting n and k one can optimize the behavior of θ for a particular transistor model [23]. For the simulations presented in this paper, $k = 2.5$ and $n = 6$ were used.

We will refer to the homotopy defined above as $H_{\text{arh}}(x, \lambda)$ where x is the vector of nodal voltages as discussed in Section I. This homotopy is completely defined for $\lambda \in [0, 1]$ by the set of $\lambda = 0$ transistor states and (1) and (2).

One way to extend the arclength reducing homotopy for finding multiple operating points might be to specify the

[3]We exclude diode-connected transistors from this replacement since they are essentially two-terminal nonlinear resistors and thus cannot be one of the two transistors that defines a feedback structure.

[4]Loops of short circuits must be avoided, however.

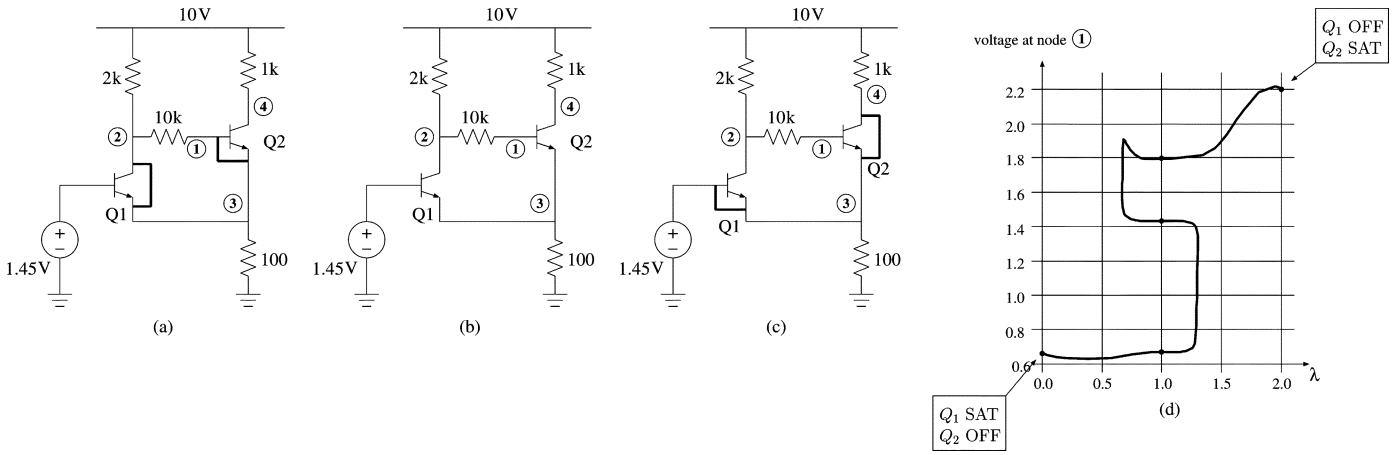

Fig. 7. (a) Schmitt trigger circuit corresponding to $\lambda = 0$. (b) Schmitt trigger circuit being simulated (corresponding to $\lambda = 1$. (c) Circuit corresponding to $\lambda = 2$. (d) Resulting zero curve.

transistor states corresponding to a *pair* of expected operating points. One of these operating points is used to construct the $\lambda = 0$ circuit; the other to construct the $\lambda = 2$ circuit. (In practice, it is of course unrealistic to expect the user to specify, *a priori*, two operating points. In the next section, we will show how to dispense with this requirement, leading to an algorithm that automatically searches for multiple operating points.)

On this basis, we construct a new homotopy $\hat{H}_{\rm arh}$ that is defined for $\lambda \in [0, 2]$ as follows:

$$\hat{H}_{\rm arh}(x,\lambda) = \begin{cases} H_{\rm arh}(x,\lambda), & \lambda \in [0,1] \\ H'_{\rm arh}(x, 2-\lambda), & \lambda \in [1,2] \end{cases} \tag{3}$$

where $H'_{\rm arh}(x,0)$ corresponds to a set of transistor states that may be different from those corresponding to $H_{\rm arh}(x,0)$. Thus, the homotopy $\hat{H}_{\rm arh}(x,\lambda)$ is completely defined for $\lambda \in [0,2]$ by two sets of transistor states, one corresponding to $\lambda = 0$ and the other corresponding to $\lambda = 2$, and (1) and (2).

As an example, consider the Schmitt trigger circuit shown in Fig. 7(b). The behavior of this circuit is well known. It possesses two stable operating points: One of these operating points corresponds to Q_1 biased in saturation and Q_2 biased in cutoff; the other operating point has the transistor operating regions reversed. It also possesses an unstable operating point corresponding to both transistors biased in the forward-active region.

A homotopy was constructed with the $\lambda = 0$ pseudomodels corresponding to the first stable operating point as shown in Fig. 7(a) and the $\lambda = 2$ pseudomodels corresponding to the second stable operating point as shown in Fig. 7(c). This simulation does obtain three operating points; the zero curve projection of the node **1** voltage is shown in Fig. 7(d).

C. Opposite States

We will now describe how a multiple operating point search algorithm can be implemented *without* requiring the user to specify appropriate transistor states *a priori*. In order to find appropriate transistor states to be assigned to $\lambda = 0$ and $\lambda = 2$, we arrange for the $\lambda = 0$ state to be constructed using a known operating point of the circuit. (This can be done by use of another homotopy or some other simulation method. Or, the $\lambda = 0$ circuit could be constructed by selecting expected transistor states based on the designer's knowledge of the circuit's operating point. Finally, the states can be selected randomly. Global convergence guarantees that an operating point will be found even though the arclength will be greater than unity.) After a simulation from $\lambda = 0$ to $\lambda = 1$ is run, the transistor states for the operating point obtained at $\lambda = 1$ are recorded; the threading homotopy is then constructed based on these transistor states. The $\lambda = 2$ state is constructed by setting the pseudomodel of each transistor to the "opposite" state to that set for $\lambda = 0$. The "opposite" state of a transistor is defined in Table I.

TABLE I
DEFINITION OF "OPPOSITE STATE" OF TRANSISTOR

$\lambda = 0$ **state**	$\lambda = 2$ **state**
low-voltage	low-current
low-current	low-voltage
high-impedance:	
$V_{CE} > V_{BE}$ or $V_{DS} > V_{GS}$	low-voltage
$V_{CE} < V_{BE}$ or $V_{DS} < V_{GS}$	low-current

D. Multiple Operating Point Search Algorithm

The multiple operating point search (MOPS) algorithm is based on the principle which is somewhat "opposite" to the *No-threading Property*. Based on an analysis of an operating point previously identified, the algorithm "assumes" that there is an operating point which is opposite (as defined above) to the original operating point, and constructs the homotopy from the known operating point (defined at $\lambda = 0$) to the predicted location of the opposite operating point (defined at $\lambda = 2$). As will be shown shortly, our experiments indicate that in the majority of simulations of circuits possessing multiple operating points, the predicted operating point (i.e., opposite of one already found) is indeed very close to the location of the existing operating point of a circuit. Based on this observation, the following algorithm has been constructed. We assume that one operating point has already been found.

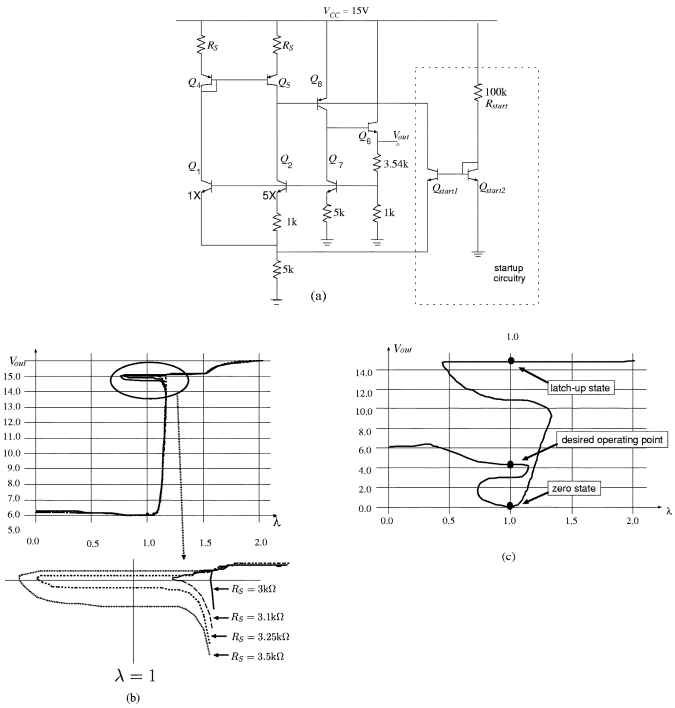

Fig. 8. Voltage regulator circuit and zero curves.

Multiple Operating Point Search Algorithm:

1) Construct the homotopy $\hat{H}_{\text{arh}}(x, \lambda)$ with $\lambda = 0$ corresponding to the transistor states in the operating point previously found and $\lambda = 2$ corresponding to the opposite of these transistor states.
2) Track the zero curve for this homotopy and note all operating points found (corresponding to crossings of $\lambda = 1$).
3) For each new operating point found, repeat steps 1 and 2 until no new operating points are found.

Choosing the $\lambda = 2$ transistor states opposite to the the corresponding $\lambda = 0$ transistor states attempts to utilize the homotopy's asymmetry around $\lambda = 1$, thereby maximizing the probability of λ-threading. In order to ensure that each zero curve does not contain a bifurcation, in implementation of this algorithm, some randomization must always be present in the homotopy. This is accomplished by introducing small random perturbations in (2).

IV. Circuit Examples

A. Brokaw Voltage Regulator

The voltage regulator circuit shown in Fig. 8(a) is commonly used to generate an output voltage that is highly insensitive to temperature [24]. Resistors R_S are placed in the circuit to improve the matching of the current mirror consisting of transistors Q_4 and Q_5. This circuit includes "start-up" circuitry (consisting of $Q_{\text{start1}}, Q_{\text{start2}}, R_{\text{start}}$) that prevents it from setting at its zero state. A simulation of this circuit was run for four different values of R_S, each incorporating the multiple operating point search algorithm described in the previous section. The zero curve projections V_{out} versus λ for each of the four simulations are shown in Fig. 8(b). All four zero curves are almost the same except for one area which is encircled and shown magnified in the bottom part of the graph. It can be seen from the plots that for $R_S \geq 3.25$ k the circuit possesses three operating points: the desired one, where V_{out} is near 5 V; one where V_{out} is close to V_{CC} (latch-up state); and a third, unstable operating point.

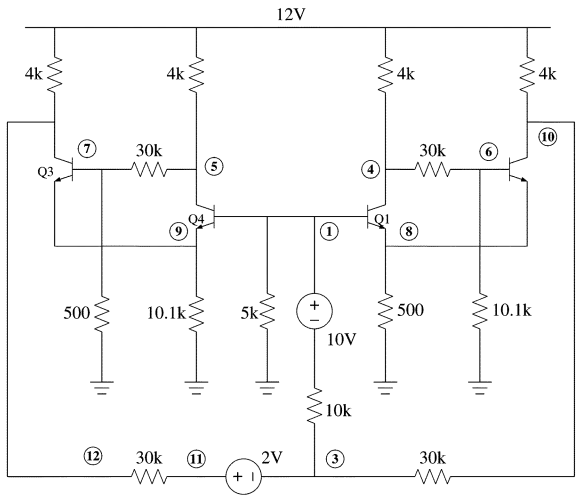

Fig. 9. Circuit with nine dc operating points.

Using the other two operating points found as starting points (as specified in the algorithm), additional simulations were run; however, no additional operating points were found.

This example illustrates another very important advantage of the continuation method presented here. By observing the *entire* zero curve, the designer can be made aware of not only the *number* of operating points the nominal circuit possesses, but also information is given regarding *how close* the circuit is to possessing additional dc operating points. For example, for the case where $R_S = 3.1$k it can be observed that even though the circuit does not have multiple operating points, it is very close to having them. Hence, this method allows the designer to gauge the *robustness* of a circuit's dc behavior.

Another simulation was run without the startup circuitry, consisting of $Q_{\text{start1}}, Q_{\text{start2}}$, and R_{start}, removed. Such a circuit is known to have a zero state where all transistors are off. The resulting zero curve (where R_S was set to 5 k), shown in Fig. 8(c) where five operating points (three stable) were found, clearly shows the presence of such a state.

B. A BJT Circuit With Nine Operating Points

The circuit shown in Fig. 9 has been shown to possess nine dc operating points [25]. We will apply the MOPS algorithm to find those operating points. To find the first operating point we will start from a randomized state. The result of the MOPS algorithm is shown in Table II.

The transistor states corresponding to all nine operating points are shown in Table III. As discussed earlier, all even-indexed operating points are unstable. In addition, operating point 9 is unstable of type $\mathcal{U}^e$, as defined in [17].

Some graphical simulation results are shown in Fig. 10. Two-dimensional (2-D) zero-curve projections of nodes 6 and 7 versus λ are shown in Fig. 10(a) and (b), respectively. A

TABLE II
MULTIPLE OPERATING SEARCH ALGORITHM PATH FOR BJT CIRCUIT WITH NINE OPERATING POINTS

Starting point $\lambda = 0$	Found Operating points	Ending point $\lambda = 2$
random	1	
1	1 2 3 4 5	$\overline{1}$
2	3 2 1	$\overline{2}$
3	3 2 1 6 7	$\overline{3}$
4	5 8 9 4 3 2 1	$\overline{4}$
5	5 4 3 2 1	$\overline{5}$
6	7 6 1 2 3	$\overline{6}$
7	7 6 1 2 3	$\overline{7}$
8	5 4 9 8 7 6 1	$\overline{8}$
9	1	$\overline{9}$

TABLE III
DC9: 9 OPERATING POINTS

OP	Stability	Q_1	Q_2	Q_3	Q_4
1	stable	saturation	cutoff	cutoff	saturation
2	unstable	saturation	cutoff	forward-active $Ic = 2.38$mA	forward-active $Ic = 0.41$mA
3	stable	saturation	cutoff	saturation	forward-active $Ic = 2.28$mA
4	unstable	forward-active $Ic = 0.71$mA	forward-active $Ic = 1.64$mA	saturation	forward-active $Ic = 6.43\mu$A
5	stable	cutoff	saturation	saturation	cutoff
6	unstable	forward-active $Ic = 0.41$mA	forward-active $Ic = 2.36$mA	cutoff	saturation
7	stable	forward-active $Ic = 0.29$mA	saturation	cutoff	saturation
8	unstable	forward-active $Ic = 20.99\mu$A	saturation	forward-active $Ic = 1.67$mA	FA $Ic = 0.70$A
9	unstable	forward-active $Ic = 0.59$mA	forward-active $Ic = 1.93$mA	forward-active $Ic = 1.93$mA	forward-active $Ic = 0.59$mA

TABLE IV
AB+C LOGIC CIRCUIT: TRUTH TABLE WITH ALLOWED LOGIC STATES

A	B	C	Y
L	L	L	L
L	L	H	H
L	H	H	H
H	L	H	H
H	H	L	H
H	H	H	H

three-dimensional (3-D) curve showing both voltages versus λ is shown in Fig. 10(c).

C. Combinational Logic Circuit With Feedback

The circuit shown in Fig. 11 consists of combinational logic with feedback through a set of AND gates connected to its inputs. The operating points of such a circuit include those corresponding to the states of $A_1 \ldots A_n$ for which $Y = 1$. We have simulated a CMOS realization of the circuit implementing the logic function $Y = AB + C$. The realization and the logic diagram of the circuit is shown in Fig. 12.

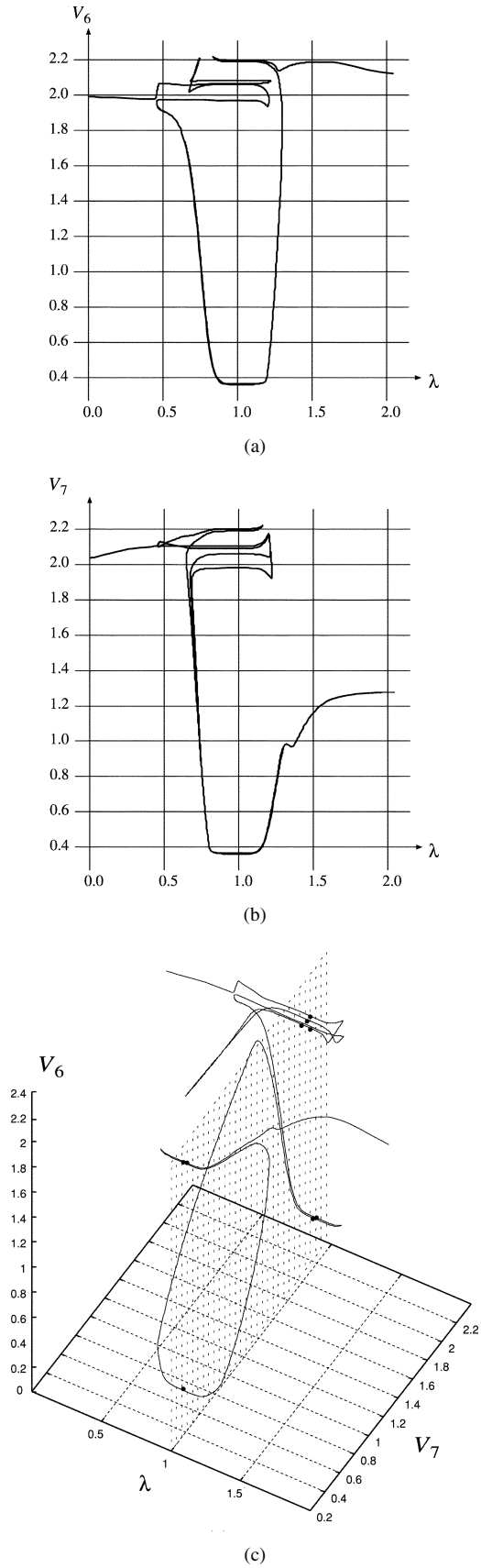

Fig. 10. (a) V_6 versus λ; (b) V_7 versus λ; (c) V_6 and V_7 versus λ.

We will first analyze this circuit by hand. From the logic diagram of the circuit shown in Fig. 12(a) we can construct the

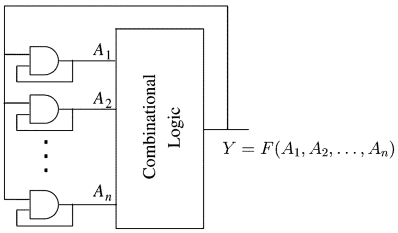

Fig. 11. Combinational logic with latch up inputs.

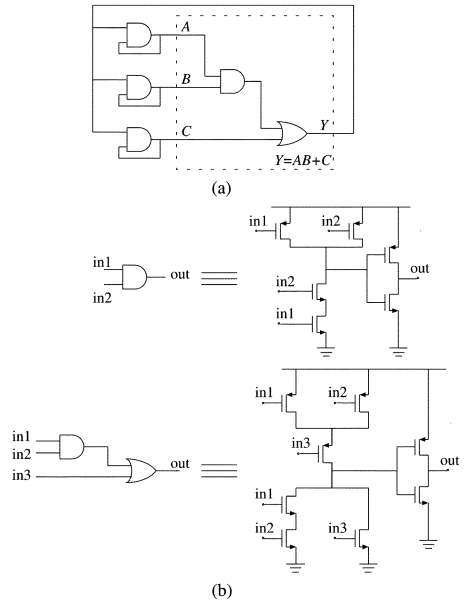

Fig. 12. Combinational logic. CMOS realization.

TABLE V
LISTING OF 23 OPERATING POINTS FOUND BY MOPS FOR FIG. 12 LOGIC CIRCUIT

	A	B	C	Y	Logic State?
1	0	10	10	10	Yes
2	0	5.1	10	10	
3	0	0	10	10	Yes
4	0	0	5.1	9.8	
5	0	0	0	0	Yes
6	0	5.1	5.1	9.9	
7	0	10	5.1	9.9	
8	5.1	0	10	10	
9	10	0	10	10	Yes
10	10	5.1	10	10	
11	5.1	5.1	10	10	
12	5.1	10	10	10	
13	10	10	10	10	Yes
14	10	0	5.1	9.9	
15	5.1	0	5.1	9.9	
16	10	5.1	5.1	10	
17	10	5.2	0	8.6	
18	6.4	6.4	0	6.4	
19	5.4	10	0	7.8	
20	10	10	0	10	Yes
21	10	10	5.1	10	
22	5.1	5.1	5.1	10	
23	5.1	10	5.1	10	

truth table shown in Table IV containing all valid logic states; all of these operating points can be shown to be stable.

The MOPS algorithm found 23 operating points for the circuit, all of which are listed in Table V. Included in all of these operating points are the six valid logic states listed in Table IV; these are indicated by a "Yes" in the last column of Table V.

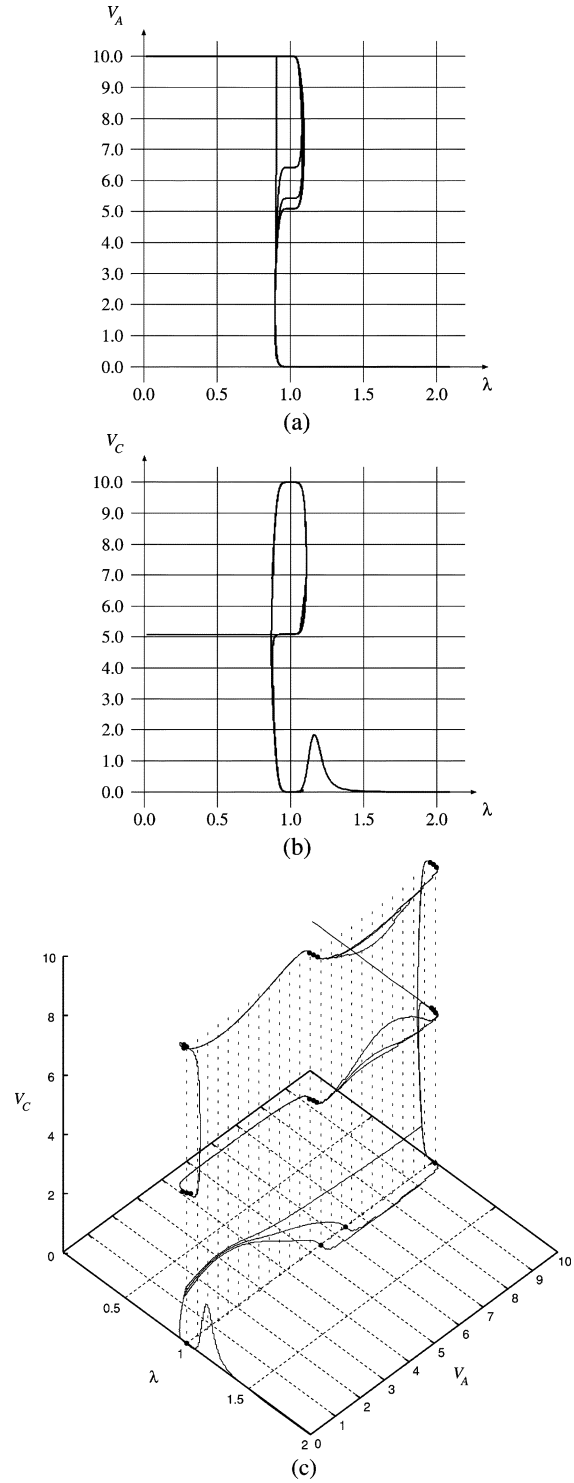

Fig. 13. (a) V_A versus λ; (b) V_C versus λ; (c) V_A, and V_C versus λ.

Some graphical simulation results are shown in Fig. 13. 2-D zero-curve projections of nodes A and C versus λ are shown in Fig. 13(a) and (b), respectively. A 3-D curve showing both voltages versus λ is shown in Fig. 13(c).

V. CONCLUSION

We have described how threading homotopy curves can be exploited to find more than one operating point of a circuit

during a single simulation. A method of constructing threading homotopies for circuits based on transistor states has also been described. It has been shown that multiple operating points can be found using this algorithm with no user intervention or *a priori* knowledge of locations of operating points.

REFERENCES

[1] C. W. Ho, A. E. Ruehli, and P. A. Brennan, "The modified nodal approach to network analysis," *IEEE Trans. Circuits Syst.*, vol. CAS-22, no. 6, pp. 504–509, Jun. 1975.

[2] R. C. Melville, L. Trajković, S.-C. Fang, and L. T. Watson, "Artificial parameter homotopy methods for the dc operating point problem," *IEEE Trans. Computer-Aided Design*, vol. 12, no. 6, pp. 861–877, Jun. 1993.

[3] A. N. Willson, "The no-gain property for networks containing three-terminal networks," *IEEE Trans. Circuits Syst.*, vol. CAS-22, no. 8, pp. 678–687, Aug. 1975.

[4] L. Trajkoviæ, E. Fung, and S. Sanders, "HomSPICE: Simulator with homotopy algorithms for finding dc and steady-state solutions of nonlinear circuits," in *Proc. Int. Symp. Circuits Systems*, May 1998, pp. 227–231.

[5] A. Dyes, E. Chan, H. Hofmann, W. Horia, and L. Trajković, "Simple implementations of homotopy algorithms for finding dc solutions of nonlinear circuits," in *Proc. Int. Symp. Circuits Systems*, May 1999, pp. 290–293.

[6] W. Ma, L. Trajković, and K. Mayaram, "HomSSPICE: A homotopy-based circuit simulator for periodic steady-state analysis of oscillators," in *Proc. Int. Symp. Circuits Systems*, May 2002, pp. 26–29.

[7] L. Chua and A.-C. Deng, "Canonical piecewise-linear analysis: Generalized breakpoint hopping algorithm," *Int. J. Circuit Theory Appl.*, vol. 14, no. 1, pp. 35–52, 1986.

[8] Q. Huang and R. Liu, "A simple method for all solutions of a piecewise linear network," in *Proc. Int. Symp. Circuits Systems*, Jun. 1988, pp. 1233–1236.

[9] H. Mizutani, "An effective method to find all solutions of piecewise-linear circuits by using partitioning," *Electron. Comm. Jpn.*, pt. 3, vol. 78, pp. 20–31, 1995.

[10] S. Pastore and A. Premoli, "Capturing all branches of any one-port characteristic in piecewise-linear resistive circuits," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 43, no. 1, pp. 26–33, Jan. 1996.

[11] K. Yamamura and M. Mishina, "An algorithm for finding all solutions of piecewise-linear resistive circuits," *Int. J. Circuit Theory Appl.*, vol. 24, pp. 223–231, 1996.

[12] M. Tadeusiewicz, "DC analysis of circuits with idealized diodes considering reverse bias breakdown phenomenon," *IEEE Trans. Circutis Sys. I, Fundam. Theory Appl.*, vol. 44, no. 4, pp. 312–326, Apr. 1997.

[13] A. Ushida, Y. Yamagami, Y. Nishio, I. Kinouchi, and Y. Inoue, "An efficient algorithm for finding multiple dc operating points based on SPICE oriented Newton homotopy method," *IEEE Trans. Computer-Aided Design* , vol. 21, no. 3, pp. 337–348, Mar. 2002.

[14] Y. Inoue, S. Kusanobu, and K. Yamamura, "A practical approach for the fixed-point homotopy method using a solution-tracing circuit," *IEICE Trans. Fund.*, vol. E85-A, no. 1, pp. 222–233, Jan. 2002.

[15] Y. Inoue, S. Kusanobu, K. Yamamura, and M. Ando, "An effective initial solution algorithm for globally convergent homotopy methods," in *Proc. Int. Symp. Circuits Systems*, May 2003, pp. 196–199.

[16] L. O. Chua and N. N. Wang, "On the application of degree theory to the analysis of resistive nonlinear networks," *Int. J. Circuit Theory Appl.*, vol. 5, pp. 35–68, 1977.

[17] M. M. Green and A. N. Willson Jr., "(Almost) half of all operating points are unstable," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 41, no. 3, pp. 286–293, Mar. 1994.

[18] L. Watson, S. Billups, and A. Morgan, "ALGORITHM 652 HOMPACK: A suite of codes for globally convergent homotopy algorithms," *ACM Trans. Math. Softw.*, vol. 13, pp. 281–310, 1987.

[19] R. Geoghegan, J. C. Lagarias, and R. C. Melville, "Threading homotopies and dc operatin points of nonlinear circuits," in *SIAM J.Optim.*, vol. 9, pp. 159–178.

[20] M. M. Green, "The augmentation principle of nonlinear circuits and its application to continuation methods," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 45, no. 9, pp. 1002–1006, Sep. 1998.

[21] R. O. Nielsen and A. N. Willson Jr., "A fundamental result concerning the topology of transistor circuits with multiple equilibria," *Proc. IEEE*, vol. 68, no. 2, pp. 196–208, Feb. 1980.

[22] M. M. Green and R. C. Melville, "Sufficient conditions for finding multiple operating points of dc circuits using continuation methods," in *Proc. IEEE Int. Symp. Circuits Systems*, May 1995, pp. 117–120.

[23] L. Goldgeisser, "Enhanced dc operating point simulation using probability-one continuation methods," Ph.D. dissertation, Department of Electrical and Computer Engineering, Univ. of California, Irvine, 1999.

[24] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993.

[25] A. Ushida and L. O. Chua, "Tracing solution curves of nonlinear equations with sharp turning points," *Int. J. Circuit Theory Appl.*, vol. 12, pp. 1–21, 1984.

Leonid B. Goldgeisser (S'97–M'98) received the Dipl.Eng. Degree in electrical engineering from Kazan State Technical University, Kazan, Russia, in 1990, the M.Sc. degree in electrical and computer engineering from the Technion, Israel Institute of Technology,Haifa, Israel, in 1994 and the Ph.D. degree in electrical and computer engineering from the University of California at Irvine in 1998.

In 1998, he joined Analogy Inc. While at Analogy, he worked on simulation algorithms, focusing on improving convergence of nonlinear solver and participated in the design and implementation of the next generation analog and mixed signal simulator. After spending 2001 and 2002 at Cadence Design Systems, Santa Clara, CA, working on VHDL-AMS simulator, he joined Synopsys Inc., Hillsboro, OR, where he works on development of multilingual mixed signal simulator. His research interests include nonlinear circuits and systems, mixed signal circuits design and simulation, hardware description languages and systems design.

Michael M. Green (S'89–M'91) received the B.S. degree in electrical engineering from the University of California at Berkeley, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles (UCLA), in 1984, 1988, and 1991, respectively.

He is currently Associate Chair in the Department of Electrical Engineering and Computer Science, University of California, Irvine, where he has been a Professor since 1997. From 1999 to 2001, he was an Integrated Circuit Designer with the Optical Transport Group at Broadcom Corp. (formerly Newport Communications), Irvine, CA. His current research interests include the design of analog and mixed-signal integrated circuits for use in high-speed broadband communication networks and nonlinear circuit theory. He has published over 50 papers in technical journals and has three patents.

Dr. Green was the recipient of the Outstanding Master's Degree Candidate Award in 1989 and the Outstanding Ph.D. Degree Candidate Award in 1991, both from the UCLA School of Engineering and Applied Science. He was also the recipient of the Sigma Xi Prize for Outstanding Graduate Science Student at UCLA in 1991, the 1994 Guillemin–Cauer Award of the IEEE Circuits and Systems Society, the 1994 W. R. G. Baker Award of the IEEE, a 1994 National Young Investigator Award from the National Science Foundation and the Award for New Technical Concepts in Electrical Engineering from IEEE Region 1. He has served as Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS, and IEEE TRANSACTIONS ON EDUCATION.