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A Method for Fabricating a Superior Oxide/Nitride/Oxide Gate Stack

T. C. Chang,[a,d,*,z] S. T. Yan,[b] P. T. Liu,[c] M. C. Wang,[e] and S. M. Sze[b,c]

[a]*Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan*
[b]*Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan*
[c]*National Nano Device Laboratory, Hsin-Chu 300, Taiwan*
[d]*Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Gushan Chiu, Kaohsiung, Taiwan 804*
[e]*Department of Materials Science and Engineering, National Tsing Hua University, Hsin-Chu, Taiwan*

A superior oxide/nitride/oxide (ONO) gate stack was demonstrated. High density plasma chemical vapor deposition was used to deposit the silicon nitride layer instead of the conventional low-pressure chemical vapor deposition for silicon/oxide/nitride/oxide/silicon technology. The densified nitride layer was performed by high-temperature dry oxidation to form a thermally grown blocking oxide layer on the silicon nitride rather than a deposited oxide layer. The ONO gate stack shows large memory window, high breakdown voltage, and reliable endurance characteristics, which is a potential candidate for future nonvolatile memory technology.
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To date, mass-produced nonvolatile memory devices are based on the concept of a continuous layer of floating gate.[1] However, these devices have faced the difficulties of consecutive scaling down by the compromise between long-term nonvolatility and high operating speed.[2] Recently, the concept of distributed storage of charge by a nitride layer[3] has caught much attention. Due to the intrinsic better endurance, the absence of erratic bits, and relatively higher radiation tolerance, the silicon/oxide/nitride/oxide/silicon (SONOS) structure has emerged as the most mature nonvolatile semiconductor memory (NVSM) currently in use for space applications.[4] The SONOS structure has a great potential of scaling the thickness of the tunnel oxide down to 1.6 nm and reducing the programming voltage below 5 V.[5] Therefore, the dielectric properties of the blocking oxide, charge-trapping nitride, and tunnel oxide (ONO) gate stack are concerned. Generally, the nitride layer of the SONOS structure is fabricated by low-pressure chemical vapor deposition (LPCVD) and, afterward, the blocking oxide is deposited on the nitride layer also by LPCVD followed by steam densification at 900°C.[6,7] In this study, high density plasma (HDP)CVD is used to deposit a trap-rich silicon nitride layer, followed by high-temperature dry oxidation to form a thermally grown oxide layer on the HDP nitride layer as a blocking oxide. This method provides a superior ONO gate stack with larger memory window and higher breakdown field compared with the conventional ONO gate stack for SONOS application.

First, a 2 nm thick thermal oxide was grown at 925°C on p-type Si(100) substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide. Subsequently, a 6 nm silicon nitride layer was deposited by HDPCVD on the tunnel oxide as a charge-trapping layer, followed by a dry oxidation at 982°C for 30 min to form a blocking oxide layer, estimated to be about 4 nm, on the nitride layer. The deposition of the HDPCVD silicon nitride was kept at 350°C in a low pressure of 3 mTorr with the ratio of $SiH_4:NH_3 = 12: 24$ sccm and an inductively coupled plasma (ICP) power of 900 W. The low pressure of 3 mTorr during deposition makes the path length an electron travels without undergoing a collision with a gas atom (or mean free path) increased, which will improve the uniformity of the thin film.[8] Differing from the prevailing SONOS technology, the blocking oxide in this study was thermally grown on the nitride layer instead of depositing on that. The oxidation was performed in APCVD at 925°C. Before and after the fabrication of the HDP nitride and blocking oxide, Fourier transfer infrared spectroscopy (FTIR) was used to investigate the quality of the HDP nitride and blocking oxide stack. After the aluminum gate electrode was patterned and sintered, the electrical measurements were performed by an HP 4156 and Keithley capacitance-voltage (C-V) analyzer to examine the electrical characteristics and reliability of the ONO gate stack.

Figure 1 exhibits the FTIR spectrum of the HDP nitride and blocking oxide stack before Al gate deposition. The absorption of sharp Si—O bonds ($\sim$1075 and 1255 cm^{-1}) and Si—N bonds ($\sim$820 to 900 cm^{-1}) are clearly observed. Also, the absorption of Si—O bonds at 1255 cm^{-1} indicates the formation of a high quality film.[9,10] To study memory effects of the ONO sandwiched structure, a bidirectional voltage sweeping between 5 and (-5) V was performed.

Figure 2 shows the C-V hysteresis after forward (from inversion to accumulation region) and reverse voltage sweeping (from accumulation to inversion region). When the sample is operated in positive polarity, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the nitride layer. When the device is negatively operated, the electrons may tunnel back to the Si substrate. The different threshold voltages can be defined as "1" or "0" for a memory device. The blocking oxide is used to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. In Fig. 2, hysteresis is also found in a counterclockwise direction, which implies the substrate injection of carriers rather than gate injection.[11] In our previous results, the trap-rich HDPCVD nitride contributes a larger threshold voltage shift, ΔV_t, (memory window) than the conventional LPCVD nitride.[12] Under the low-voltage operation of 5 V, ΔV_t is estimated to be around 1.3 V which is sufficient to be defined as "1" or "0" for a memory device.

Figure 3 shows the current-voltage (I-V) characteristics of the ONO gate stack. From the viewpoint of low-voltage operation, the leakage current at 5 V is low under both positive bias (write) and negative bias (erase). The breakdown voltage of the ONO gate stack is about 12 V under negative bias. Dramatically, the ONO stack is operated under positive bias without breakdown up to 80 V. This feature shows a superior dielectric property for the ONO gate stack. The HDPCVD silicon nitride is produced in a high-density-plasma chamber with a 900 W ICP power. The radio-frequency (rf) ICP power is used to increase the spiral motion of the charged particle. A charged particle will gain more energy the more times it moves around the spiral and a high density plasma is, hence, produced. During the deposition of the nitride layer, the simultaneously slight etching due to the bombardment of the high-density plasma is processed, which forms a more densified silicon nitride layer than

* Electrochemical Society Active Member.
[z] E-mail: tcchang@mail.phys.nsysu.edu.tw

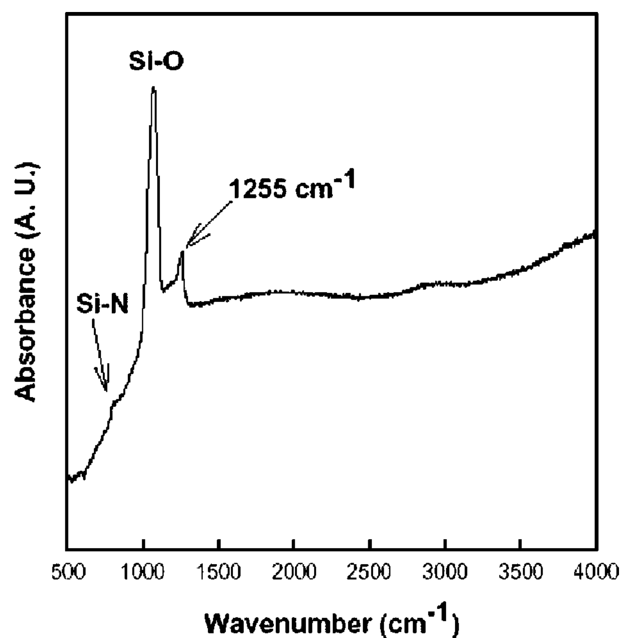

Figure 1. FTIR spectrum of the surface oxide layer and HDP nitride layer stack with the background spectrum of Si wafer and tunnel oxide deposited.

LPCVD nitride.[8,13] After the densified nitride layer is thermally oxidized, the thermally grown oxide/HDP nitride stack possesses a higher breakdown voltage than other deposited oxide/nitride stacks. The asymmetry of the leakage current at low electric field is currently under investigation.

In addition, the reliability of the memory device was also investigated. As shown in Fig. 4, the endurance of the memory device retains an obvious memory window of 0.91 V after 10^6 5/(−5) V write/erase cycles. The inset exhibits the C-V hysteresis after 10^6 write/erase cycles. A typical sense amplifier can easily detect the threshold voltage shift of 0.91 V to define the "1" or "0" for a logic memory device.

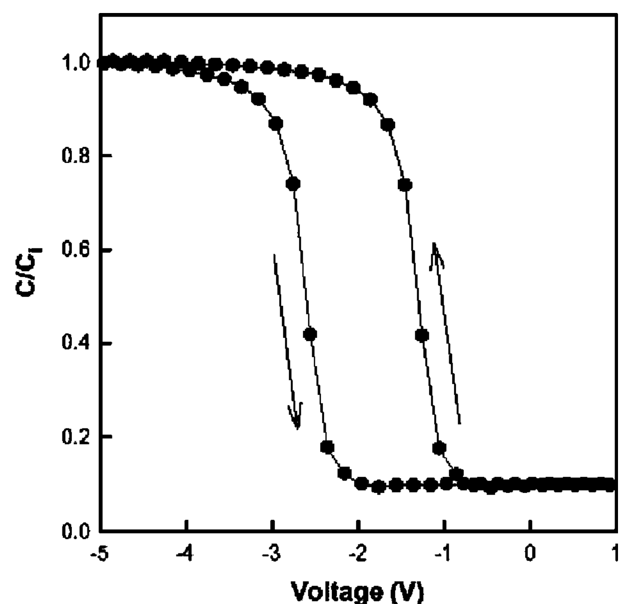

Figure 2. C-V hysteresis after forward (from inversion to accumulation region) and reverse voltage sweeping (from accumulation to inversion region).

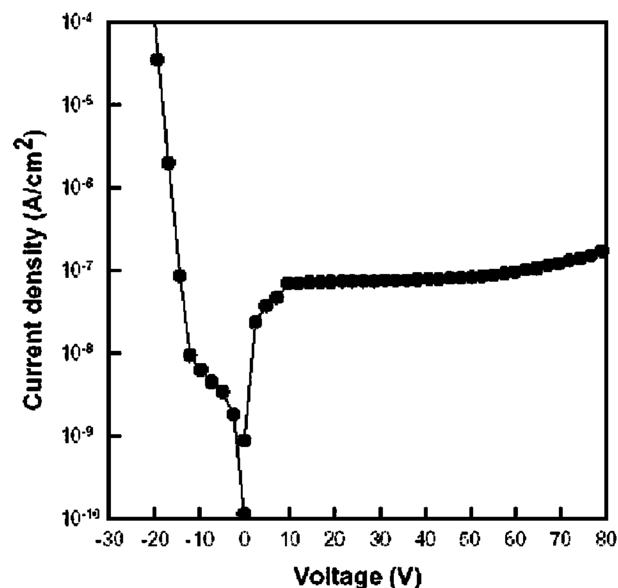

Figure 3. Current-voltage characteristics of the ONO gate stack.

In summary, a superior ONO gate stack with a large memory window and high breakdown voltage was demonstrated. HDPCVD silicon nitride was deposited on the tunnel oxide followed by a high temperature dry oxidation to form a blocking oxide layer on the nitride layer. This ONO stack with densified nitride layer and thermally grown oxide layer on the silicon nitride exhibited a reliable and viable approach for SONOS nonvolatile memory technology.

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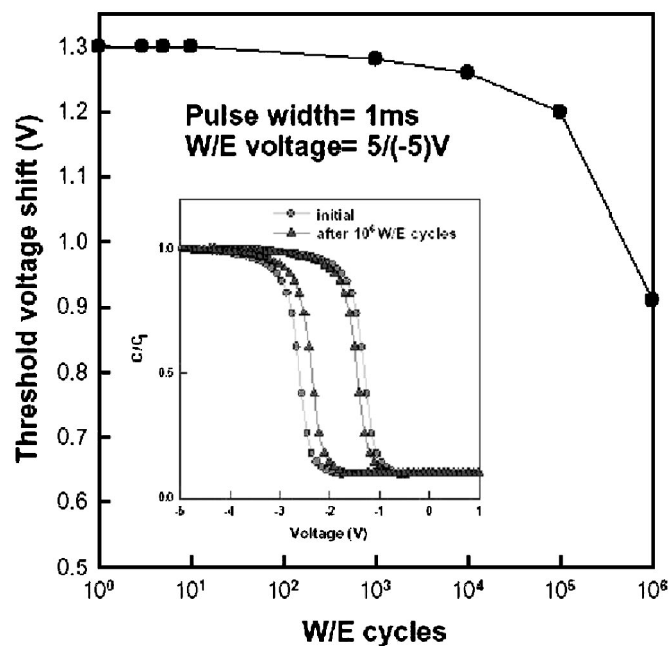

Figure 4. The endurance characteristics of the memory device retains an obvious memory window of 0.91 V after 10^6 5/(−5) V write/erase cycles. The inset exhibits the C-V hysteresis after 10^6 write/erase cycles.

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