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A Method for Parametric and Catastrophic Fault Diagnosis of Analog Linear Circuits

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ABSTRACT A universal method for single parametric and catastrophic fault diagnosis of analog linear circuits is presented in this paper. The methodology is based on fundamental laws governing linear circuits and methods of their analysis. The method involves creating models of the faulty elements, both passive and active, including current and voltage sources and applying an appropriately modified node method. This enables the creation of simple formulas to define the parameters of the faulty elements. Some measurement data must be collected during the course of the diagnostic test performed in the frequency domain and certain computation results obtained in the before-test-process. The method achieves all of the objectives of fault diagnosis: detection, location, and estimation of the faulty value. In 88.48%, the method correctly identifies the fault and estimates its value, but in 6.47%, the actual fault is accompanied by a virtual fault. The method is adapted to real conditions to improve the practical relevance and can be directly extended to double fault diagnosis. Six numerical examples are presented to illustrate the method.

INDEX TERMS Active circuits, analog circuits, circuit faults, circuit testing, computer aided engineering, electronic circuits, fault detection, fault diagnosis, fault location, linear circuits.

I. INTRODUCTION

Methods for fault diagnosis of analog circuits have been intensively studied over the last decades. Reliable fault diagnosis is required to improve the design and quality of electronic devices. Although digital content dominates in applications, electronics have a lot of analog content. Linear analog circuits such as active filters, instrumentation amplifiers, microphone preamplifiers, and others are commonly used in industrial systems. Despite the great effort made in this area, the results are not fully satisfactory in real circumstances and the problem remains open. Consequently, many analog circuits are tested functionally in practice. A great variety of methods related to different aspects of fault diagnosis have been developed over the years. Many of them are discussed in [1]–[4]. Numerous works in this field are focused on the problem of single fault diagnosis [5]–[7], because this is the most frequent case [8]. The diagnostic methods and techniques are based on circuit theory and signal processing methods [9]–[11], various branches of mathematics [7], [12]–[15], and Artificial Intelligence (AI) concepts [16]–[22].

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Faults that occur in analog circuits can be divided into parametric and catastrophic. Different approaches have been proposed for parametric fault diagnosis [9], [16], [17], [23], [24]. Short and open in circuit connectivity are classified as catastrophic faults. In extreme cases that occur in electronic circuits, they are called hard faults. The terms soft short and soft open are used if the short or open is not complete. Some problems associated with catastrophic fault diagnosis are discussed in [10], [18], [25], [26]. Usually, parametric and catastrophic faults are tested using different techniques. The former uses the simulation after test approach whereas the latter often uses the simulation before test approach.

This paper focuses on the fault diagnosis of linear analog electronic circuits. The goal of this study is to develop a reliable, fast, and accurate method for the diagnosis of both parametric and catastrophic faults. The proposed method is based on the following idea. The deviations of the parameters of the passive and active faulty elements are represented by the extra current and voltage sources introduced into the circuit. The deviations influence these extra sources and node voltages. Using the appropriately modified node method in the frequency domain it is proved that the sources and the node voltages are related by linear equations whose coefficients can be determined by analyzing the nominal circuit in

the before test stage. This property allows the source to be found if the value of the corresponding node voltage is given by the measurement test. With these sources, the voltages of the other nodes required to determine the faulty parameter can be easily determined. The results still require validation using other test point voltage. The outlined approach is very fast and allows the method to be generalized to multiple fault diagnosis.

Methods developed using AI-based techniques have dominated the fault diagnosis of analog circuits in recent decades. These methods use different computation and optimization techniques such as Artificial Neural Networks (ANN) [2]–[4], [19], Support Vector Machine (SVM) [16]–[18], Fuzzy Logic Method (FLM) [4], Evolutionary Computation (EC) [19], Genetic Algorithm (GA) [20], and Particle Swarm Optimization (PSO) [4], [16]. Diagnostic methods based on AI allow a wide range of parameter tolerances and have high efficiency in assigning faults to the predefined classes. The classes are determined by how much the parameter deviates from the nominal value by assumed specific values, e.g., ±10%, ±30%, ±50%, or 1 Ω resistance for short circuit, and 100 MΩ resistance for open circuit. The classes are learned and tested on this set. However, the process of creating the classifier required by many AI methods (e.g., [16]–[19]) requires different signal processing tools, statistical and heuristic methods and is time consuming. The process is carried out on a previously selected small set of tested elements with assumed values of the faulty parameter and the remaining parameters scattered randomly in their tolerance ranges. The methods indicate the correct class as long as the fault has a value close to that assumed in the classifier development stage. If the fault has a value significantly different from that in the training set, the result may be incorrect. A large number of classes lengthens the feature selection and learning processes. AI methods usually deal with a single fault, and it is difficult to generalize them to multiple faults.

The proposed method avoids some disadvantages of the methods developed with AI. The method manages continuous parameter faults and achieves all of the objectives of fault diagnosis. The method allows a wide spectrum of faults, both parametric and catastrophic, to be tested and is fast, easy to implement, and does not require large computing power. The accuracy of measurements taken in the course of the diagnostic test are taken into account. The simulation after test approach is used by the proposed method. Only simple circuit analyses are performed in the before test process. The proposed method can be generalized to a double-fault diagnosis.

The main contribution of this work can be summarized in the following points.

- Development of a method for single fault diagnosis of a broad class of analog linear circuits, including both parametric and catastrophic faults.

- Addressing real-world conditions and achieving all the fault diagnosis objectives.

- Implement the method as fully automated and demonstrate, using circuits containing voltage amplifiers, operational amplifiers, and operational transconductance amplifiers, that it is reliable, fast, and accurate.

The remainder of this paper is organized as follows. The basic equations are derived in Section II. Modeling the parametric faults is discussed in Section III. Section IV presents the methodology of the proposed approach, whereas the detailed description of the method is given in Section V. Section VI provides three examples of parametric fault diagnoses. Diagnosis of short and open faults is described in Section VII. A discussion is presented in Section VIII. Finally, Section IX concludes the paper.

II. PRELIMINARIES

We consider linear analog circuits consisting of passive and active devices [27], [28]. The active Integrated Circuit (IC) devices are characterized by linear macro models that are built using resistors, capacitors, inductors, and controlled sources. This is much easier than specifying the individual elements such as resistors and transistors. In these circuits, we consider permanent parametric and catastrophic faults that appear during either the fabrication process or the operational life of the circuit.

The primary faults of resistors are open, parameter changes, or short. The source of the resistor faults is generally due to external environmental factors. The primary fault of capacitors is parameter change or shorting due to aging of the dielectric or its breakdown. Parametric faults of inductors can be caused by short circuits of some turns due to damage of the insulation coating or changing magnetic properties.

The faults of the macro model parameters of the active device (IC), for example, the voltage transfer ratio of a voltage amplifier, reflect some defects that occur inside the device at the transistor level, which can be divided into parametric and spot defects. Parametric faults of IC components are mainly due to fabrication or aging. Examples of variations in ICs include geometrical deformations, such as variations in the channel length and width, oxide thickness, threshold voltage, etc [29]. Spot defects are produced by splotches of extra or missing material during production and can produce short or open faults [29]. We consider the situations, in which the occurring faults do not introduce nonlinear distortion, and the structure of the device macro model remains correct, but its parameters deviate from the nominal values. Consequently, the signals of the normal and fault states of the device are sinusoidal. Thus, we consider faults of IC device in terms of the faults of its macro model parameters. The proposed diagnostic method provides the values of these parameters, which play an important role in the circuit functionality.

Let us consider a linear circuit in the AC state driven by current sources, consisting of passive elements represented by their admittances, Voltage Controlled Current Sources (VCCSs) described by equations in the form $I = \hat{\lambda} V_x$, and Voltage Controlled Voltage Sources (VCVSs) with the description $V = \hat{\gamma} V_z$. The sets of passive elements,

VCCSs, and VCVSs will be denoted by Θ, Λ, and Γ, respectively. Let the number of the nodes in the circuit, except the datum node, be N and the number of VCVSs be M. The circuit with parameters that have nominal values is described using the modified node method leading to the matrix equation

$$\begin{bmatrix} \boldsymbol{Y} & \boldsymbol{A} \\ \boldsymbol{B} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \hat{\boldsymbol{e}} \\ \hat{\boldsymbol{i}} \end{bmatrix} = \begin{bmatrix} \hat{\boldsymbol{j}} \\ \boldsymbol{0} \end{bmatrix} \tag{1}$$

where $\hat{\boldsymbol{e}} = \left[\hat{E}_1 \cdots \hat{E}_N\right]^{\mathrm{T}}$ is an $N \times 1$ vector consisting of the node voltage phasors, $\hat{\boldsymbol{i}} = \left[\hat{I}_1^{\Gamma} \cdots \hat{I}_M^{\Gamma}\right]^{\mathrm{T}}$ is an $M \times 1$ vector consisting of the phasors of the currents flowing through the VCVSs, $\hat{\boldsymbol{j}} = \left[\hat{I}_1 \cdots \hat{I}_N\right]^{\mathrm{T}}$ is an $N \times 1$ vector of the phasors of the node current sources, and T denotes the transpose. $\boldsymbol{Y}$ is an $N \times N$ node matrix, $\boldsymbol{A}$ is an $N \times M$ matrix whose elements are $-1, 0, 1$, $\boldsymbol{B}$ denotes an $M \times N$ matrix whose rows correspond to the VCVSs. This matrix is created as follows. For m-th VCVS, described by the equation $V_m = \hat{\gamma} V_z$, connected to the nodes k_m and l_m and controlled by the voltage V_z between nodes z_1 and z_2, m-th row of $\boldsymbol{B}$ has the form $[0 \cdots 0 \overset{k_m}{1} 0 \cdots 0 \overset{l_m}{-1} 0 \cdots 0 \overset{z_1}{-\hat{\gamma}} 0 \cdots 0 \overset{z_2}{\hat{\gamma}} 0 \cdots 0]$.

Equation (1) can be written as

$$\boldsymbol{C} \begin{bmatrix} \hat{\boldsymbol{e}} \\ \hat{\boldsymbol{i}} \end{bmatrix} = \begin{bmatrix} \hat{\boldsymbol{j}} \\ \boldsymbol{0} \end{bmatrix} \tag{2}$$

where $\boldsymbol{C} = \begin{bmatrix} \boldsymbol{Y} & \boldsymbol{A} \\ \boldsymbol{B} & \boldsymbol{0} \end{bmatrix}$ and its inversion $\boldsymbol{C}^{-1}$ is denoted by $\boldsymbol{D} = \left[d_{ij}\right] i, j = 1, \ldots, N + M$.

Let us apply a current source ΔI to a pair of nodes k and l. In such a disturbed circuit, the matrix $\boldsymbol{C}$ remains intact, but the vector of the node current sources becomes $\hat{\boldsymbol{j}} + \boldsymbol{j}_0$ where

$$\boldsymbol{j}_0 = \left[0 \cdots 0 \quad \overset{k}{-\Delta I} 0 \cdots 0 \quad \overset{l}{\Delta I} 0 \cdots 0\right]^{\mathrm{T}}. \tag{3}$$

Consequently, we write

$$\boldsymbol{C} \begin{bmatrix} \boldsymbol{e} \\ \boldsymbol{i} \end{bmatrix} = \begin{bmatrix} \hat{\boldsymbol{j}} \\ \boldsymbol{0} \end{bmatrix} + \begin{bmatrix} \boldsymbol{j}_0 \\ \boldsymbol{0} \end{bmatrix} \tag{4}$$

where $\boldsymbol{e} = [E_1 \cdots E_N]^{\mathrm{T}}$ and $\boldsymbol{i} = \left[I_1^{\Gamma} \cdots I_M^{\Gamma}\right]^{\mathrm{T}}$ are $N \times 1$ and $M \times 1$ vectors whose elements are the phasors of the node voltages and the currents flowing through VCVSs, respectively, in the disturbed circuit. We convert (4) into

$$\begin{bmatrix} \boldsymbol{e} \\ \boldsymbol{i} \end{bmatrix} = \boldsymbol{D} \begin{bmatrix} \hat{\boldsymbol{j}} \\ \boldsymbol{0} \end{bmatrix} + \boldsymbol{D} \begin{bmatrix} \boldsymbol{j}_0 \\ \boldsymbol{0} \end{bmatrix} \tag{5}$$

where according to (2) and (3)

$$\boldsymbol{D} \begin{bmatrix} \hat{\boldsymbol{j}} \\ \boldsymbol{0} \end{bmatrix} = \begin{bmatrix} \hat{\boldsymbol{e}} \\ \hat{\boldsymbol{i}} \end{bmatrix} \tag{6}$$

and

$$\boldsymbol{D} \begin{bmatrix} \boldsymbol{j}_0 \\ \boldsymbol{0} \end{bmatrix} = \begin{bmatrix} d_{1l} - d_{1k} \\ \vdots \\ d_{N+M,l} - d_{N+M,k} \end{bmatrix} \Delta I. \tag{7}$$

Substituting (6) and (7) into (5) yields the vector $\begin{bmatrix} \boldsymbol{e} \\ \boldsymbol{i} \end{bmatrix}$ where the subvector $\boldsymbol{e} = [E_1 \cdots E_N]^{\mathrm{T}}$ is

$$\begin{bmatrix} E_1 \\ \vdots \\ E_N \end{bmatrix} = \begin{bmatrix} \hat{E}_1 \\ \vdots \\ \hat{E}_N \end{bmatrix} + \begin{bmatrix} d_{1l} - d_{1k} \\ \vdots \\ d_{N,l} - d_{N,k} \end{bmatrix} \Delta I. \tag{8}$$

Now we consider another disturbance to the circuit caused by including in series with m-th VCVS a voltage source ΔV_m. In this case, the right hand side of the modified node equation becomes $\begin{bmatrix} \hat{\boldsymbol{j}} \\ \boldsymbol{0} \end{bmatrix} + \boldsymbol{w}$, where $\boldsymbol{w}$ is an $(N + M) \times 1$ vector of the form $\boldsymbol{w} = [0 \cdots 0 \; \Delta V_m \; 0 \cdots 0]^{\mathrm{T}}$, where ΔV_m occupies $(N + m)$ th position.

Consequently, the disturbed circuit is described by

$$\begin{bmatrix} \boldsymbol{e} \\ \boldsymbol{i} \end{bmatrix} = \begin{bmatrix} \hat{\boldsymbol{e}} \\ \hat{\boldsymbol{i}} \end{bmatrix} + \begin{bmatrix} d_{1,N+m} \\ \vdots \\ d_{N+M,N+m} \end{bmatrix} \Delta V_m \tag{9}$$

which allows the following to be written

$$\begin{bmatrix} E_1 \\ \vdots \\ E_N \end{bmatrix} = \begin{bmatrix} \hat{E}_1 \\ \vdots \\ \hat{E}_N \end{bmatrix} + \begin{bmatrix} d_{1,N+m} \\ \vdots \\ d_{N,N+m} \end{bmatrix} \Delta V_m. \tag{10}$$

III. MODELING THE PARAMETRIC FAULTS

The fault model is created such that the fault is represented by an unknown current or voltage source that can be determined by solving appropriately modified node equations.

Let us consider an element of set Θ specified by the nominal equation $I = \hat{Y} V$. When the element is faulty, the admittance becomes $Y = \hat{Y} + \Delta Y$ and can be modeled as shown in Fig. 1. The circuit in Fig. 1 is equivalent to the circuit depicted in Fig. 2, where $\Delta I = \Delta Y \, V$ and V is the unknown voltage in the faulty circuit. Thus, the fault is represented by the current source ΔI.

If the nodes to which this element is connected are labeled k and l, then the element can be described by the equation $I = \hat{Y} \, (E_k - E_l) + \Delta I$, where

$$\Delta I = \Delta Y \, (E_k - E_l) \tag{11}$$

and the node voltages in the faulty circuit are given by (8).

Similarly, we consider an element of set Λ described by the nominal equation $I = \hat{\lambda} V_x$, where V_x is the controlling voltage between the nodes labeled x_1 and x_2. When the element is faulty $\lambda = \hat{\lambda} + \Delta\lambda$ and can be described by $I = \left(\hat{\lambda} + \Delta\lambda\right) V_x$, or $I = \hat{\lambda} V_x + \Delta I$, where $\Delta I = \Delta\lambda V_x$ that leads to the model shown in Fig. 3.

If the nodes to which the VCCS is connected are labeled k and l then

$$\Delta I = \Delta\lambda \left(E_{x_1} - E_{x_2}\right) \tag{12}$$

and the node voltages in the faulty circuit are given by (8). As in the previous case, the fault is represented by a current source connected to the terminals of the element.

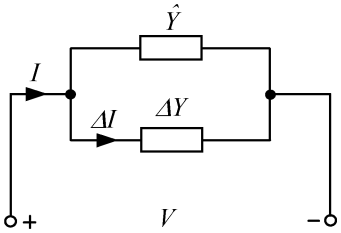

FIGURE 1. Model of the faulty passive element specified by the nominal admittance $\hat{Y}$. Both current ΔI and voltage V are unknown variables. When they are determined the faulty parameter $Y = \hat{Y} + \Delta I/V$ can be found.

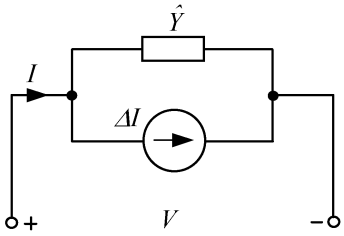

FIGURE 2. Equivalent model of the circuit shown in Fig. 1 including the current source ΔI. This model is used to write the modified node equation.

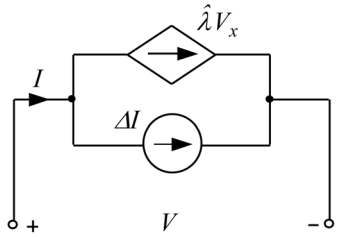

FIGURE 3. Model of the faulty VCCS specified by the nominal transconductance $\hat{\lambda}$. The current source ΔI and the voltage V_x enable to find the faulty parameter $\lambda = \hat{\lambda} + \Delta I/V_x$.

Now we consider an element of set Γ and discuss its disturbance. Let the element be m-th VCVS ($m \in \{1, \cdots, M\}$) specified by the nominal equation $V = \hat{\gamma}_m V_z$ where V_z is the controlling voltage between the nodes labeled z_1 and z_2. The faulty element is described by the equation $V = \left(\hat{\gamma}_m + \Delta\gamma\right) V_z$ or $V = \hat{\gamma}_m V_z + \Delta V_m$, where $\Delta V_m = \Delta\gamma V_z$ and is modeled as shown in Fig. 4. If the nodes to which the VCVS is connected are labeled k_m and l_m, then the circuit in Fig. 4 can be represented by the equation $E_{k_m} - E_{l_m} - \hat{\gamma}_m \left(E_{z_1} - E_{z_2}\right) = \Delta V_m$, where

$$\Delta V_m = \Delta\gamma \left(E_{z_1} - E_{z_2}\right). \tag{13}$$

Thus, the voltage source ΔV_m represents the fault of the VCVS and the node voltages in the faulty circuit are given by (10).

IV. PRINCIPLE OF THE PARAMETRIC FAULT DIAGNOSIS METHOD

The proposed method is based on a diagnostic test arranged in the AC state at frequency f. Two node voltage phasors, E_p and E_r, are measured during this test.

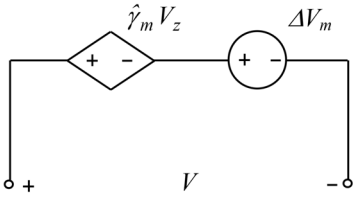

FIGURE 4. Model of the faulty VCVS specified by the nominal voltage transfer ratio $\hat{\gamma}_m$. The voltage source ΔV_m and the voltage V_z enable to find the faulty parameter $\gamma_m = \hat{\gamma}_m + \Delta V_m/V_z$.

Section III shows that the faults of the elements belonging to sets Θ and Λ are represented by a current source connected to the terminals of the faulty element. The node voltages of the faulty circuit are specified by (8). To diagnose an element of set $\Theta \cup \Lambda$, use (8) to write

$$E_p = \hat{E}_p + \left(d_{pl} - d_{pk}\right) \Delta I \tag{14}$$

$$E_r = \hat{E}_r + \left(d_{rl} - d_{rk}\right) \Delta I \tag{15}$$

and solve (14) for ΔI

$$\Delta I = \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}}. \tag{16}$$

To validate this result, we determine whether the result satisfies (15). If it does, or

$$\frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}} = \frac{E_r - \hat{E}_r}{d_{rl} - d_{rk}} \tag{17}$$

the current ΔI specified by (16) is used to estimate the fault.

If the diagnosed element belongs to set Θ, then (11) is used to write

$$\Delta Y = \frac{\Delta I}{E_k - E_l}. \tag{18}$$

The node voltages E_k and E_l are determined using (8) and substituting (16)

$$E_k = \hat{E}_k + \left(d_{kl} - d_{kk}\right) \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}} \tag{19}$$

$$E_l = \hat{E}_l + \left(d_{ll} - d_{lk}\right) \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}}. \tag{20}$$

If the diagnosed element belongs to set Λ, then apply (12) to write

$$\Delta\lambda = \frac{\Delta I}{E_{x_1} - E_{x_2}} \tag{21}$$

where E_{x_1} and E_{x_2} are calculated using (8) and (16)

$$E_{x_1} = \hat{E}_{x_1} + \left(d_{x_1 l} - d_{x_1 k}\right) \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}} \tag{22}$$

$$E_{x_2} = \hat{E}_{x_2} + \left(d_{x_2 l} - d_{x_2 k}\right) \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}}. \tag{23}$$

To diagnose the m-th VCVS belonging to set Γ, we consider a circuit disturbed by the voltage source ΔV_m and apply (13)

$$\Delta\gamma = \frac{\Delta V_m}{E_{z_1} - E_{z_2}}. \tag{24}$$

The voltage ΔV_m is determined using equations

$$E_p = \hat{E}_p + d_{p,N+m}\Delta V_m \tag{25}$$

$$E_r = \hat{E}_r + d_{r,N+m}\Delta V_m \tag{26}$$

that are written based on (10). We solve (25) for ΔV_m

$$\Delta V_m = \frac{E_p - \hat{E}_p}{d_{p,N+m}} \tag{27}$$

and determine whether it also satisfies (26). If it does, or

$$\frac{E_p - \hat{E}_p}{d_{p,N+m}} = \frac{E_r - \hat{E}_r}{d_{r,N+m}} \tag{28}$$

the voltage ΔV_m specified by (27) is used to calculate, based on (10), E_{z_1} and E_{z_2}

$$E_{z_1} = \hat{E}_{z_1} + d_{z_1,N+m}\frac{E_p - \hat{E}_p}{d_{p,N+m}} \tag{29}$$

$$E_{z_2} = \hat{E}_{z_2} + d_{z_2,N+m}\frac{E_p - \hat{E}_p}{d_{p,N+m}}. \tag{30}$$

These equations are substituted into (24) to obtain $\Delta\gamma$.

V. DESCRIPTION OF THE METHOD

In this section, we explain how the proposed method is used to perform parametric fault diagnosis, which includes fault detection as well as locating faulty element and estimating its value.

A. SKETCH OF THE METHOD

1) Analyze the nominal circuit to obtain $\hat{E}_1, \cdots, \hat{E}_N$ at frequency f. Determine the matrix $\boldsymbol{D}$ and register its elements d_{ij}, $i = 1, \ldots, N, j = 1, \ldots, N + M$. Perform the sensitivity analysis to determine a set of parameters that can be tested and two voltages, E_p and E_r, with sufficiently large variations due to deviation of the parameters. Repeat this procedure for frequency f_v. The frequencies f and f_v are selected using the brute–force method.

2) Arrange the diagnostic test in the AC state at two frequencies f and f_v and measure the voltages at nodes p and r for both cases. The voltages are denoted by E_p and E_r at frequency f and E_p^v and E_r^v at frequency f_v. The first pair of voltages is used in steps 4 and 5 of the diagnostic procedure whereas the other pair of voltages is only used to validate the faults in step 6.

3) Create a set A of the elements that are considered to be potentially faulty and select one of the elements

4) If the element belongs to set $\Theta \cup \Lambda$, identify terminals k and l and check if (17) holds. If it does not hold, discard the element. Otherwise, determine ΔY using (18), (16), and (19)-(20) if the element belongs to set Θ, or determine $\Delta\lambda$ using (21), (16), and (22)-(23) if the element belongs to set Λ.

If the selected element belongs to set Γ, check if (28) is satisfied. If it is not satisfied, discard the element, otherwise determine $\Delta\gamma$ using (24), (27), and (29)-(30).

Calculate the value of the parameter using the deviation ΔY or $\Delta\lambda$ or $\Delta\gamma$.

5) Discard the element if its parameter does not deviate or if the determined deviation is incorrect (e.g., $\mathrm{Re}\,(Y + \Delta Y) < 0$, or $\Delta\lambda$ or $\Delta\gamma$ is not a real number). If the element is accepted, add its parameter value to a list of faults. If all elements of set A have been diagnosed, proceed to step 6. Otherwise, select a succeeding element of this set and proceed to step 4.

6) If the list of faults contains more than one parameter, some of them may correspond to virtual faults. Therefore, they are validated as follows. Choose one parameter from the list and analyze the circuit at frequency f_v, substituting its value. Thus, the voltages at nodes p and r are calculated. Compare each of these voltages with the corresponding voltage E_p^v or E_r^v measured during the diagnostic test. If the voltages are equal the fault is accepted, otherwise, the fault is removed. Repeat this procedure for all items in the list.

This validation process is simple to arrange and very fast. The process typically eliminates most of the virtual solutions. Occasionally, the validation can be performed at two frequencies to further improve the results.

B. ADAPTING THE METHOD TO REAL CONDITIONS

The proposed method is effective if the measurement and computation errors are small enough to be neglected. In real circumstances, however, such a situation does not occur due to imperfections. Therefore, the diagnostic procedure should be modified by considering the following conditions.

1) We assume that the measurement accuracy of the AC voltages, in the course of the diagnostic test, is 0.1mV for the amplitude and 0.01° for the phase.

2) If $\left|E_p - \hat{E}_p\right|$ or $\left|E_r - \hat{E}_r\right|$ is less than 0.001 V, the value $\left|\left(E_p - \hat{E}_p\right)\Big/\left(d_{pl} - d_{pk}\right)\right|$ or $\left|\left(E_r - \hat{E}_r\right)\Big/\left(d_{pl} - d_{pk}\right)\right|$ is uncertain and condition (17) cannot be satisfied. In this case, the diagnostic procedure fails. The same note relates to condition (28).

3) During the diagnostic procedure, some complex numbers are required to be equal (see (17) and (28)). If the numbers are denoted by Z_1 and Z_2, we consider them equal if $\frac{|Z_1 - Z_2|}{|Z_1|} < 0.01$.

4) Sometimes the simulation process leads to large currents. In a real circuit, such a current could totally change the behavior of the circuit or even destroy the circuit. In this instance, the circuit model becomes nonrepresentative. Therefore, the tested case should be discarded if the magnitude of a simulated current exceeds an upper limit (e.g., 0.1 A in examples 4 and 5).

5) Some quantities that occur during the diagnostic procedure should be real numbers. If the quantity is a ratio of two complex numbers, the computed value is usually complex, $A + \mathrm{j}B$. We accept it if $\frac{|A|}{\sqrt{A^2+B^2}} > 0.999$.

All the discussed conditions were implemented into the proposed method. In this way, its practical relevance and effectiveness have been improved.

VI. NUMERICAL EXAMPLES OF THE PARAMETRIC FAULT DIAGNOSES

The method proposed in Sections III-V was implemented in the DELPHI environment. It operates on net-list files of the analyzed and diagnosed circuits, with a structure similar to the structure used in the SPICE software. The method is fully automated. After entering the test and validation frequencies, and the test nodes, the appropriate analyses and diagnostic process are performed. The results are saved to a text file. IsSpice4 software from Intusoft is employed to perform the AC sensitivity analysis, which is used to select parameters that can be diagnosed with the assumed measurement accuracy. The calculations are carried out on a PC with an Intel Core i7-6700 processor.

Three numerical examples are presented to illustrate the proposed method. The simulations were performed under the assumption that the measurement accuracy of the voltages during the diagnostic test was as described in Section V.B (point 1).

A. EXAMPLE 1

Let us consider the linear circuit in the AC state, including two voltage amplifiers, shown in Fig. 5. The nominal parameter values are indicated in this figure. The voltage amplifiers are simulated by VCVSs with a voltage transfer ratio (gain) equal to 4.472. The test frequency is $f = 3000$ Hz and the validation frequency is $f_1 = 5000$ Hz. The amplitude of the current source is 10 mA and the phase is 0°. Based on the sensitivity analysis, performed before the test, the diagnostic nodes $p = 4$ and $r = 7$ and the set of diagnosable parameters $\{R_1, R_2, R_3, C_1, C_2, C_3, C_4, S_1, S_2\}$ were selected. The quantities S_1 and S_2 are the voltage transfer ratios of the VCVSs that model the voltage amplifiers.

All 9 parameters were diagnosed considering 26 faults spread across wide ranges. In all cases, the method determined the actual faulty element and correctly estimated its value. However, if we consider the faulty parameter $C_2 = 0.01$ nF, the method fails. The relative errors of the parameter values provided by the method, defined as $\left|\left(x^{\text{actual}} - x^{\text{calculated}}\right)/x^{\text{actual}}\right| 100\%$, are very small and do not exceed 0.5%. The results of nine diagnoses are presented in Table 1. The CPU time of each diagnosis does not exceed 0.05 s. In addition, the Fault Coverages (FCs) were calculated assuming that the considered parameter has random values in the intervals [0.1, 0.95] $*$ (the nominal value) and [1.05, 5] $*$ (the nominal value). 100 draws were made each time. The percentages of correctly indicated faults were taken as FCs. The results are as follows: FC = 100% for parameters R_1, R_2, C_1, C_2, C_3, S_1, S_2, FC = 96.5% for C_4, and FC = 83% for R_3.

Generally, the approach based on testability and ambiguity group determination [8], [15] is very effective for fault diagnosis. However, in the case of a single fault diagnosis, considering the measurement accuracy during the diagnostic test, the sensitivity approach in conjunction with the method proposed in this paper is simpler and has some advantages. Since the method examines all of the elements in the parameter set, then in the case of an ambiguity group, the method finds the actual solution that can be accompanied by virtual solutions.

To explain how the method operates in the case of an ambiguity group, we consider the circuit shown in Fig. 5 and replace the resistor R_1 with a nominal value 16200 Ω by two resistors R_1' and R_1'', where $R_1' = 56000\,\Omega$ and $R_1'' = 22800\,\Omega$, connected in parallel. A fault of the first resistor $R_1' = 47000\,\Omega$ is considered. The method produced two solutions $R_1' = 47020\,\Omega$ and $R_1'' = 21155\,\Omega$ of which the first is close to the actual solution and the second is virtual. Since both solutions satisfy the diagnostic test, they are equally valid.

B. EXAMPLE 2

Let us consider the circuit shown in Fig. 6, which includes two operational amplifiers operating in the linear region. They are represented by the model with two resistors and a VCVS as depicted in Fig. 7. The circuit is driven by two current sources with amplitudes 400 μA and 30 μA and the phase 0°. The nominal parameters are indicated in Figs. 6 and 7. The test frequency is $f = 80$ Hz, and the validation frequencies are $f_1 = 20$ Hz and $f_2 = 200$ Hz. Based on the sensitivity analysis performed before the test, the diagnostic nodes $p = 9$ and $r = 11$ and a set of diagnosable parameters $\{R_1, R_2, R_3, R_6, R_8, C_1, C_2, C_3, C_4\}$ were selected.

All 9 parameters were diagnosed considering 18 of their faults. The obtained results were examined using a validation procedure at frequency $f_1 = 20$ Hz. If the results were unsatisfactory, an additional validation procedure was applied at frequency $f_2 = 200$ Hz. The results are as follows. In 14 cases (77.8%), the method provides only the actual faulty parameter. In 4 cases (22.2%), the method produces the actual faulty parameter accompanied by a virtual faulty parameter. In any case, the value of the actual faulty parameter is accurately estimated. In 9 out of 18 cases, two validation procedures were necessary. The results of 9 fault diagnoses are summarized in Table 2. The relative errors of the parameter values are less than 0.4%. The CPU time of each diagnosis does not exceed 0.07 s.

C. EXAMPLE 3

Let us consider the circuit shown in Fig. 8 containing three operational transconductance amplifiers. The nominal values of the circuit parameters are indicated in this figure. The circuit is driven by a current source with an amplitude of 100 mA and the phase 0°. The amplifiers are modeled by the voltage controlled current source as depicted in Fig. 9, where g_m is the transconductance of the amplifier. Based on the sensitivity analysis, the test nodes $p = 2$ and $r = 3$ and the diagnosable parameters C_1, C_2, g_{m_1}, g_{m_2}, g_{m_3} were selected. The frequency used by the diagnostic procedure is $f = 15$ kHz and the validation frequency is $f_1 = 8$ kHz. All 5 parameters were diagnosed considering 10 of their faults. The

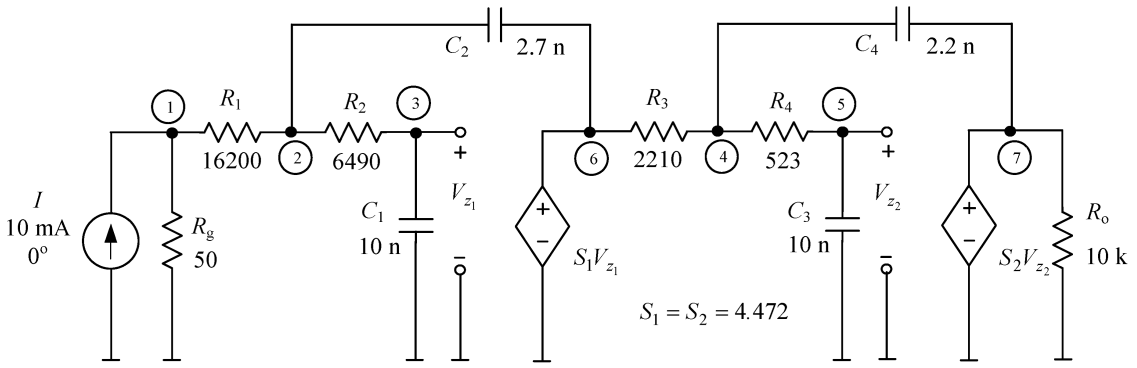

FIGURE 5. Circuit including two voltage amplifiers simulated by the VCVSs with the voltage transfer ratios S_1 and S_2. The parameters R_1, R_2, R_3, C_1, C_2, C_3, C_4, S_1, and S_2 whose nominal values are indicated are considered potentially faulty.

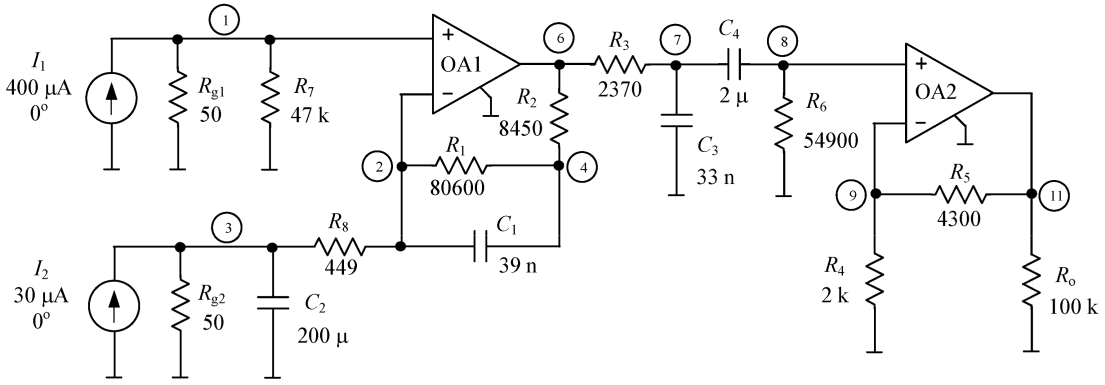

FIGURE 6. Circuit including two operational amplifiers simulated by the circuit shown in Fig. 7. The parameters R_1, R_2, R_3, R_6, R_8, C_1, C_2, and C_4 whose nominal values are indicated are considered potentially faulty.

TABLE 1. Results of nine parametric fault diagnoses for the circuit in Fig. 5.

Case number	Faulty parameter, resistance in Ω, capacitance in nF	Faulty parameter provided by the method, resistance in Ω, capacitance in nF
1	$R_1 = 12000$	$R_1 = 12000$
2	$R_2 = 10000$	$R_2 = 10000$
3	$R_3 = 5300$	$R_3 = 5298$
4	$C_1 = 18.0$	$C_1 = 18.0$
5	$C_2 = 1.2$	$C_2 = 1.19$
6	$C_3 = 15.0$	$C_3 = 14.99$
7	$C_4 = 1.5$	$C_4 = 1.50$
8	$S_1 = 3.3$	$S_1 = 3.30$
9	$S_2 = 5.9$	$S_2 = 5.90$

results are as follows. In all cases, the method provides one or two faulty parameters including the actual parameter and correctly estimates the value. In 6 cases, only one parameter is determined, whereas in 4 cases, the actual parameter is accompanied by a virtual parameter. The relative errors of the actual faulty parameter values are very small and can be neglected. The results of the 5 fault diagnoses are summarized in Table 3. The CPU time in each case does not exceed 0.04 s.

VII. DIAGNOSIS OF SHORT AND OPEN FAULTS

The method described in Sections IV-V can be directly applied to short and open fault diagnoses.

A. DIAGNOSIS OF SHORT FAULTS

A short fault, often referred to as a bridge, is defined as an unintended connection between two otherwise disconnected nodes, say k and l. The fault is simulated by a small resistor R connected to these nodes. If $1\ \Omega < R < 1\ \text{k}\Omega$, the fault is considered a soft short. If $0\ \Omega \leq R \leq 1\ \Omega$, the fault is considered a hard short. The current flowing through this resistor is labeled ΔI and the fault can be modeled as shown in Fig. 10.

The circuit depicted in this figure is described by (8), (14)-(16) and (19)-(20). Thus, similar to Section IV, we state that if (17) is satisfied, then the resistance R of the branch represented by the current source ΔI is

$$R = \frac{E_k - E_l}{\Delta I} = \frac{\hat{E}_k - \hat{E}_l}{E_p - \hat{E}_p}\left(d_{pl} - d_{pk}\right) + d_{kl} - d_{kk} - d_{ll} + d_{lk}. \quad (31)$$

Resistance R defines the fault value.

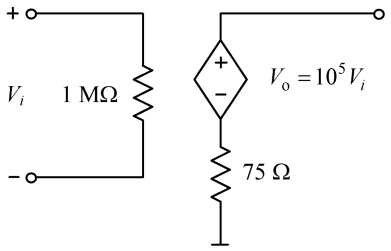

FIGURE 7. Model of the operational amplifier including the VCVS described by the equation $V_o = 10^5 V_i$, with 1 MΩ input resistance and 75 Ω output resistance.

TABLE 2. Results of nine parametric fault diagnoses for the circuit in Fig. 6.

Case number	Faulty parameter, resistance in Ω, capacitance in µF	Faulty parameters provided by the method, resistance in Ω, capacitance in µF	Number of used validation procedures
1	$R_1 = 91000$	$R_1 = 91001$	1
2	$R_2 = 10000$	$R_2 = 10001$	2
3	$R_3 = 1800$	$R_3 = 1798$	2
4	$R_6 = 47000$	$R_6 = 47015$	2
		$R_1 = 79707$	
5	$R_8 = 560$	$R_8 = 560$	1
6	$C_1 = 47 \cdot 10^{-3}$	$C_1 = 47 \cdot 10^{-3}$	1
7	$C_2 = 250$	$C_2 = 250$	2
		$R_1 = 81747$	
8	$C_3 = 22 \cdot 10^{-3}$	$C_3 = 22 \cdot 10^{-3}$	2
9	$C_4 = 1.2$	$C_4 = 1.2$	1

1) EXAMPLE 4

For the circuit shown in Fig. 5, previously considered in Example 1, we diagnose 28 soft short faults ranging from 3 Ω to 730 Ω, occurring between 28 pairs of nodes. Similar to Example 1, a frequency of 3000 Hz is used for the diagnostic procedure and a frequency of 5000 Hz is used for validation.

The results of the 28 diagnoses are as follows. In 23 cases (82.1%), the method correctly locates the pair of bridged nodes and accurately estimates the value of the resistor simulating this fault. In 5 cases (17.9%), the method fails. The results of 12 diagnoses are presented in Table 4. The CPU time of each diagnosis does not exceed 0.1 s.

2) EXAMPLE 5

For the circuit shown in Fig. 6, previously considered in Example 2, we diagnose 48 soft short faults ranging from 2 Ω to 940 Ω, occurring between 39 pairs of nodes. Unlike Example 2, where two validation procedures were used for parametric fault diagnosis, only one validation procedure is applied at the frequency 20 Hz.

The results of the 48 soft short fault diagnoses are as follows. In 38 cases (79.1%), the method correctly locates the pair of bridged nodes, from 39 pairs, and accurately estimates the value of the resistor that simulates this fault.

TABLE 3. Results of five parametric fault diagnoses for the circuit in Fig. 8.

Case number	Faulty parameter, capacitance in nF, transconductance in mS	Faulty parameters provided by the method, capacitance in nF, transconductance in mS
1	$C_1 = 330$	$C_1 = 329.91$
2	$C_2 = 620$	$C_2 = 620.01$
		$g_{m_2} = 37.9$
3	$g_{m_1} = 80$	$g_{m_1} = 80.0$
4	$g_{m_2} = 20$	$g_{m_2} = 20.0$
		$C_2 = 1175.2$
5	$g_{m_3} = 150$	$g_{m_3} = 150.0$

In one case (2.1%), the method correctly locates and identifies the actual short fault, but also provides a virtual fault. In 9 cases (18.8%), the method fails. The results of 15 diagnoses, from 48 diagnoses, are summarized in Table 5. The CPU time of each diagnosis does not exceed 0.1 s.

Examples 4 and 5 present the effectiveness of the method in the area of soft short fault diagnosis. However, numerical experiments reveal that the method is also able to diagnose hard short faults if the measurement accuracy, during the diagnostic test, is very high. Unfortunately, it is difficult to satisfy this requirement in reality.

B. OPEN FAULT DIAGNOSIS

In this section, we consider hard and soft open faults of a branch including an element of set Θ. An open fault occurs when the branch is disconnected. In the extreme case, an open defect causes a break in the circuit connectivity. In reality, however, as a rule, the open is not complete and the fault is simulated by a large resistor connected in series with the branch as depicted in Fig. 11(a), where $\hat{Y}$ is the nominal admittance of the branch. Consequently, the impedance of the branch becomes $Z = \frac{1}{\hat{Y}} + R_o$ and its admittance becomes $Y = \frac{1}{Z} = \hat{Y} + \Delta Y$. Thus, similar to Section III, we obtain the model of the faulty branch as depicted in Fig. 2, repeated in Fig. 11(b).

As shown in previous sections, the occurrence of current ΔI causes the node voltages of the circuit that are specified by (8), (14)-(16), and (19)-(20) to be valid. Thus, if (17) holds, the current I_δ is described by

$$I_\delta = \Delta I + I = \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}} + \hat{Y} V \tag{32}$$

where

$$V = \hat{E}_k - \hat{E}_l + (d_{kl} - d_{kk} - d_{ll} + d_{lk}) \frac{E_p - \hat{E}_p}{d_{pl} - d_{pk}}. \tag{33}$$

Using V and I_δ, we calculate the impedance of the faulty branch $Z = V/I_\delta$ and determine the resistance R_o that simulates the open fault $R_o = Z - \frac{1}{\hat{Y}}$. If $R_o > 10^7\ \Omega$, the fault is considered a hard open fault. If $10^5\ \Omega \le R_o \le 10^7\ \Omega$, the fault is considered a soft open fault. Thus, the open

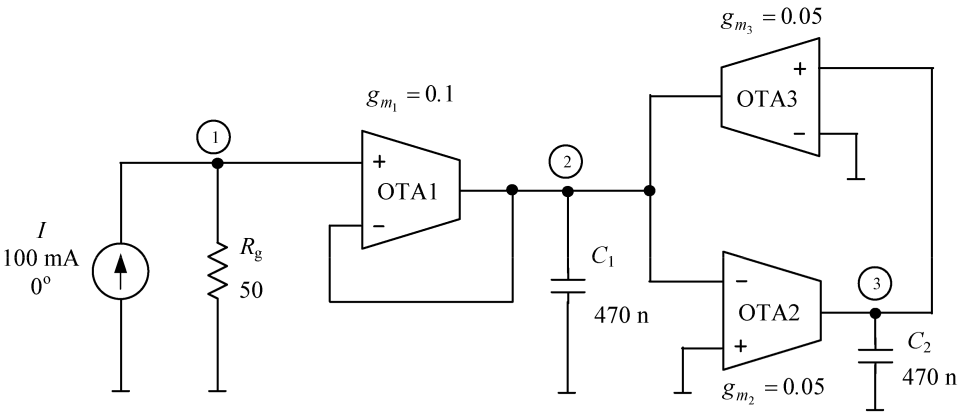

FIGURE 8. Circuit including three operational transconductance amplifiers simulated by the model shown in Fig. 9. The parameters C_1, C_2, g_{m1}, g_{m2}, and g_{m3} whose nominal values are indicated are considered potentially faulty.

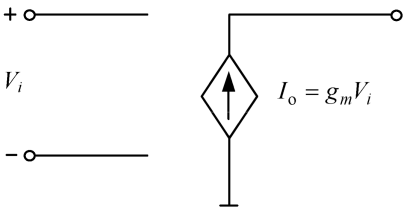

FIGURE 9. Model of the operational transconductance amplifier represented by the VCCS with the controlling input voltage V_i and the controlled output current I_o.

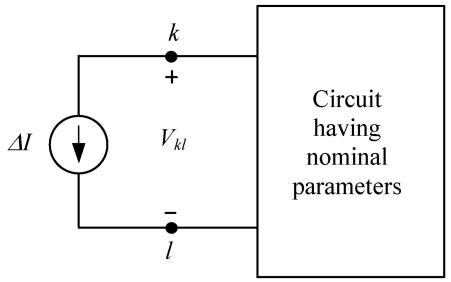

FIGURE 10. Model of the short fault occurring between nodes k and l. The short circuited branch is represented by the current source ΔI. When ΔI and V_{kl} are determined the resistance of the branch can be found.

fault diagnosis can be performed similar to the description in Section V.

1) EXAMPLE 6

Let us consider the circuit shown in Fig. 5. Diagnostic nodes 4 and 7 are selected and the frequency used in the diagnostic procedure is $f = 2$ kHz. A validation test is not required. Eight soft open faults occurring in the branches $R_1, \ldots, R_4$ and $C_1, \ldots, C_4$ numbered 1 – 8 were diagnosed. In 7 cases (87.5%), the method correctly identified the faulty branch and accurately evaluated the resistance R_o. In one case (12.5%), the method failed. The results are presented in Table 6. The CPU time of each diagnosis does not exceed 0.03 s.

TABLE 4. Results of twelve soft short fault diagnoses for the circuit in Fig. 5.

Bridged nodes	Actual soft short resistance in Ω	Soft short resistance in Ω given by the method	Relative error in %
2 – 0	150	149.64	0.24
4 – 0	3	2.92	2.67
7 – 0	380	FAIL	
1 – 2	90	89.62	0.42
1 – 4	50	49.99	0.02
1 – 7	20	19.98	0.10
2 – 4	45	45.62	1.38
2 – 5	15	15.34	2.27
3 – 5	330	328.62	0.42
3 – 6	730	731.75	0.24
4 – 5	320	FAIL	
5 – 6	20	21.35	6.75

Some hard open faults may also be diagnosed as shown in Table 7. However, they typically require a greater measurement accuracy that is difficult to achieve in real circumstances. The CPU time of each diagnosis does not exceed 0.05 s.

VIII. DISCUSSION

A. UNCERTAINTY IN THE CIRCUIT PARAMETERS

The method can be applied to realistic small and medium-sized circuits if they operate in the linear region. The method assumes that the values of the parameters considered as fault–free are nominal. In reality, however, the values do not remain nominal and are scattered in their tolerance ranges. In these circumstances, the method should be modified as shown in the sequel using the circuit of Fig. 5.

Assume the following tolerances for the circuit parameters: 0.5% for the resistors and the gains of the voltage amplifiers, and 1% for the capacitors. These tolerances are realistic in circuits that include discrete passive and IC active devices fabricated in surface-mount technology. In this circuit, we diagnose 26 faults of 9 parameters, similar to Example 1. For each diagnosis, we use 200 sets of values for the parameters considered fault–free. The parameters are

TABLE 5. Results of fifteen soft short fault diagnoses for the circuit in Fig. 6.

Bridged nodes	Actual soft short resistance in Ω	Soft short resistance in Ω given by the method	Relative error in %
1 – 0	10	10.00	0.00
1 – 4	80	79.82	0.22
1 – 6	3	2.82	6.00
1 – 9	14	13.94	0.42
2 – 4	20	21.87	9.35
3 – 0	620	FAIL	
3 – 7	50	50.04	0.08
3 – 8	940	939.99	0.00
3 – 9	250	250.02	0.00
3 – 11	560	560.00	0.00
4 – 6	40	39.17	2.07
4 – 8	200	197.65	1.17
7 – 9	5	5.00	0.00
7 – 11	60	60.06	0.10
8 – 11	800	799.88	0.02

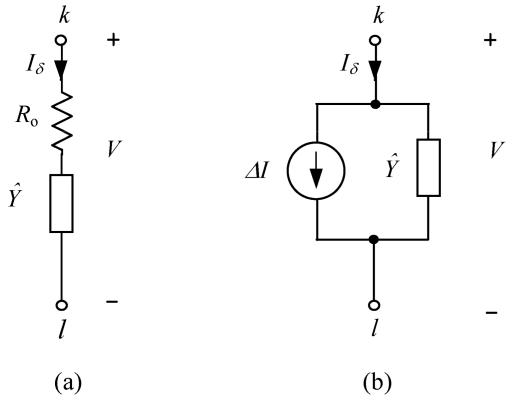

FIGURE 11. Models of the open fault, (a) represented by resistor R_o connected in series with the branch specified by the admittance $\hat{Y}$, (b) equivalent circuit including the unknown current source ΔI connected in parallel with $\hat{Y}$.

TABLE 6. Results of the soft open fault diagnoses for the circuit in Fig. 5.

Number of the faulty branch	Actual value of R_o in Ω	Value of R_o in Ω provided by the method	Relative error in %
1	$3 \cdot 10^5$	$2.999 \cdot 10^5$	0.03
2	$2 \cdot 10^5$	$1.999 \cdot 10^5$	0.05
3	$5 \cdot 10^5$	$4.998 \cdot 10^5$	0.04
4	$5 \cdot 10^5$	FAIL	
5	$3 \cdot 10^6$	$2.907 \cdot 10^6$	1.86
6	$2 \cdot 10^6$	$1.991 \cdot 10^6$	0.45
7	$1 \cdot 10^6$	$1.001 \cdot 10^6$	0.10
8	$7 \cdot 10^5$	$6.979 \cdot 10^5$	0.30

obtained by random selection from their tolerance ranges assuming a uniform distribution. We apply the method described in Section V to each diagnosed fault, but dissimilar to Step 1 in Section V, we consider 200 matrices $\boldsymbol{D}$ corresponding to the 200 sets of previously selected parameter values. The quantities and coefficients used by the computation procedures are the same as in Example 1, except for two constants at points 3 and 5 of Section V.B which are 0.05 and 0.995, respectively. In this fashion, we find a set of $J \leq 200$ values for the parameter x, $\{x^-, \ldots, x^+\}$, rather than a point value. The average value x^{av} is a synthetic coefficient that evaluates x. The results are as follows. In all cases, the method identifies the actual faulty parameter and provides a fairly dense set of possible values. In 23 cases (88.5%), the faulty parameter is the only parameter. In 3 cases (11.5%), the faulty parameter is accompanied by one or two virtual faulty parameters. In all cases, the relative errors specified by $\left|\left(x^{\text{actual}} - x^{\text{av}}\right)/x^{\text{actual}}\right| 100\%$ are quite small. If another validation procedure at frequency 10000 Hz is applied, all the virtual faults are eliminated. The outcomes of 9 fault diagnoses are summarized in Table 8. The time consumed by any fault diagnosis, including the 200 matrices $\boldsymbol{D}$, does not exceed 1.2 s. The fault diagnoses have been supplemented by calculating the confidence interval (CI). For this purpose, 99% CI was determined for each case using MATLAB. The results are presented in Table 8. The obtained results show that the method allows for the effective diagnosis of circuits whose parameter values are scattered in their tolerance ranges. Numerical experiments reveal that a smaller number of parameter sets than 200 leads to less accurate results, while a larger number slightly improves the results at the cost of a significant increase in time consumption.

TABLE 7. Hard open fault diagnoses for the circuit in Fig. 5.

Number of the faulty branch	Actual value of R_o in Ω	Value of R_o in Ω provided by the method
1	$1 \cdot 10^8$	$0.97 \cdot 10^8$
3	$5 \cdot 10^7$	$4.90 \cdot 10^7$

B. DISCUSSION OF THE RESULTS

The diagnostic method proposed in this paper includes both parametric and catastrophic faults. The fault model is created such that the fault is represented by an unknown current or a voltage source that can be determined by solving appropriately modified node equations. The devices fabricated in IC technology (e.g., the operational amplifier) are characterized by their macro models. This is much easier to achieve than specifying the individual elements such as resistors and transistors. The failure of components inside the device affect the parameters of the macro model and are diagnosed using the proposed method. Thus, measurement access to only two selected nodes, except the I/O nodes, should be ensured in the design process. In the circuits made with surface-mount technology, access to the nodes is usually possible.

Numerous experiments show that the method is useful for single fault parametric diagnosis of a broad class of linear electronic circuits. It can be directly extended to double parametric fault diagnosis. In such a case, the main function of the method remains unchanged, but three phasors of appropriate node voltages should be measured during the diagnostic test

TABLE 8. Results of the fault diagnoses for the circuit in Fig. 5 considering the parameter tolerances.

Faulty parameter x_i	Nominal value, resistance in Ω, capacitance in nF	Actual value of x_i	Lower limit x_i^-	Upper limit x_i^+	Average value x_i^{av}	99% CI	Relative error with respect to the average value in %
R_1	16200	12000	11613	12356	11942	[11913, 11972]	0.36
R_2	6490	10000	9668	10220	9941	[9919, 9963]	0.59
R_3	2210	5300	4911	5961	5451	[5392, 5510]	2.85
C_1	10.0	18.0	17.86	18.25	18.05	[18.04, 18.06]	0.28
C_2	2.7	1.2	1.13	1.27	1.21	[1.207, 1.216]	0.83
C_3	10.0	15.0	14.33	15.51	14.84	[14.78, 14.90]	1.06
C_4	2.2	1.5	1.38	1.61	1.50	[1.488, 1.521]	0.00
S_1	4.472	3.3	3.27	3.38	3.32	[3.317, 3.325]	0.67
S_2	4.472	5.9	5.82	5.97	5.90	[5.878, 5.926]	0.00

instead of two phasors. They are used to write three linear equations for two unknown variables, Δx_1 and Δx_2, which is the current ΔI or the voltage ΔV_m, to represent the faults of a pair of elements considered. The system of equations is used to write three sets of equations with the two variables. Each is solved for Δx_1 and Δx_2. If the solutions are the same, the parameters of the elements are calculated similar to the case of a single fault diagnosis. For example, applying this approach for double fault diagnosis of the circuit shown in Fig. 5 and considering 21 pairs of faulty elements, we obtained the correct results in 18 cases (85.7%).

The parametric faults are calculated using mathematical formulas derived in this paper. They operate with complex variables which depend on the circuit elements and voltages measured in the frequency domain with accuracy limited to realistic values. Some real variables which appear in the computation process become complex variables due to rounding errors. In addition, the comparison of two complex numbers close to one another that may occur when the process is running can be erroneous. There are other reasons which may cause some uncertainties in the computation process. Although the method is equipped with mechanisms that effectively minimize these disturbances, they sometimes fail.

The times consumed by the proposed method to diagnose different types of faults present in the circuits shown in Figs. 5, 6 and 8 are as follows. When a fault occurs in the circuits with nominal values of the components considered fault-free, the time consumed by the proposed method to diagnose a parametric or soft short or soft open fault is less than 0.1 s. The relative errors of the parametric faults do not exceed 0.5%. Typical values of the relative errors of the resistors that simulate soft short and soft open faults are 0.5% and 0.1%, respectively. Occasionally they exceed 1% and the maximum value that occurred was 9.35%.

When tolerances of the circuit components are considered, 200 sets of values of the parameters considered as fault–free are used as above. In such cases, the time consumed by the method to diagnose each of the parametric faults does not exceed 1.2 s. The typical relative errors of parametric faults, which are represented by intervals of the parametric values, are less than 1% and their maximum value is 2.85%.

Although some very special cases of parametric fault diagnosis in the silicon chip could be solved by the proposed method it is dedicated to the linear circuits consisting of discrete and IC devices fabricated in surface-mount technology, where the IC devices are characterized by linear macro-models.

IX. CONCLUSION

The method developed in this paper is fast and allows parametric and catastrophic faults in analog linear circuits to be diagnosed. The method is based on some fundamental laws and techniques used in the analysis of electronic circuits [27], [28] and does not employ advanced mathematical tools. Unlike the verification approach, this method achieves all of the fault diagnosis objectives: detection, location, and estimation of the faulty element value. The diagnostic test employed by the method is arranged in the frequency domain. It is simple and requires access to only two nodes. While the test is running, the phasors of the required voltages must be measured at an accuracy of 0.1 mV for the amplitude and 0.01° for the phase. For this purpose, a proper measuring apparatus is necessary.

The method is very effective for soft short and soft open fault diagnosis when adapted to catastrophic fault diagnosis. To diagnose hard short and hard open faults, more accurate measurement data is required.

The computation time for the diagnosis of small and medium-size circuits is very short and ranges from 0.03 to 0.10 s in the circuits presented in this paper. When the size of the circuit is larger, more elements must be considered, which increases the time of parametric fault diagnosis approximately proportionally. As the number of nodes increases, the number of short faults also increases. Doubling the number of nodes approximately quadruples the number of short faults. The computation for a single fault of this type is elementary, so the average time per fault is less than 2 ms. The computational process can be parallelized using multithreading. Therefore, the method could be implemented as an online fault diagnoser.

The limitations of the method are: applicability to linear circuits, diagnosis of single faults, and ability to diagnose

only small and medium-sized circuits. Fault diagnosis of nonlinear circuits requires a different approach and methodology.

Future work will be focused on generalizing the method for multiple fault diagnosis, developing a systematic method of selecting optimal frequencies, and the parametric fault diagnosis of nonlinear circuits using the small signal model.

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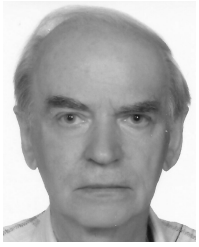

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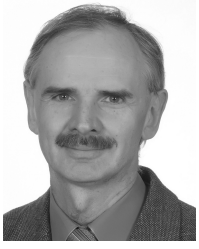

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