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A METHOD FOR THE MEASUREMENT OF THE TURN-ON CONDITION IN MOS TRANSISTORS

H. WALLINGA
Department of Electronics, Twente University of Technology, P.O. Box 217, Enschede, The Netherlands

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Abstract – Metal-oxide-silicon (MOS) integrated circuits usually consist of MOS transistors and interconnections. Both, interconnections and MOS transistors are built up of diffused regions in the bulk substrate and conductive strips (metal or polycrystalline silicon) on top of the oxide. For proper electrical operation the interconnection paths should not exhibit MOS transistor effects, i.e. should not induce inversion layers at the silicon–silicon dioxide interface. Furthermore from a designer's point of view it will be desired that some transistors operate in the saturated mode and others in the non-saturated mode. This implies that a method for the determination of the turn-on of channel conduction is highly desirable for designers of MOS integrated circuits. Using a straightforward definition of turn-on, a fast and simple measurement method will be presented for the determination of the relation between gate voltage and diffused region voltage for MOST structures in the turn-on condition.

Résumé – Les circuits intégrés MOS (métal-oxyde-silicium) se composent en général de transistors MOS et d'interconnexions. Les deux sont composés de régions diffusées dans la base et de bandes conductibles (métal ou silicium polycristallin) au dessus de l'oxyde. Pour une bonne opération les interconnexions ne peuvent pas montrer des effets de transistor MOS, c.à.d. ils ne peuvent pas induire des couches d'inversion à la couche intermédiaire entre l'oxyde et le silicium. En outre il faut que quelques transistors travaillent dans le mode saturé et d'autres dans le mode non-saturé. Cela implique qu'il est très désirable de disposer d'une méthode de déterminer la tension de seuil de la conduction du canal. Utilissant une définition générale de la condition de seuil, une méthode rapide et simple est présentée à déterminer expérimentalement la relation entre la tension de la grille et la tension de la région diffusée pour les structures de transistors MOS dans la condition de seuil.

Zusammenfassung – Metall–Oxyd–Silizium (MOS) integrierte Schaltungen bestehen im allgemeinen aus MOS-Transistoren und deren Verbindungen. Sowohl die Verbindungen als auch die MOS-Transistoren sind aus diffundierten Regionen im Substrat und leitfähigen Streifen (Metall oder polykristallinischem Silizium) auf dem Oxyd aufgebaut. Für richtiges elektrisches Verhalten dürfen die Verbindungsstreifen keine MOS-Transistoreffekte aufweisen, das heisst sie dürfen keine Inversionsschichten an der Grenzfläche des Silizium–Siliziumdioxydes induzieren. Weiterhin ist es vom Entwicklungsstandpunkt erwünscht dass manche Transistoren im Sättigungsbereich arbeiten, während andere im ungesättigten Zustand betrieben werden. Dass bedeutet, dass eine Methode zur Bestimmung des Schwellenwertes der Kanalleitfähigkeit für den Entwerfer der MOS-integrierten Schaltungen besonders wünschenswert ist. Ausgehend von einer allgemeinen Definition des Schwellenwertes wird eine schnelle und einfache Messungsmethode vorgestellt. Sie dient zur Bestimmung der Beziehungen zwischen Gatespannung und der Spannung der diffundierten Regionen für MOST-Strukturen, die sich gerade im Schwellenwert befinden.

NOTATION

- a — $(2\epsilon\epsilon_{si} q N_b)^{1/2}$
- C_{ox} — oxide capacitance per unit area
- G — sheet conductance of channel (mho per square)
- G_{ch} — $G\,W/L$ = channel conductance
- I_d — drain current
- I_r — junction reverse bias leakage current
- L — channel length
- N_b — net impurity concentration in the bulk
- q — magnitude of electronic charge
- Q_m — mobile inversion layer charge per unit area
- Q_{ox} — oxide charge per unit area, effectively located near the Si-SiO_2 interface
- Q_{ss} — surface state charge per unit area at the Si-SiO_2 interface
- t_{ox} — oxide thickness
- V_d — drain voltage with respect to bulk
- V_{ds} — $V_d - V_s$
- V_g — gate voltage with respect to bulk
- V_{gt} — gate voltage in the turn-on condition, for which channel conduction sets in
- V_s — source voltage with respect to bulk

V_p diffused region pinch-off voltage (= voltage of a gated diffused region at the onset of channel formation) with respect to bulk
W channel width
ϵ permittivity of free space
ϵ_{ox} dielectric constant of SiO_2
ϵ_{si} dielectric constant of Si
ϕ $a^2/4C_{ox}^2$
ϕ_F Fermi potential in the substrate
ϕ_{MS} metal–semiconductor work function difference

INTRODUCTION

THE OPERATION of the MOS transistor is based on the induction of an inversion layer or conductive channel at the silicon–silicon dioxide interface by action of the gate field. After discussing the turn-on condition we will in this article be concerned with the measurement of the conditions for which the channel conduction turns on.

Imagine an MOS transistor with common substrate electrode, such as we may find in an MOS integrated circuit. The gate voltage has a value V_g, and the source and drain diffused regions have voltages V_s and V_d.

For a constant source and drain voltage $V_s = V_d$, the gate voltage for which the channel conduction just turns on is called the gate turn-on voltage V_{gt}.

On the other hand, for a constant gate voltage V_g, the voltage of source and drain diffused regions for which the channel conduction just turns on is called the diffused region pinch-off voltage V_p. For turn-on, the applied dielectric displacement in the insulator should be sufficient to compensate the fixed insulator charge and the silicon depletion charge.

Knowledge of the relation between the diffused region pinch-off voltage V_p and the gate turn-on voltage V_{gt} will enable the MOS integrated circuit designer to predict whether an MOS transistor structure with applied voltages will conduct and in which mode it will operate, as clarified by Table 1.

In practice one often deals with an MOS integrated circuit in which different oxide thicknesses and different bulk dopes have been employed, in order to ensure that in the range of applied voltages, the occurence of channels remains confined to active gate regions and is prevented everywhere else. Thus a number of different types (parasitic or real) of MOS transistors will be present inside an IC. For each type of transistor the turn-on condition $V_{gt} = f(V_p)$ should be known in order to predict the voltage range in which the transistor will satisfy its function.

The aim of our work is to propose a generalized definition of the turn-on condition and to present a measurement method to establish the turn-on relationship between the gate voltage V_{gt} and the diffused region voltage V_p.

THE THEORETICAL RELATIONS FOR TURN-ON

Several authors [1–4] have derived mathematical expressions for the relation between the gate turn-on voltage V_{gt} and the diffused region pinch-off voltage V_p:

$$V_{gt} = V_p + \phi_{MS} + 2\phi_F \mp 2\phi^{1/2}|V_p + 2\phi_F|^{1/2} - \frac{Q_{ox} + Q_{ss}}{C_{ox}} \qquad (1)$$

or, in explicit form for V_p:

$$V_p = V_{gt} - 2\phi_F - \phi_{MS} + \frac{Q_{ox} + Q_{ss}}{C_{ox}} \pm 2\phi \times \left[\left(1 \mp \frac{V_{gt} - \phi_{MS} + (Q_{ox} + Q_{ss})/C_{ox}}{\phi}\right)^{1/2} - 1\right]$$

with

$$\phi = a^2/4C_{ox}^2 = 2\epsilon\, \epsilon_{si} q N_b / 4C_{ox}^2 \qquad (2)$$

Table 1.

Mode of operation	p-channel ($V_s, V_d < 0$)	n-channel ($V_s, V_d > 0$)	Properties
Cut-off	$V_s, V_d < V_p$	$V_s, V_d > V_p$	no channel
Saturation	$V_s > V_p$; $V_d < V_p$	$V_s < V_p$; $V_d > V_p$	drain in pinch-off
	$V_s < V_p$; $V_d > V_p$	$V_s > V_p$; $V_d < V_p$	source in pinch-off
Non-saturation	$V_s, V_d > V_p$	$V_s, V_d < V_p$	complete channel

The upper sign applies for p-channel and the lower sign for n-channel devices.

The above relations are derived under the following assumptions:

– the surface state charge and oxide charge are constant,

– the depletion charge remains constant after the inversion charge carrier density at the interface exceeds the bulk carrier concentration,

– the inversion charge tends to zero at the turn-on condition.

Prediction of the turn-on condition with the help of expressions (1) and (2) may be possible if the device parameters are known. This is however usually not the case. Especially Q_{ox} and Q_{ss}, which are dependent among others on incidental process circumstances, which are not fully understood, are difficult to predict. Also the impurity concentration in the bulk may not be precisely known and it may even vary in a distance normal to the surface.

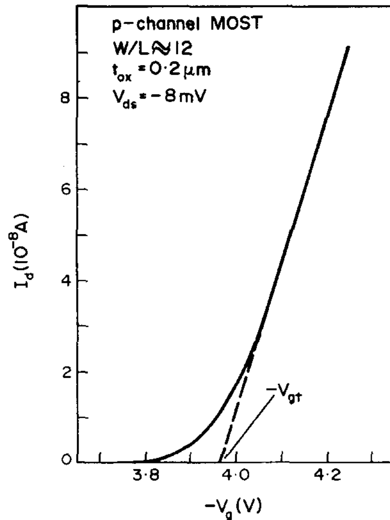

Fig. 1. $I_d - V_g$ curve of a p-channel MOS transistor with small drain-source voltage ($V_{ds} = -8$ mV).

DISCUSSION OF THE TURN-ON CONDITION

A well known method[2] to determine a gate turn-on voltage V_{gt} is to extrapolate the linear part of the $I_d - V_g$ curve of an MOST, measured with small source-drain voltage V_{ds} and constant value of V_s with respect to bulk. The intersection with the V_g axis at $I_d = 0$ is then defined as the turn-on voltage V_{gt}, belonging to the diffused region pinch-off voltage $V_p = V_s$.

In fact, as has been discussed in the literature [1, 2] the turn-on voltage V_{gt}, as determined from such an extrapolation, is described by expression (1) and based upon a constant depletion charge. When we observe an actual measured plot of channel conductance vs. gate voltage (Fig. 1), we find however that for the extrapolated gate voltage $V_g = V_{gt}$ the conductance is not zero, on account of diminishing depletion charge when the inversion layer turn-on condition is approached.

Experiments on several p-channel devices showed that the residual channel conductance for the extrapolated gate voltage $V_g = V_{gt}$ corresponds with a sheet conductance per square between $1\cdot10^{-7}$ mho and $1\cdot10^{-6}$ mho.

Assuming a hole mobility of 200 $cm^2\ V^{-1}\ sec^{-1}$ the corresponding surface concentration of holes would amount to $3\cdot10^9 - 3\cdot10^{10}\ cm^{-2}$.

Now, in view of the need to define the turn-on condition in terms of a residual conduction we propose to define the gate turn-on voltage experimentally as the gate voltage which causes a certain small sheet conductance per square (for example $1\cdot10^{-7}$ mho) at the Si–SiO_2 interface. This will indicate sufficiently the active voltage region where channel formation occurs.

THE TURN-ON MEASUREMENT METHOD

The new measurement method makes use of a control system, which maintains a constant channel conduction in the MOS transistor. The circuit employs an operational amplifier, which is assumed to be ideal, i.e. without any offset voltage and offset current. The input impedance of the operational amplifier as well as the open loop gain are assumed to be infinite, hence the input currents will be zero and $V_{in\,1} = V_{in\,2}$ (Fig. 2).

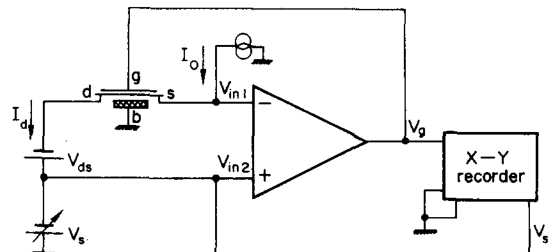

Fig. 2. Measurement circuit. The current source I_0 and the voltage source V_{ds} can be adjusted to attain the desired turn-on condition ($G = 10^{-7}$ mho) in the MOST. The voltage V_s is the independent variable.

The source and drain terminals of the p-channel MOST are connected in series with a small external drain-source voltage V_{ds}. Source and drain terminals may be biased at a variable voltage with respect to the bulk. A current source I_0 is connected to the source and input terminal V_{in1}.

The drain-source voltage will cause a drain current $I_d = |V_{ds}| \cdot G_{ch}$, because $V_{in1} = V_{in2}$ and as the input impedance of the amplifier is infinite, I_d should be equal to I_0. Therefore the channel conductance G_{ch} will have to satisfy $G_{ch} = I_0/|V_{ds}|$. This value will be attained by action of the operational amplifier, which controls the gate electrode of the MOST.

Current source I_0 and voltage source V_{ds} can be adjusted in such a fashion that correction is made for the aspect ratio W/L of the MOST and turn-on is measured for constant surface sheet conductance $G = 1 \cdot 10^{-7}$ mho, i.e. $I_0 = 10^{-7} \cdot |V_{ds}| \cdot W/L$.

In Fig. 2 the basic measurement circuit has been outlined for a p-channel MOST. For n-channel transistors we have simply to change the sign of all the applied voltage and current sources.

In our measurements we used the Keithley model 602 Solid State Electrometer as an almost ideal operational amplifier. It was used in the 'Ohm meter' mode.

The terminals J101 and J105 of the electrometer act respectively as the inverting and non-inverting input, while the terminal J106 provides the output voltage. In this fashion the electrometer supplies a current I_0 at the inverting input J101. The current I_0 may be varied in decade steps between 10^{-5} and 10^{-12} A. The open loop gain is about 10^6 in the 10 V output range. When an output voltage $|V_{gt} - V_s| > 10$ V is required, a d.c. battery has to be connected between the amplifier output and the gate.

The applied drain-source voltage as well as the current source were used to set the channel conductance, which corresponds to a sheet conductance $G = 10^{-7}$ mho, defining the turn-on condition. The lower the voltage V_{ds}, the more uniform is the channel in the MOST. Care should be taken however that the condition $|V_{ds}| \gg |V_{in1} - V_{in2}|$ holds. The voltage of the source diffused region was varied by a slow ramp. The turn-on gate voltage V_{gt} was plotted directly as a function of the source diffused region pinch-off voltage V_p.

Some typical curves obtained by the described measurement method are shown in Fig. 3. It is obvious that the relatively small substrate dopes combined with thin oxides cause a low value of ϕ in expression (1), so the curves approach a straight line with a slope near to 1.

For increased substrate dopes and oxide thicknesses the square root term in expression (1), due to the charge storing capacity of the substrate, becomes more important. Also the influence of oxide and interface charge is greater for thick oxides.

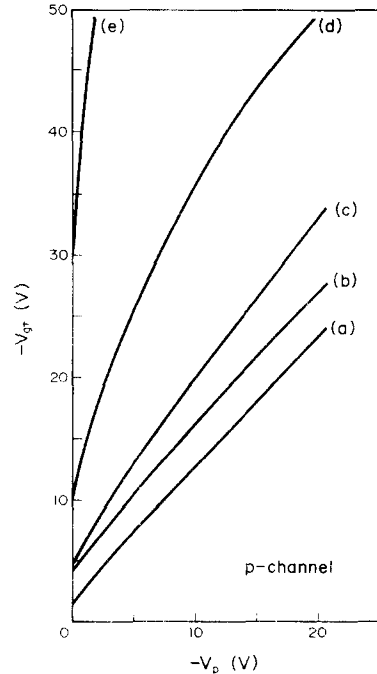

Fig. 3. $V_{gt} - V_p$ curves obtained by the described measurement method. The curves belong to five p-channel MOS transistors of the same geometry but with different impurity concentration underneath the gate oxide and different oxide thicknesses.

$W/L = 12$, $V_{ds} = -8$ mV, $I_0 = 10^{-8}$ A
(a) : $N_b \sim 5 \cdot 10^{14}$ cm^{-3}; $t_{ox} \sim 0 \cdot 12$ μm
(b) : $N_b \sim 5 \cdot 10^{14}$ cm^{-3}; $t_{ox} \sim 0 \cdot 2$ μm
(c) : $N_b \sim 5 \cdot 10^{14}$ cm^{-3}; $t_{ox} \sim 0 \cdot 6$ μm
(d) : $N_b \sim 1 \cdot 10^{17}$ cm^{-3}; $t_{ox} \sim 0 \cdot 2$ μm
(e) : $N_b \sim 1 \cdot 10^{17}$ cm^{-3}; $t_{ox} \sim 0 \cdot 6$ μm

The high impurity dopes from (d) and (e) are obtained by a shallow diffusion of phosphorus in the bulk from a phosphorus doped silane deposited oxide. Dope concentrations and oxide thicknesses are determined from C–V measurements.

DISTURBING EFFECTS ON THE MEASUREMENT METHOD

An eventual leakage current I_r in the source-substrate diffused junction has to be carried off as a source-drain current in the MOST and appears to enlarge the current I_0. For a good quality junction, I_r is much smaller than I_0, and will not influence the measurements.

However in the case of junction defects, the leakage current I_r cannot be neglected and may even surpass I_0, resulting in an increased value of $|V_g|$. The now obtained gate voltage V_g belongs to the drain current $I_d = I_0 + I_r$. Because the leakage current normally will be strongly dependent on the junction reverse voltage, the turn-on curve may be recognised immediately as belonging to an MOST with a defective source-substrate junction, as is obvious from Fig. 4.

For n-channel MOS transistors there may, for low values of V_p, exist a parasitic conducting inversion layer besides the gate covered area.

When the source region is not surrounded by the gate metal, this causes a conductance, which is not controlled by the gate, parallel to the channel. For increased V_s the parasitic inversion layer will vanish. Figure 5 shows that this kind of disturbance also will be recognized at the $V_{gt} - V_p$ plot.

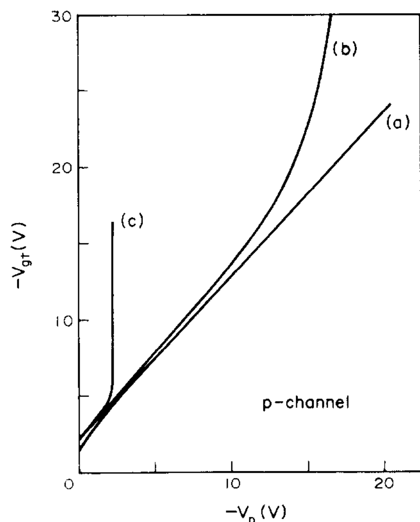

Fig. 4. $V_{gt} - V_p$ plots of three p-channel MOS transistors (a) good quality MOST (b) and (c) MOST's with defective source-bulk junctions. Their leakage currents disturb the measurement of the $V_{gt} - V_p$ plot.

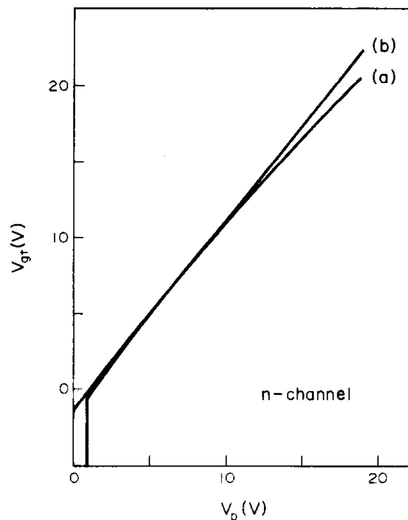

Fig. 5. $V_{gt} - V_p$ plots of two n-channel MOS transistors (a) MOST from which the source is surrounded by the gate metal (b) MOST from which the source is not surrounded by the gate metal. For low values of V_p, there exists a parasitic conducting channel besides the gate.

CONCLUSIONS

A fast, simple and self registrating measurement method is described for the relation between the gate turn-on voltage V_{gt} and the source diffused region pinch-off voltage V_p of an MOS transistor structure. Essential for the method is that the turn-on voltage has to be defined in terms of a turn-on sheet conductance G, which is independent of device geometry.

The obtained curves are useful for the MOS integrated circuit designer in order to obtain information about the voltage ranges in which an MOST operates in the saturated or non-saturated mode, and in which range it is cut-off.

The latter information is of particular interest for the interconnection paths at the top of the oxide, which should not induce conducting layers at the $Si-SiO_2$ interface. Furthermore the described method may be used by the MOS–IC manufacturer as a test on the quality of his products. Especially the value of V_{gt} for $V_s = 0$ V will be of interest as a process parameter.

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