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A Micropower Low-Distortion Digital Pulsewidth Modulator for a Digital Class D Amplifier

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***Abstract*—We describe the design of a micropower digital pulsewidth modulator (PWM) for a hearing instrument Class D amplifier. The PWM embodies a novel delta-compensation (δC) sampling process and a novel pulse generator. The δC process is sampled at the same low rate as reported algorithmic sampling processes and it features a similar low total harmonic distortion (THD). Its arithmetic computation is however, substantially simplified. We analytically derive the double Fourier series expression for the δC process and show that the THD is low. The pulse generator is based on a hybrid 9-b counter 3-b tapped-delay-line. We investigate the compromise between the different design parameters that affect its power dissipation and THD. The complete proposed PWM features a simple circuit implementation (small IC area), micropower low voltage operation ($\sim$22.1 μW @ 1.1 V), low sampling rate (48 kHz) and low harmonic distortion ($\sim$0.2%), thereby rendering it suitable for a practical digital hearing instrument. We verify our design by means of computer simulations and on the basis of experimental measurements.**

***Index Terms*—Class D amplifiers, delta-compensation (δC), digital signal processing process, hearing instruments, pulse generator, pulsewidth modulation, sampling process.**

List of Symbols

B	Pulse duration in the absence of modulation.
H	Amplitude of the PWM pulse.
J_n	Bessel function with order n.
k	Ratio of zero-input duty cycle of the input signal to the ideal 50% zero-input duty cycle.
M	Modulation index ($0 < M < 1$).
m	Carrier harmonic index.
n	Modulating signal harmonic index.
Q	Amplitude of the sinusoidal input modulating signal.
S_1	Current uniform PWM sampled point.
S_2	Next uniform PWM sampled point.
S_{NS}	Current natural PWM sampled point
t_p	PWM pulsewidth.
T	Sampling period.
V_c	Amplitude of the carrier signal.
ω_s	Modulating signal frequency.
ω_c	Carrier frequency.
p	Ratio of the carrier frequency to the input modulating signal frequency (ω_c/ω_s).
α	Amplitude difference between two successive uniform PWM sampled points.
δ	Amplitude difference between natural and uniform PWM sampled points.
ε	Variable sampling factor for the linear interpolation algorithm.
θ	Phase shift of the carrier signal.
ϕ	Phase shift of the input modulating signal.
$F(\theta,\phi)$	PWM pulse amplitude function.
$\Omega(\theta,\phi)$	Pulsewidth function.
$\Omega_T(\theta,\phi)$	Transformed pulsewidth function.

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I. Introduction

CLASS D AUDIO amplifiers (amps) have gained preponderance over their linear audio amp counterparts, e.g., Class A, B, and AB, in particular for hearing instruments (hearing aids). In this application, the critical parameters include low voltage (1.1–1.4 V) and low power (<1 mA) operation and small physical size [small integrated circuits (IC)] for aesthetic considerations. The Class D amp can be advantageously applied because when appropriately designed, it features high power efficiency (of the order of 90%) over a wide modulation index range (signal swing) [1] or where the crest factor is large (e.g., 15 dB). This efficiency is important as most of the power budget for a digital hearing instrument is allocated to the complex signal processing, for example noise reduction [2], as opposed to signal conditioning. In a digital hearing instrument application, a digital Class D amp directly interfaces to the digital processor, thereby eliminating the need for a digital-to-analog converter.

A typical digital Class D amp, as depicted in Fig. 1, comprises a pulsewidth modulation (PWM) process, an output stage, and a low-pass filter stage. The PWM process involves two steps. The first step is a sampling process to determine the digital value of the PWM pulsewidth equivalent to the instantaneous amplitude of the input modulating signal sampled with a carrier. The second step is the PWM pulse generation that generates the pulses that correspond to the digital value of the sampling process. The output stage is a cascade of inverters whose final transistors have a large W/L ratio to obtain a low output impedance, typically <30 Ω, to drive a subminiature receiver (loudspeaker with a typical impedance of less than 600 Ω). The low-pass filter attenuates the carrier frequency components (pulses from the pulse generator), thereby retrieving a continuous-time output signal corresponding to the digital input signal. In some applications, it may be possible to drive the loudspeaker directly from the output stage. This

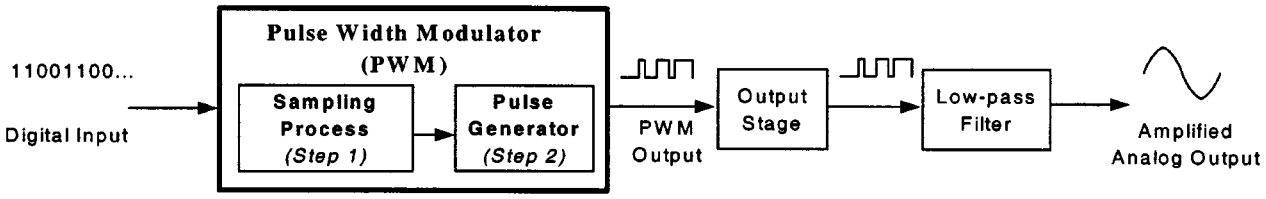

Fig. 1. Digital Class D amplifier.

filterless design [3], however, requires a high sampling rate (∼250 kHz) or equivalently a high carrier frequency and is hence less appropriate for a power sensitive hearing instrument application.

The three PWM sampling processes commonly used in a digital Class D amp are natural, uniform and algorithmic-based processes. The natural process emulates its analog counterpart [4] and requires a very high clock frequency (e.g., a 48-kHz sampling rate with 12-b resolution requires a 48 kHz $\times$ 2^{12} $\approx$ 200 MHz) for high resolution. In practice, however, a lower sampling rate (e.g., ∼512 kHz) is used, primarily for power considerations. The uniform process offers a simpler design primarily because it does not require any digital PWM sampling [5]. However, it is well established that this process exhibits high total harmonic distortion (THD), of the order of 2% (also see Section IV later), and is generally avoided. Examples of reported algorithmic-based processes include linear interpolation [5], noise and ripple shaping [6], $\Delta\Sigma$ [7], and logan [8] algorithms. The hardware requirement of these algorithmic-based processes is relatively complex and in many cases, the power dissipation is somewhat prohibitive for a hearing instrument application.

The reported methodologies to generate the PWM pulse signals in a digital PWM include the fast-clock-counter-based pulse generator [9], tapped-delay-line-based pulse generator [10] and a hybrid counter-tapped-delay-line-based pulse generator [11], [12] termed "hybrid pulse generator." The fast-clock-counter-based method requires a high frequency clock and is therefore less appropriate for a low power application. Although the tapped-delay-line method eliminates the need for a high frequency clock, it instead requires a delay locked-loop (DLL) circuit for accuracy. However, as a digital DLL requires substantial computation, the tapped-delay-line method is also less appropriate for low power applications. In some cases, an analog DLL is used but this circuit realization has poor tolerances due to the variations in the fabrication process. Although the hybrid pulse generators can potentially circumvent the disadvantages of the former two methods, reported designs suffer from other shortcomings. For example, one method [11] requires a stringent operating condition for some transistors to operate in the linear region to limit distortion. Another method [12] requires a fabrication process with critical parameters.

In this paper, we describe a low voltage (1.1–1.4 V) micropower (∼22.1 μW) digital PWM [13] embodying a novel delta-compensation (δC) sampling process and a novel hybrid 9-b counter 3-b tapped-delay-line pulse generator. Our proposed PWM design circumvents the shortcomings of the reported techniques, in particular, it features low sampling frequency, simple hardware, micropower operation and low distortion (∼0.2%). The proposed δC sampling process is clocked at the same low rate as the uniform and reported algorithmic sampling processes, and features THD similar to reported algorithmic sampling processes. Its primary advantage, however, is the substantially simpler arithmetic computation, resulting in simple hardware and micropower operation. We analytically derive the double Fourier series expression for the δC sampling process to evaluate the extent of the harmonic distortion, and show that the THD is low despite the simple arithmetic computation and low sampling rate.

The proposed pulse generator is based on a 9-b counter 3-b tapped-delay-line. We investigate the different design parameters that affect the power dissipation and THD, and show that a 9-b counter 3-b tapped-delay-line is an appropriate design compromise.

We verify our PWM design and analytical derivations by computer simulations and on the basis of experimental measurements. We show that our design is suitable for low voltage micropower applications including hearing instruments.

II. δC PWM Sampling Process

A. Review of Digital PWM Sampling Processes

In this section, we briefly review the reported sampling processes and their associated harmonic distortions. This brief review serves to provide benchmarks for the proposed δC process.

Fig. 2 depicts how the pulsewidths of the natural and uniform sampling processes (both being trailing edge modulations) are obtained. In this diagram, point A along the abscissa time axis is referenced as time $t = 0$, and the magnitude of the carrier is normalized to 1 unit with point F referenced as the initial zero point. By inspection, the pulsewidth t_p(NS) of the natural sampling process can be obtained by simple trigonometry and is shown in (1); we will later derive the pulsewidth of our δC sampling process for comparison

$$\frac{\mathrm{AC}}{T} = \frac{S_{NS}}{1}$$
$$\Rightarrow \quad t_p(\mathrm{NS}) = \mathrm{AC} = T \cdot S_{NS}. \tag{1}$$

where S_{NS} is the magnitude of the natural sampled point. Similarly, the pulsewidth of the uniform sampled process is

$$t_p(\mathrm{US}) = T \cdot S_1. \tag{2}$$

It is well established and apparent here that there is substantial time variation between the pulsewidths of the natural and uniform sampling processes. An alternative viewpoint to compare these processes is to review their well established double

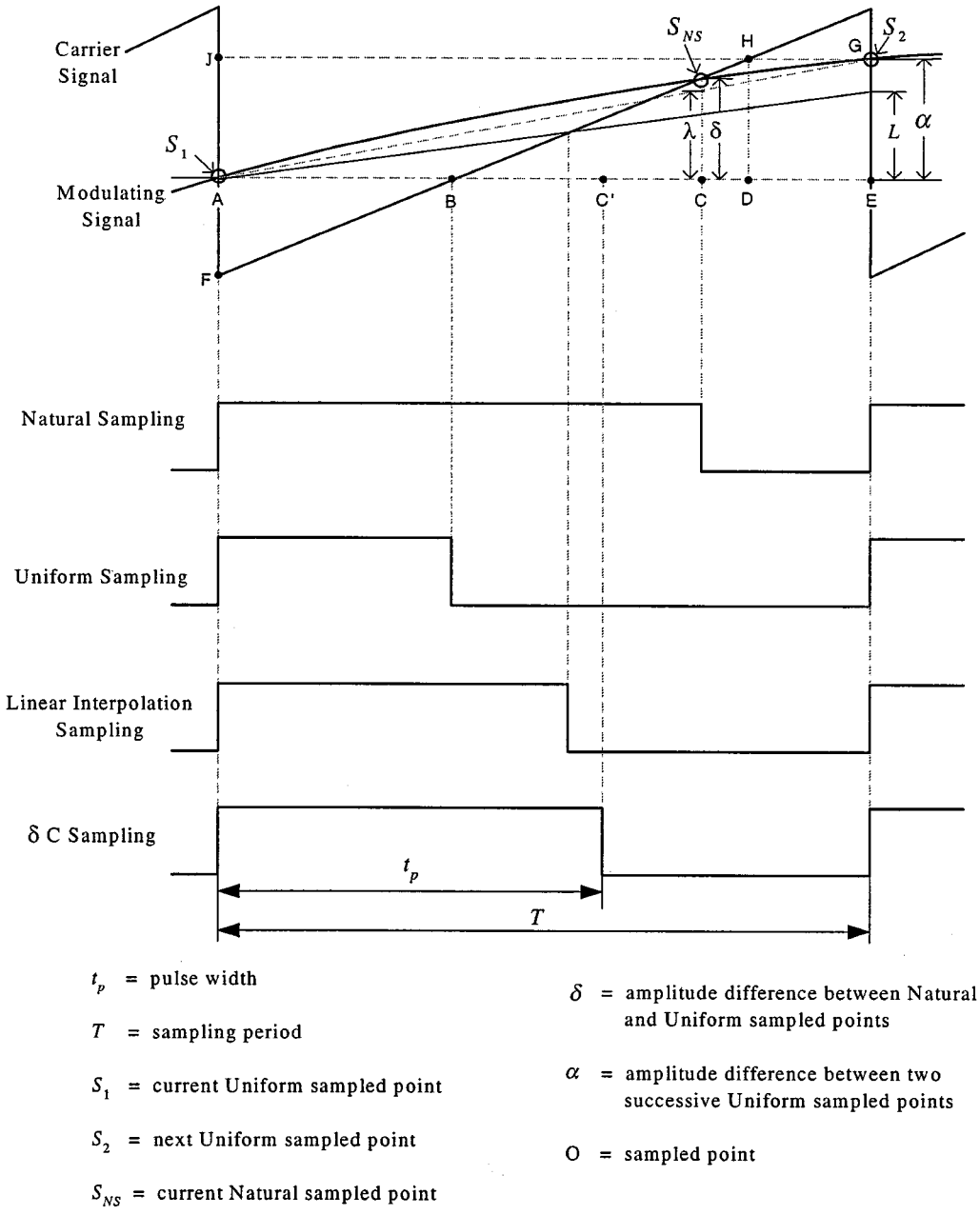

Fig. 2. Natural, uniform, linear interpolation and δC sampling processes.

Fourier series expressions [4] given in (3) and (4). We will later derive a double Fourier series expression for our δC sampling process for comparison

$$F_{NS}(t) = k + \frac{M}{2}\cos(\omega_s t) + \sum_{m=1}^{\infty} \cdot \left[\frac{\sin(m\omega_c t)}{m\pi} - \frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k)\right] - \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \frac{J_n(m\pi M)}{m\pi} \cdot \sin\left(m\omega_c t + n\omega_s t - 2m\pi k - \frac{n\pi}{2}\right) \quad (3)$$

$$F_{US}(t) = k - \sum_{n=1}^{\infty} \frac{J_n\left(\frac{n\pi M\omega_s}{\omega_c}\right)}{\frac{n\pi\omega_s}{\omega_c}} \sin\left(n\omega_s t - \frac{2n\pi k\omega_s}{\omega_c} - \frac{n\pi}{2}\right) + \sum_{m=1}^{\infty} \frac{\sin(m\omega_c t) - J_0(m\pi M)\sin(m\omega_c t - 2m\pi k)}{m\pi} - \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \frac{J_n\left[(m\omega_c + n\omega_s)\frac{\pi M}{\omega_c}\right]}{(m\omega_c + n\omega_s)\frac{\pi}{\omega_c}} \cdot \sin\left[(m\omega_c + n\omega_s)\left(t - \frac{2\pi k}{\omega_c}\right) - \frac{n\pi}{2}\right]. \quad (4)$$

Equation (3) for the natural sampling process can be interpreted as follows. The first term k is the dc component of the resultant PWM output and is of no consequence as it is easily ac-

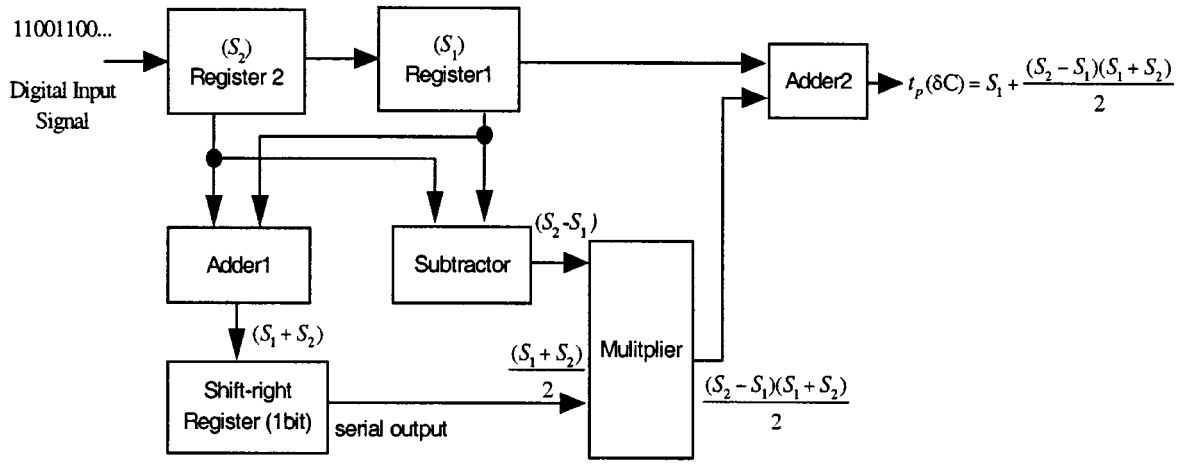

Fig. 3. Digital hardware implementation for the δC sampling process.

commodated. The second term represents the input modulating signal. The third term corresponds to the carrier and its associated harmonics, and is effectively attenuated by the low-pass filter in Fig. 1. The last term represents the modulating signal and its harmonics intermodulated with the carrier and its harmonics, and are normally negligible. It is well established [4] that the second term depicts that theoretically, there is no signal harmonics in the natural sampling process, that is zero THD. Despite this advantage, the major shortcoming of this process is that in practice, a high over-sampling ratio is required [5] for precise sampling as described earlier.

In (4) for the uniform sampling process, the first term k is the dc component and is similarly of no consequence. The second term corresponds to the input modulating signal and its harmonics, and is the source of the large harmonic distortion. The third and last terms are similar to those in (3) and as described earlier, these terms are of little consequence in practice.

A reported methodology that partially circumvents the shortcomings of the natural and uniform sampling processes is the algorithmic linear interpolation (LI) process [5]. The pulsewidth t_p(LI) of this process is obtained through an interpolation between sampled points S_1 and S_2 depicted in Fig. 2, and is described as follows:

$$t_p(\mathrm{LI}) = T\frac{1+S_1}{2+(1-\varepsilon)(S_1-S_2)}, \qquad -1 \le V_c \le 1$$

or

$$t_p(\mathrm{LI}) = T\frac{S_1}{1+(1-\varepsilon)(S_1-S_2)}, \qquad 0 \le V_c \le 1. \quad (5)$$

The main advantage of this process is a low sampling frequency requirement which is the same frequency as the uniform sampling process. Although the harmonic distortion of this sampling process is significantly better than the uniform sampling process (see Section IV), its major shortcoming, as evident from (5), is its algorithmic complexity. This is because this process requires a division operation and the computation to determine ε. As a result, the hardware is relatively complex. The other reported algorithmic-based sampling processes [6]–[8] suffer from similar shortcomings. It is probably instructive to note that in these algorithmic-based sampling processes, the PWM output is obtained after one clock (sampling period) delay. This is because the present pulsewidth is computed only after the next sampling point is obtained, and this delay is of no consequence in audio applications.

We shall now describe our novel δC algorithmic-based PWM sampling process [13].

B. Proposed δC Algorithm

The objective of the δC process as in other algorithmic-based processes is to obtain a pulsewidth that is close to the natural sampling process, but with a substantially reduced sampling rate. With reference to Fig. 2, we do this by estimating δ, that is, $S_{NS} = S_1 + \delta$; note that S_{NS} and S_1 refer to the magnitude of these sampling points with reference to the initial point F. In other words, δ is the amplitude difference between the natural and the uniform sampled points.

We can estimate δ easily. We first approximate the input modulating signal arc S_1S_2 by a straight line AG, refer to Fig. 2. We further approximate λ to be equal to δ, and this approximation is accurate if the PWM sampling frequency is much higher than the input modulating frequency. This is in fact the case for hearing instruments where the PWM sampling frequency is typically 48 kHz or higher and the maximum inband input modulating frequency is usually limited to 6 kHz. α is the amplitude difference between the sampled points S_1 and S_2, and is a known quantity. A pair of similar triangles is now formed between the time interval ac and amplitude δ, and AE and α, that is

$$\frac{\delta}{\alpha} \approx \frac{\mathrm{AC}}{\mathrm{AE}} \Rightarrow \delta \approx \alpha\frac{\mathrm{AC}}{\mathrm{AE}} \quad (6)$$

where AE is the known sampling period T.

To determine ac, we note that another pair of similar triangles is formed between triangles FAB and FJH, yielding AB/AD $= S_1/S_2$. We now estimate $t_p(\delta\mathrm{C}) \approx t_p(\mathrm{NS})$ as

$$\mathrm{AC}' = \frac{\mathrm{AB}+\mathrm{AD}}{2} \approx \mathrm{AC} \quad (7)$$

where time intervals AB and AD are proportional to the known amplitudes of S_1 and S_2, respectively.

By substituting (7) into (6), we obtain

$$\delta \approx \alpha\frac{(\mathrm{AB}+\mathrm{AD})/2}{\mathrm{AE}} = (S_2-S_1)\frac{(S_1+S_2)/2}{1}. \quad (8)$$

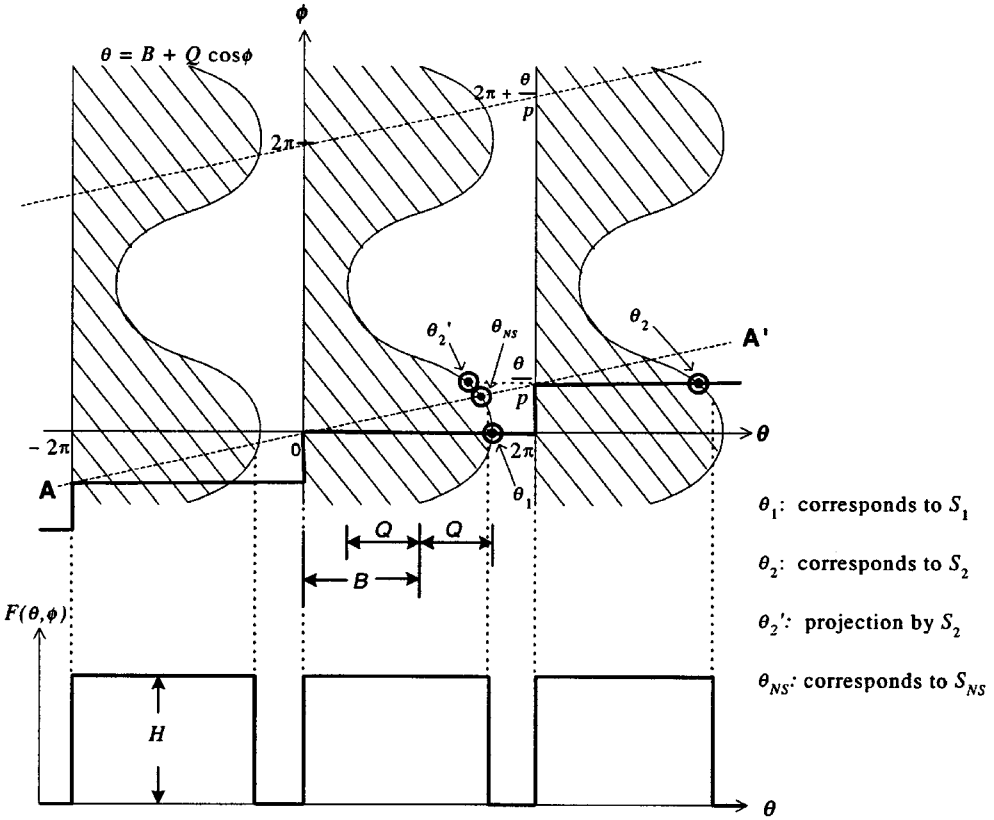

Fig. 4. Spectral analysis by double Fourier series.

Hence, the pulsewidth of the δC process is

$$t_p(\delta\mathrm{C}) \approx T(S_1+\delta) = T\left(S_1 + (S_2 - S_1)\frac{(S_1+S_2)}{2}\right). \tag{9}$$

From (9) and from the example in Fig. 2, we remark that $t_p(\delta\mathrm{C})$ more closely resembles t_p(NS) than t_p(US) and the computation to obtain $t_p(\delta\mathrm{C})$ is very simple. The example in Fig. 2 pertains to a part of the input modulating signal that has positive gradient. We make the same observation when the input modulating signal has a negative gradient. Note that as in other algorithmic-based sampling processes, the PWM output of the δC process is also obtained after one clock delay.

We show in Fig. 3 the block circuit diagram to realize the simple arithmetic operation of the δC process expressed in (9). In Section IV, we will report the simulations and practical measurements of the δC process based on the circuit diagram in Fig. 3.

C. Spectral Analysis for δC Sampling Process

In view of the simplicity of the δC sampling process, it is instructive to analytically determine the extent of its harmonic distortion. We will apply the double Fourier series [4] and [14] on the δC PWM output signal for a single-sided trailing edge PWM of a cosine input modulating waveform. The three-dimensional geometrical representation [14] of the PWM signal can be simplified to a two-dimensional representation [4] depicted in Fig. 4. In Fig. 4, the ordinate represents the phase shift of the input modulating signal, $\phi = \omega_s t$, in the period of 2π. The abscissa represents the phase shift of the carrier frequency, $\theta = \omega_c t$, and line AA′ corresponds to the path of the PWM sampling contour passing through the origin with gradient $1/p = \omega_s/\omega_c$. The pulse amplitude function $F(\theta, \phi)$ is defined by

$$F(\theta,\phi) = \begin{cases} H, & 0 \le (\theta - |\theta|_{2\pi}) \le \Omega(\theta,\phi) \\ 0, & \text{otherwise} \end{cases} \tag{10}$$

where $|\theta|_{2\pi}$ denotes the nearest multiple of 2π less than or equal to θ, $\Omega(\theta,\phi)$ is determined by the input signal and the type of PWM sampling, and H is the height of the wall (or amplitude of the PWM pulse) and is usually normalized to unity. $F(\theta, \phi)$ takes the form of an infinite series of parallel walls placed at periodic intervals of 2π along the θ-axis. In Fig. 4, for the δC sampling, the points θ_1 and θ_2, respectively, correspond to the sampled points S_1 and S_2 in Fig. 2, and can be represented as

$$\begin{aligned} \theta_1 &= B + Q\cos\phi_1 \\ \theta_2 &= B + Q\cos\phi_2 \end{aligned} \tag{11}$$

where $B = 2\pi k$ and $Q = M\pi$.

Following the double Fourier series analysis given in the Appendix, we derive the resultant double Fourier series expression for the δC single-sided trailing edge PWM sampling process (see Fig. 5) as

$$\begin{aligned} F_{\delta\mathrm{C}}(t) = k &- \sum_{n=1}^{\infty} \frac{\omega_c I_{0n}}{2\omega_s n\pi^2} \sin\left(n\omega_s t - \frac{2n\pi k\omega_s}{\omega_c}\right) + \sum_{m=1}^{\infty} \\ &\cdot \left[\frac{1}{m\pi}\sin m\omega_c t - \frac{I_{m0}}{2m\pi^2}\sin(m\omega_c t - 2m\pi k)\right] \\ &- \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \frac{I_{mn}}{2\left(m + \frac{n\omega_s}{\omega_c}\right)\pi^2} \\ &\cdot \sin\left[m\omega_c t + n\omega_s t - 2m\pi k - \frac{2n\pi k\omega_s}{\omega_c}\right] \end{aligned} \tag{12}$$

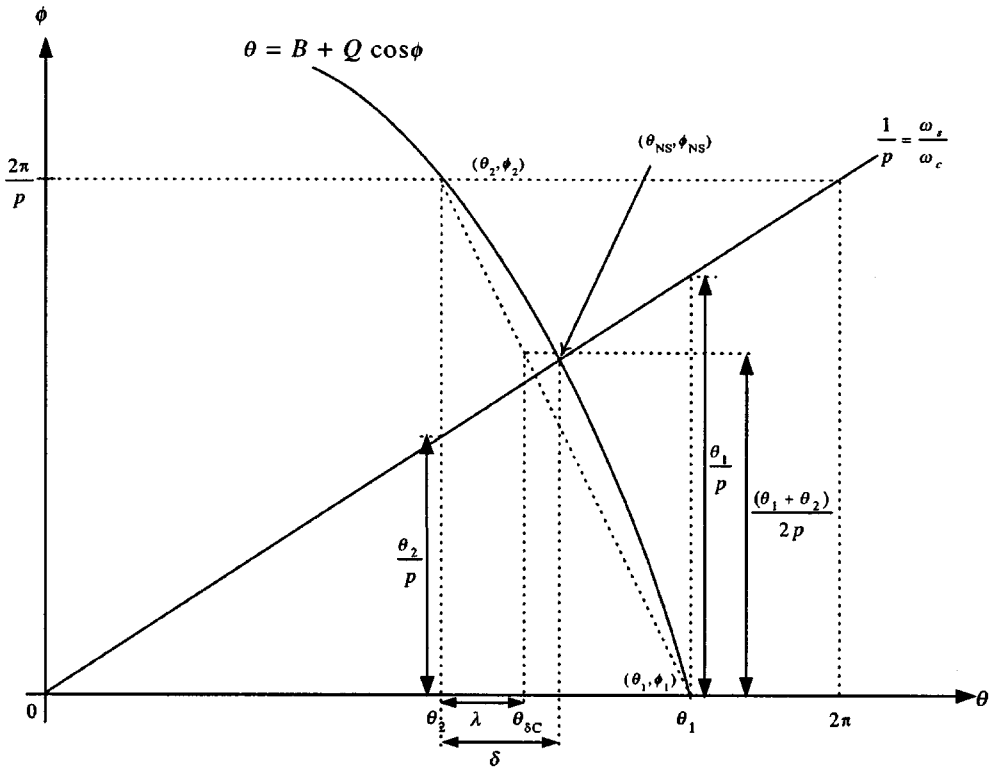

Fig. 5. Detailed illustration of the δC single-sided trailing edge PWM sampling.

where

$$I_{0n} = \int_0^{2\pi} e^{-jn\Phi} e^{-j(nQ/p)\cos\Phi} \cdot \exp\left(j\frac{nBQ}{2p\pi}\sin\frac{2\pi}{p}\sin\Phi\right) \cdot \exp\left(j\frac{nBQ}{p\pi}\sin^2\frac{\pi}{p}\cos\Phi\right) \cdot \exp\left(j\frac{nQ^2}{8p\pi}\sin\frac{4\pi}{\pi}\sin 2\Phi\right) \cdot \exp\left(j\frac{nQ^2}{4p\pi}\sin^2\frac{2\pi}{p}\cos 2\Phi\right) d\Phi$$

$$I_{m0} = \int_0^{2\pi} e^{-jmQ\cos\Phi} \exp\left(j\frac{mBQ}{2\pi}\sin\frac{2\pi}{p}\sin\Phi\right) \cdot \exp\left(j\frac{mBQ}{\pi}\sin^2\frac{\pi}{p}\cos\Phi\right) \cdot \exp\left(j\frac{mQ^2}{8\pi}\sin\frac{4\pi}{\pi}\sin 2\Phi\right) \cdot \exp\left(j\frac{mQ^2}{4\pi}\sin^2\frac{2\pi}{p}\cos 2\Phi\right) d\Phi$$

$$I_{mn} = \int_0^{2\pi} e^{-jn\Phi} \exp\left(-j\left(m+\frac{n}{p}\right)Q\cos\Phi\right) \cdot \exp\left(j\left(m+\frac{n}{p}\right)\frac{BQ}{2\pi}\sin\frac{2\pi}{p}\sin\Phi\right) \cdot \exp\left(j\left(m+\frac{n}{p}\right)\frac{BQ}{\pi}\sin^2\frac{\pi}{p}\cos\Phi\right) \cdot \exp\left(j\left(m+\frac{n}{p}\right)\frac{Q^2}{8\pi}\sin\frac{4\pi}{\pi}\sin 2\Phi\right) \cdot \exp\left(j\left(m+\frac{n}{p}\right)\frac{Q^2}{4\pi}\sin^2\frac{2\pi}{p}\cos 2\Phi\right) d\Phi.$$

We interpret (12) as follows. The first term, as in (3) and (4), is the dc component. The third term corresponds to the carrier and its associated harmonics. The fourth term represents the input modulating signal and its harmonics intermodulated with the carrier and its harmonics. As explained earlier, these third and fourth terms are of little consequence in practice. The second term comprises the modulating signal and its harmonics, and is the source of the harmonic distortion.

To evaluate the extent of this harmonic distortion, we note that the integral term in the second term of (12) is a complex term comprising real and imaginary components. As this term appears to be mathematically untractable, we can employ the numerical integration method to determine the magnitude of the individual signal harmonics, and eventually determine the THD.

To appreciate the extent of the harmonic distortion of the δC process, we now compare the THD of the δC sampling process in (12) with that of the second term in (4) of the uniform sampling process. We present in Fig. 6 the THD of the δC and uniform sampling processes, respectively. On the basis of Fig. 6, we remark that the harmonics of the δC sampling process is substantially smaller than that of the uniform sampling process. As a case in point, for $M = 0.9$ and $p = 48$, the THD of the δC PWM sampling process is approximately 23 times (27 dB) lower than the uniform sampling process. In Section IV, we will make further comparisons between the proposed δC sampling process and the other processes.

III. Proposed Hybrid PWM Pulse Generator

We show in Fig. 7 our proposed 12-b hybrid pulse generator comprising a 9-b counter and a 3-b tapped-delay-line; the reason for this partitioning is described in Section IV. The 12-b data is partitioned into a 9-b most-significant portion (MSP) and a 3-b least-significant portion (LSP) and they are, respectively, the

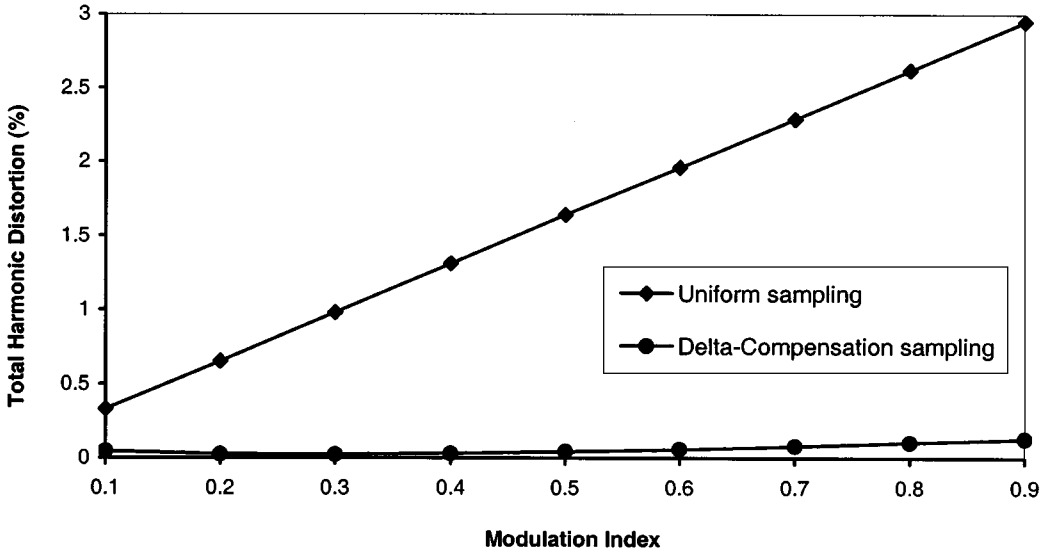

Fig. 6. Theoretical THD comparison between the δC and uniform sampling processes.

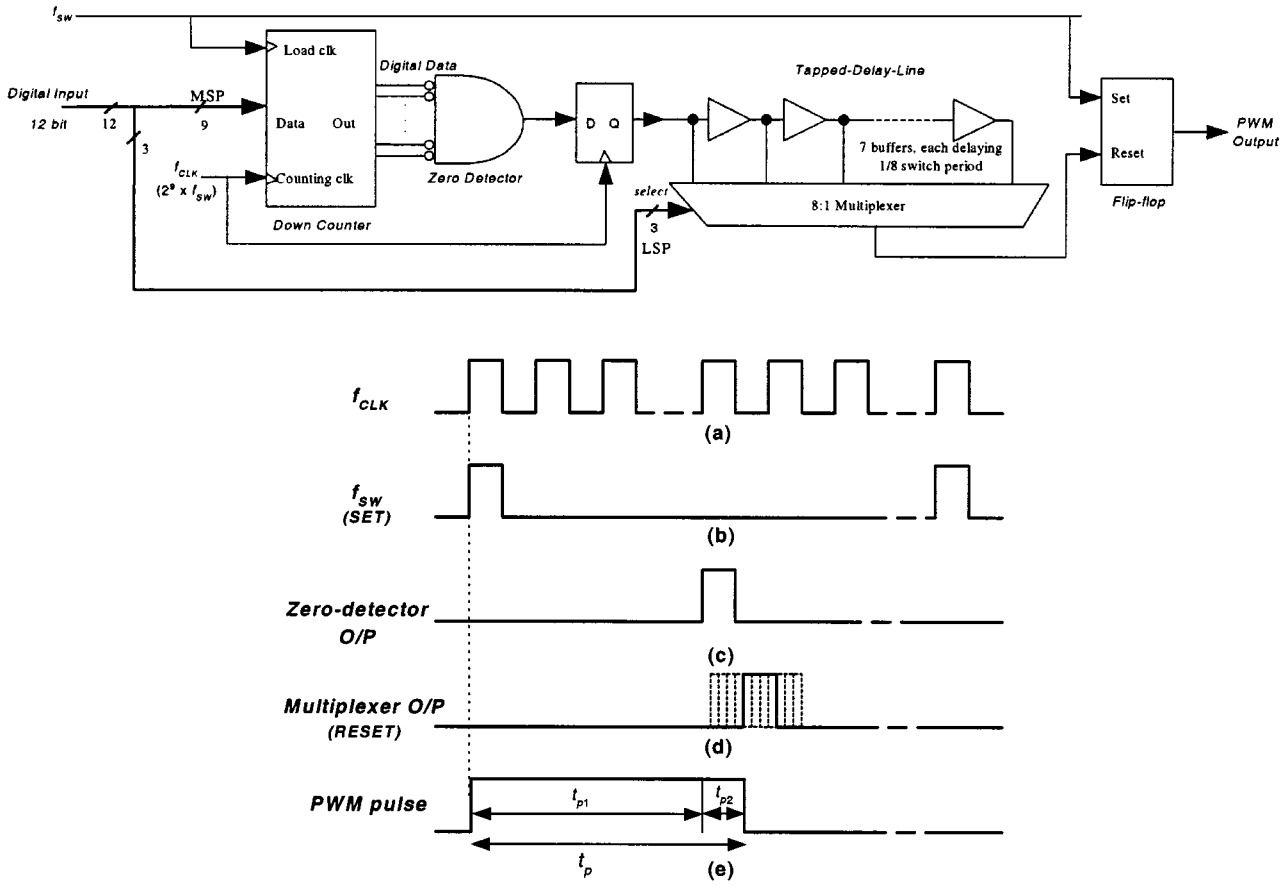

Fig. 7. Hybrid 9-b counter 3-b tapped-delay-line PWM pulse generator. Timing diagram of the hybrid PWM pulse generator. (a) 24.576 MHz clock signal $f_{\rm CLK}$. (b) SET signal to start the PWM pulse by $f_{\rm SW}$. (c) Zero-detector output. (d) RESET signal to end the PWM pulse by the multiplexer output. (e) PWM output comprising t_{p1} generated through the 9-b counter and t_{p2} through the 3-b tapped-delay-line.

inputs to a down counter and a tapped-delay-line. The tapped-delay-line is simply a cascade of seven CMOS inverters.

The timing diagram in Fig. 7 shows how the PWM pulse, t_p, is generated from the proposed hybrid pulse generator. The sampling clock $f_{\rm SW}$ and the counter clock $f_{\rm CLK}$ for the down counter are set at 48 kHz and 24.576 MHz, respectively. The time t_{p1} of the PWM pulse is determined by the MSP and t_{p2} is determined by the LSP. The PWM output is set high on the rising edge of $f_{\rm SW}$ and the down counter will commence counting down the 9-b data to zero. When the count reaches zero, the 3-b tapped-delay-line is initiated. In this LSP, the 3-b tapped-delay-line is divided into eight equal clock periods and is se-

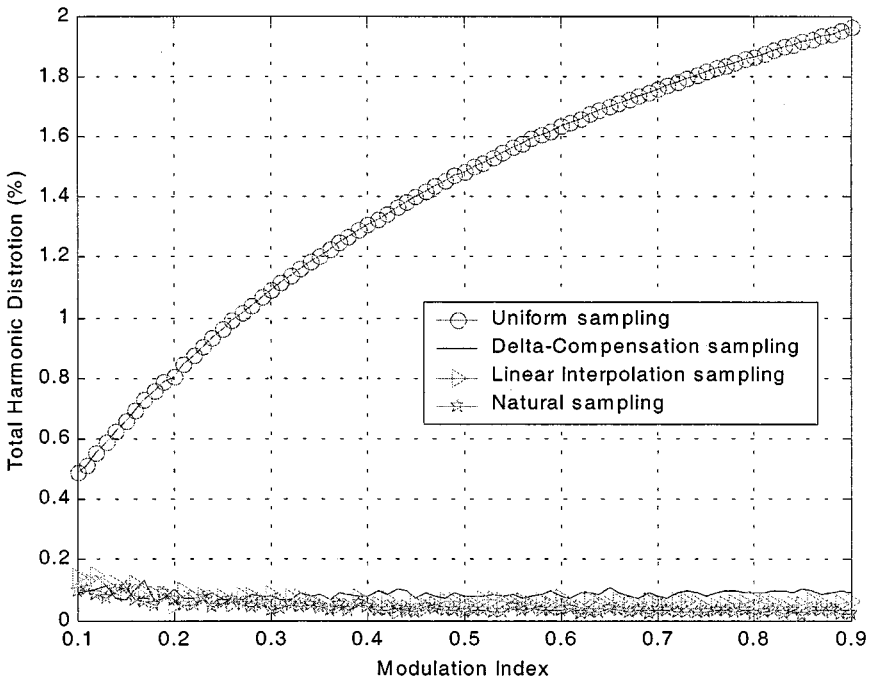

Fig. 8. A comparison of THD on different PWM sampling processes at different modulation indexes, M. The fundamental frequency is 1 kHz, resolution = 12 b, sampling frequency $f_{\rm SW} = 48$ kHz.

lected by an 8 : 1 multiplexer whose output depends on the value of the LSP. The overall PWM pulsewidth $t_p = t_{p1} + t_{p2}$ is equivalent to the 12-b digital value determined by the sampling process.

We adjust the propagation delay of the tapped-delay-line by selecting the appropriate aspect ratio of the transistors of the CMOS inverters. The variation of the delay time for a tapped-delay-line to a first-order depends on the tolerance of the capacitance at the output of the inverter and the threshold voltage V_T of the fabrication process. For a 12-b resolution input signal sampled at 48 kHz, we can show that the deviation due to worst-case variation of a typical CMOS fabrication process will result in a delay (for a 3-b tapped-delay-line) between 28.5 and 52.9 ns where the nominal delay is 40.7 ns. We can subsequently show that the worst-case THD for the 12-b pulse generator embodying a 3-b tapped-delay-line with worst-case time tolerances due to the fabrication variations, is a low 0.19% and the average THD for typical fabricated component variations is 0.10%. These distortion values are all well within practical and acceptable limits for many applications including hearing instruments.

In view of this low THD, it may be possible to omit the 3-b tapped-delay-line. In this extreme case, the worst-case THD of the 9-b counter-based pulse generator is 0.36% compared to a 12-b counter-based pulse generator of 0.09%.

IV. Simulation and Experimental Results

We present in Fig. 8 a comparison of the THD of the natural, uniform, linear interpolation and the δC sampling processes over a range of the modulation indexes M. In this study, the pulsewidths of these respective sampling processes given in (1), (2), (5), and (9) were used, and we determine the THD by using a 16384-point fast Fourier transform (FFT) analysis in MATLAB.

We note from Fig. 8 that the THD of the δC sampling process is low (average = 0.1%) over the full modulation index range and is substantially better than the uniform process, and is slightly worse than the linear interpolation process; note that we have chosen ε of the linear interpolation process for the best possible condition, i.e., for its lowest THD. It is, however, worthwhile reiterating that this is achieved with much simpler arithmetic computation [see (9)] and with simple hardware (Fig. 3). The THD improvement of the δC process over the uniform sampling process becomes more apparent for higher modulation indexes. We had earlier intuitively noted this in (12) in Section II-C. For the case example given there, the THD reduction agrees well with that obtained from Fig. 8; there are some differences for other modulation indexes and we attribute this to the 12-b resolution used in the simulations and to the approximations made in the derivation of (12).

We simulated the circuit design in Fig. 3 for realizing the δC sampling process and a circuit for the linear interpolation process using a 0.35-μm CMOS process cell library and at 1.1 V operation. The multiplier used is based on the well established Wallace multiplier. The simulated power dissipation of the circuit for the δC and linear interpolation is 1.7 and 5.0 μW, respectively. This shows that as a consequence of the simplicity of the δC sampling process, its power requirement is substantially smaller than the linear interpolation process—it is approximately a third of the power dissipation of the linear interpolation process. A further advantage of the δC process is its hardware simplicity. The transistor count for the circuits for the δC sampling process and for the linear interpolation is 11 527 and 20 132, respectively. This transistor count difference can be translated as a comparison of the required IC area—the IC area for realizing the δC sampling process is approximately 57% of that required for the linear interpolation process. In summary, the δC process dissipates substantially lower power and requires

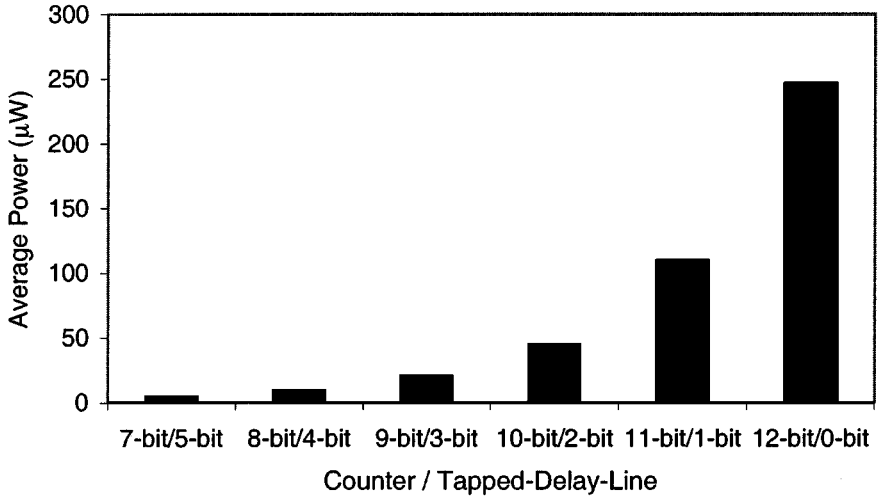

Fig. 9. Relationship between power dissipation and the allocation of the number of bits for the counter/tapped-delay-line of the 12-b PWM pulse generator.

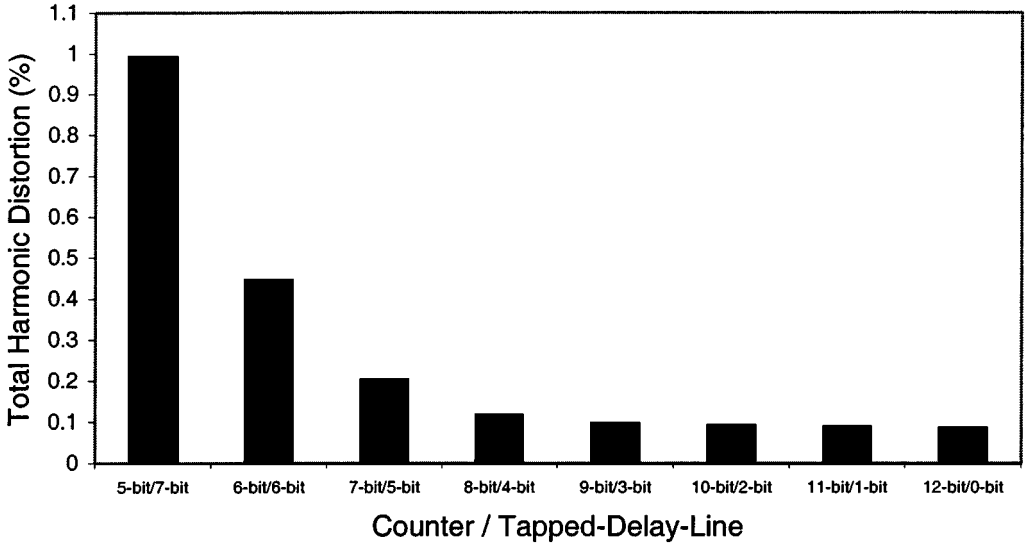

Fig. 10. Relationship between THD and the allocation of the number of bits for the counter/tapped-delay-line of the 12-b PWM pulse generator.

substantially smaller area than the linear interpolation process for a 12-b realization.

As the dominant power dissipation of the PWM is due to the pulse generator, we investigate the consequences of allocating the number of bits to the counter and to the tapped-delay-line for a 12-b signal representation. We show in Fig. 9 and Fig. 10, the effect of the allocation of the number of bits on the average power dissipation and average THD. From these figures, we remark that a larger number of bits allocated to the counter improves the THD but at the expense of higher power dissipation. From this study, we recommend a 9-b allocation to the counter and a 3-b allocation to the tapped-delay-line as a good design compromise. This pulse generator design results in a low power dissipation of 20.4 μW and a low average THD of 0.1%.

The complete PWM embodying the δC sampling process and 9- counter 3-b tapped-delay-line pulse generator dissipates 22.1 μW at 1.1 V operation and the average THD is 0.2%.

To verify our theoretical derivations and simulations, we construct and measure the THD of the entire digital Class

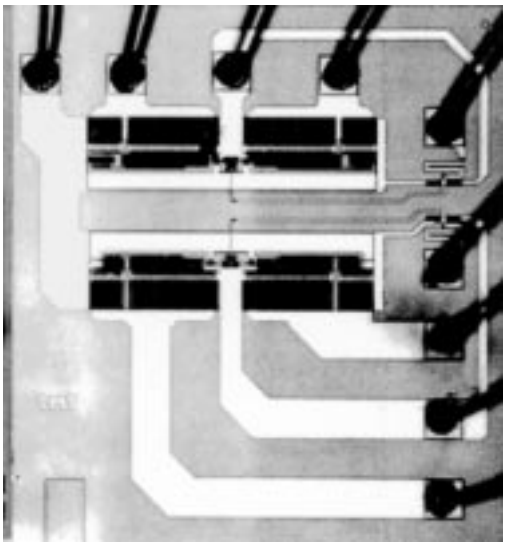

Fig. 11. Microphotograph of the Class D output stage.

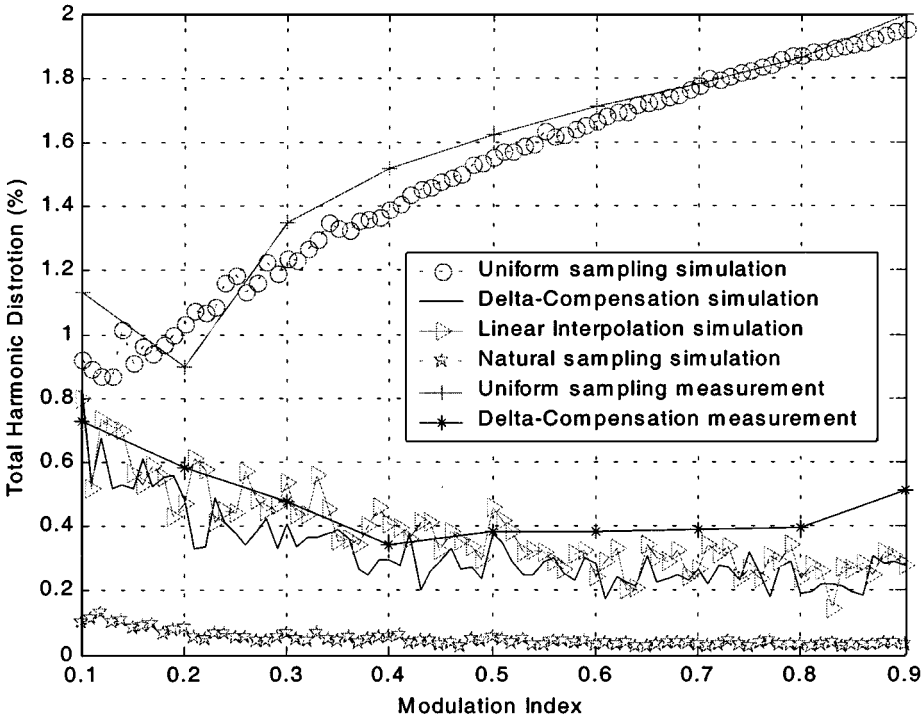

Fig. 12. Comparison of THD from Class D amp realizations embodying different sampling process and the pulse generator obtained from simulations and from experimental measurements.

D amp depicted in Fig. 1 embodying the PWM, an output stage and a low-pass filter. The PWM was realized on a CPLD while the output stage (bridge-output) was realized in a prototype IC depicted in Fig. 11. The output impedance of this output stage is 20 Ω. As it is not possible to realize a tapped-delay-line in the CPLD, the tapped-delay-line in the pulse generator was omitted in this experiment; the counter is retained as a 9-b counter. As previously discussed, this omission would increase the THD by 0.26% as compared to 12-b counter pulse generator.

We summarize in Fig. 12 the THD of Class D amps based on different approaches obtained from computer simulations and from experimental measurements. All approaches for the Class D amps employ the 9-b pulse generator (without the 3-b tapped-delay-line) except for the Class D amp with the natural sampling process that employs a 12-b counter pulse generator. The observations made on Fig. 8 apply. Furthermore, we note that even with the additional 0.26% THD due to the omission of the 3-b tapped-delay-line is considered, the actual average THD for the Class amps with the δC algorithmic process and the 9-b pulse generator is approximately 0.4% and is still within acceptable practical limits for many applications. We note that the THD obtained from computer simulations and from experimental measurements agree well, thereby verifying our theoretical analysis and proposed designs.

Another well-accepted figure-of-merit parameter that qualifies an audio output other than THD, is the signal-to-noise ratio. On the basis of the computer simulations and experimental measurements, we conclude that the floor noise for the δC sampling process and pulse generator for the same number of bits used is approximately the same as the other practical implementations including the uniform sampling process and the linear interpolation sampling process.

In summary, our proposed δC sampling process and proposed pulse generator are suitable for low voltage, micropower Class D amps including hearing instrument applications.

V. Conclusion

We have described a low voltage micropower digital PWM embodying a novel δC sampling process and a novel pulse generator. The δC sampling process required simple arithmetic computation and simple hardware, and featured a low THD. We have analytically shown that the THD of the δC process is low. The pulse generator was based on a hybrid counter-tapped-delay-line design. We have investigated the effects of the number of bits allocated to the counter and tapped-delay-line on THD and power dissipation, and have recommended a respective 9-b and 3-b allocation. The complete Class D amp embodying the proposed δC sampling process and proposed hybrid pulse generator featured a low voltage micropower operation with a low THD. Our theoretical derivations and designs have been verified by computer simulations and on the basis of experimental measurements.

Appendix
Evaluation of Fourier Series Coefficients for the δC Sampling Process

With reference to (10) and (11), we apply the double Fourier series analysis to evaluate the Fourier series coefficients for the δC sampling process. First, we substitute θ as a function of ϕ so that the ϕ points correspond to the θ_1 and θ_2 points, i.e.

$$\phi_1 = \left\lfloor \frac{\theta}{2\pi} \right\rfloor \frac{2\pi}{p}$$
$$\phi_2 = \left(\left\lfloor \frac{\theta}{2\pi} \right\rfloor + 1 \right) \frac{2\pi}{p} \tag{13}$$

where $\lfloor \theta/2\pi \rfloor$ denotes the nearest integer less than or equal to $\theta/2\pi$.

A detailed illustration of the δC single-sided trailing edge PWM sampling corresponding to Fig. 4 is depicted in Fig. 5. As explained in Section II-B earlier, we can approximate λ to be equal to δ, and by using simple geometry, we can show that

$$\frac{\delta}{\theta_1 - \theta_2} \approx \frac{\frac{2\pi}{p} - \frac{(\theta_1+\theta_2)}{2p}}{\frac{2\pi}{p}}. \tag{14}$$

Using (14), we easily derive an expression for the sampling point

$$\begin{aligned}\theta &= \theta_2 + \delta \\ &= \theta_1 + (\theta_1 - \theta_2)\left(1 - \frac{(\theta_1+\theta_2)}{4\pi}\right) \\ &= \theta_1 + (\theta_2 - \theta_1)\frac{(\theta_1+\theta_2)}{4\pi}.\end{aligned} \tag{15}$$

By substituting (11) and (13) into (15), we can now show that the pulsewidth function of the δC sampling contour $\Omega(\theta, \phi)$ is (16) shown at the bottom of the page.

The PWM spectrum cannot be obtained directly by evaluating the double Fourier series along the sampling contour because the δC sampling contour is discontinuous in the (θ, ϕ) coordinate space due to the discrete term $\lfloor \theta/2\pi \rfloor$. We overcome this difficulty by transforming (15) into a continuous function with a new term

$$u = \left(\phi - \left\lfloor \frac{\theta}{2\pi} \right\rfloor \frac{2\pi}{p} + \frac{\theta}{p}\right). \tag{17}$$

By straightforward manipulation of (17), we obtain

$$\phi = u - \frac{\theta}{p} \qquad \text{for} \quad 0 \le \theta < 2\pi. \tag{18}$$

We now rewrite the transformed pulsewidth function $\Omega_T(\theta, u)$ as

$$\begin{aligned}\Omega_T(\theta, u) &= B + Q\cos\left(u - \frac{\theta}{p}\right) \\ &\quad - \frac{4BQ\sin\frac{\pi}{p}\sin\left(u - \frac{\theta}{p} + \frac{\pi}{p}\right) + Q^2 \sin\frac{2\pi}{p}\sin 2\left(u - \frac{\theta}{p} + \frac{\pi}{p}\right)}{4\pi}.\end{aligned} \tag{19}$$

In order to compute the Fourier coefficient K_{mn}, we apply a linear shearing transform to the parallelogram bounded by $\theta = 0$, $\theta = 2\pi$, $u = \theta/p$ and $u = 2\pi + (\theta/p)$ in Fig. 4 into a square by introducing a new term ϕ

$$\Phi = u - \frac{\theta}{p}, \qquad 0 \le \theta; \quad u \le 2\pi. \tag{20}$$

We note that $d\Phi = du$ as θ and p are constants for a given line. In other words, the δC sampling contour is now placed along

$$\begin{aligned}\Omega(\theta, \phi) &= B + Q\cos\phi_1 + \frac{Q(\cos\phi_2 - \cos\phi_1)(2B + Q(\cos\phi_1 + \cos\phi_2))}{4\pi} \\ &= B + Q\cos\left(\left\lfloor \frac{\theta}{2\pi} \right\rfloor \frac{2\pi}{p}\right) - \frac{4BQ\sin\frac{\pi}{p}\sin\left(\left(\left\lfloor \frac{\theta}{2\pi} \right\rfloor \frac{2\pi}{p}\right) + \frac{\pi}{p}\right) + Q^2\sin\frac{2\pi}{p}\sin 2\left(\left\lfloor \frac{\theta}{2\pi} \right\rfloor \frac{2\pi}{p} + \frac{\pi}{p}\right)}{4\pi}\end{aligned} \tag{16}$$

$$\begin{aligned}K_{mn} &= \frac{1}{4\pi^2}\int_\Phi \int_\theta F(\theta, \Phi) e^{-j(m\theta + n(\Phi + (\frac{\theta}{p}))} d\theta\, d\Phi \\ &= \frac{1}{4\pi^2}\int_0^{2\pi} e^{-jn\Phi} \int_0^{(B + Q\cos\Phi - \frac{(4BQ\sin(\frac{\pi}{p})\sin(\Phi + (\frac{\pi}{p})) + Q^2\sin(\frac{2\pi}{p})\sin(2\Phi + (\frac{2\pi}{p}))}{4\pi})} H e^{-j(m + (\frac{n}{p}))\theta} d\theta\, d\Phi \\ &= \frac{jH}{4\left(m + \frac{n}{p}\right)\pi^2}\int_0^{2\pi} e^{-jn\Phi} \\ &\quad \cdot \left[\exp\left(-j\left(m + \frac{n}{p}\right)\left(B + Q\cos\Phi - \frac{4BQ\sin\frac{\pi}{p}\sin\left(\Phi + \frac{\pi}{p}\right) + Q^2\sin\frac{2\pi}{p}\sin\left(2\Phi + \frac{2\pi}{p}\right)}{4\pi}\right)\right) - 1\right] d\Phi \\ &= \frac{jH}{4\left(m + \frac{n}{p}\right)\pi^2}\left[e^{-j(m + (\frac{n}{p}))B}\int_0^{2\pi} e^{-jn\Phi}\exp\left(-j\left(m + \frac{n}{p}\right)\left(Q\cos\Phi - \frac{4BQ}{4\pi}\sin\frac{\pi}{p}\sin\left(\Phi + \frac{\pi}{p}\right)\right.\right.\right. \\ &\qquad \left.\left.\left. - \frac{Q^2}{4\pi}\sin\frac{2\pi}{p}\sin\left(2\Phi + \frac{2\pi}{p}\right)\right)\right) d\Phi - \int_0^{2\pi} e^{-jn\Phi} d\Phi\right] \\ &= \frac{jH}{4\left(m + \frac{n}{p}\right)\pi^2}\left[e^{-j(m + (\frac{n}{p}))B}\int_0^{2\pi}\left[e^{-jn\Phi}e^{-j(m + (\frac{n}{p}))Q\cos\Phi}\exp\left(j\left(m + \frac{n}{p}\right)\frac{BQ}{2\pi}\sin\frac{2\pi}{p}\sin\Phi\right)\right.\right. \\ &\qquad \cdot \exp\left(j\left(m + \frac{n}{p}\right)\frac{BQ}{\pi}\sin^2\frac{\pi}{p}\cos\Phi\right)\exp\left(j\left(m + \frac{n}{p}\right)\frac{Q^2}{8\pi}\sin\frac{4\pi}{p}\sin 2\Phi\right) \\ &\qquad \left.\left. \cdot \exp\left(j\left(m + \frac{n}{p}\right)\frac{Q^2}{4\pi}\sin^2\frac{2\pi}{p}\cos 2\Phi\right)\right] d\Phi - \int_0^{2\pi} e^{-jn\Phi} d\Phi\right]\end{aligned} \tag{22}$$

the θ-axis and the parallelogram is transformed into a square bounded by $\theta = 0$, $\theta = 2\pi$, $\phi = 0$ and $\phi = 2\pi$. This contour is

$$\Omega_T(\theta, \Phi) = B + Q\cos\Phi - \frac{4BQ\sin\frac{\pi}{p}\sin\left(\Phi+\frac{\pi}{p}\right)+Q^2\sin\frac{2\pi}{p}\sin\left(2\Phi+\frac{2\pi}{p}\right)}{4\pi}. \quad (21)$$

By substituting (10) and (21) into the Fourier coefficient equation [4], we can express the Fourier coefficient K_{mn} in the (θ, Φ) domain as shown in (22) at the bottom of the previous page.

Finally, we derive the double Fourier series expression for the δC single-sided trailing edge PWM sampling process based on (22) and is given in (12).

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