CONTRIBUTED PAPER

A Microtransceiver for UHF Proximity Links Including Mars Surface-to-Orbit Applications

Micro-transceivers, with digital and analog circuits integrated on the same chip, are small and light, for use in miniature robot scout vehicles.

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ABSTRACT | A low-volume low-mass low-power ultra-high-frequency radio transceiver for future planetary missions is described. The project targets a volume of less than 10 cm^3, mass of less than 50 grams, and power consumption of 50 mW on receive and 100 mW, 300 mW, or 3 W on transmit (for 10 mW, 100 mW, and 1 W output options). The transmitter design supports convolutionally coded binary phase-shift keying (BPSK), RC-BPSK, and quadrature phase-shift keying transmission from 1 to 256 kbps. Command/control instructions can be received at 2 or 8 kbps, with a sensitivity of better than −120 dBm. In addition to its low volume/mass/power features, temperature compensation to −100 °C and radiation tolerance to 100 krad allow operation outside of thermally controlled, shielded enclosures, further reducing the mass and complexity of exploration vehicles. The design is described in a top-down format, beginning with system requirements and proceeding through digital modem algorithm development, discussion of the silicon-on-sapphire CMOS process used and elaboration of key blocks in the radio-frequency (RF) integrated circuit design. Techniques to address coupling between high-sensitivity RF and on-chip digital circuits are also presented, and test results are given for prototypes of all major functions. Although designed for the Martian environment, the transceiver is expected to be useful in other proximity links where a small low-power radio compatible with Prox-1 space-link protocols is desired.

KEYWORDS | CMOS analog integrated circuits; CMOS integrated circuits; cryogenic electronics; digital radio; filters; integrated circuit design; integrated circuit noise; integrated circuits; integrated circuit testing; oscillator stability; space vehicle communication; space vehicle electronics; space vehicle telemetry; switching circuits; ultra-high-frequency (UHF) receivers; UHF transmitters

I. INTRODUCTION

For the past two decades, the development of radio-frequency (RF) integrated circuit (IC) technology has steadily improved, driven by market demand for cellular phones, wireless local-area networks, and other high-volume consumer products. With an RF-friendly IC fabrication process, it is now possible to integrate virtually an entire transceiver onto a single chip [1]–[5], yielding microtransceivers that are orders of magnitude smaller, lighter, and in some cases less power-hungry than classic board-level and module-based radio designs.

The implementation of such highly integrated radio designs, however, remains challenging. Difficulties include fundamental limitations of on-chip passives compared with their larger (and therefore higher Q) off-chip

Manuscript received January 22, 2007; revised March 30, 2007. This work was supported by the Mars Technology Program of the Jet Propulsion Laboratory, California Institute of Technology, under a Contract with the National Aeronautics and Space Administration.

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Digital Object Identifier: 10.1109/JPROC.2007.905092

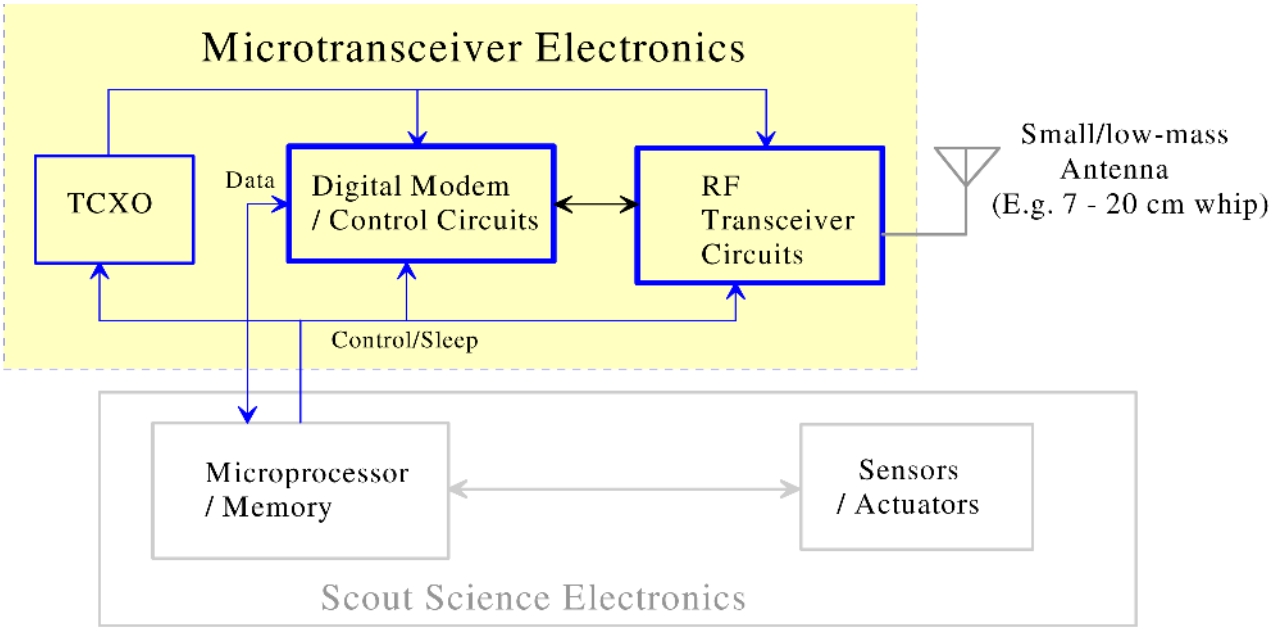


Fig. 1. *Top-level diagram of UHF microtransceiver and external interfaces.*

counterparts [6], [7] and electromagnetic compatibility of large-signal swings in digital circuits with microvolt/nanoamp analog and RF signals on the same die [8]. The latter problem in particular requires careful design at the system and circuit levels when sensitivity levels must reach −120 dBm or below.

This paper presents a top-down description of one such integration effort—implementing an ultra-high-frequency (UHF) microtransceiver for use on future robotic scout missions to the planet Mars. The transceiver, shown in simplified form in Fig. 1, operates in the 390–450 MHz band used by current Mars orbiter assets for relay of collected scientific data to earth. This paper presents both architectural and circuit level solutions to realizing the needed low-power high-sensitivity receiver circuits together with transmitter power amplifiers and digital synthesizer circuitry on the same integrated-circuit die. While digital circuits used in data formatting and digital intermediate frequency (IF) demodulation are currently implemented on a separate field-programmable gate array (FPGA) device for reprogrammability, the techniques developed allow these components to be brought together as well. In addition, the technologies discussed address design for wide temperature variations (e.g., to −100 °C) and for radiation environments to 100 k-rad total dose.

II. SYSTEM REQUIREMENTS

Robotic exploration of the surface of our sister planet began in the 1970s with the successful landing of the twin Viking science platforms carrying miniature chemical laboratories to search for signs of life [9]. The Pathfinder and Mars Exploration Rover (MER) missions continued this search with a new "follow-the-water" strategy in the 1990s and 2000s, supported by a fleet of orbiters designed to observe and photograph the planet from above and provide relay capability for rover-to-earth communications [10], [11]. During the coming decades, additional robotic missions will follow, continuing the search for water and life and laying the groundwork for eventual human explorers.

With increasing competition for funding and the desire to visit more sites on the planet, however, reductions in cost are becoming increasingly important. This fact translates directly to a need for reductions in mass, volume, and power of both the science instruments and the communications infrastructure on future probes. Existing UHF transceivers aboard the Spirit and Opportunity MERs measure as much as 2000 cm^3, have a mass of up to 2 kg, and consume as much as 45 W of power [12]. Combined with science, power generation/storage, and mechanical subsystems, the rovers themselves have a mass of 185 Kg and measure about 5 m^3, allowing only one rover per launch and limiting surface exploration of the planet to only two sites [13]. A microtransceiver measuring in the range of 10 cm^3 with a mass of 50 grams and operating at fractions of a watt would help enable the design of new types of Mars exploration craft ranging from aircraft and balloons to expendable dropoff probes and networked landers (Fig. 2). Hence, the primary system requirement for this project is reduction of mass, volume, and power by one to two orders of magnitude over existing communication assets.

Notwithstanding these goals, there are fundamental limits in the communications link, especially with respect to power reduction. Communication systems for Mars are

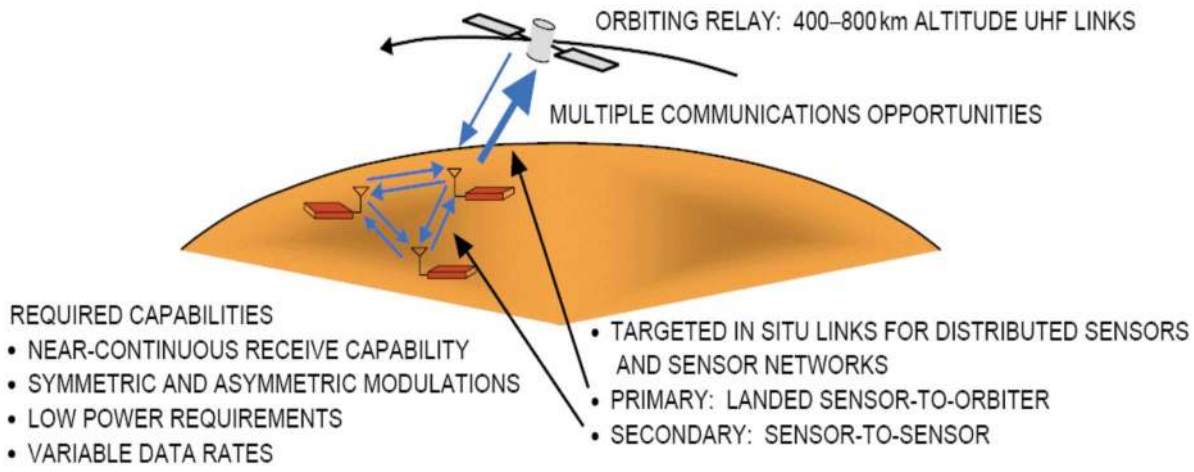


Fig. 2. ***Example Mars probe application and proximity communications link.***

constrained by the same link-budget issues as those on Earth, implying a theoretical minimum transmit power for the needed data-return volume and target data-transmission rates. Example calculations for probe-to-orbiter data rates that can be achieved on low power are shown in Fig. 3 [14], [15]. For a direct overhead orbital pass (and suitable antenna orientations), this graph shows that rates on the order of 10 kbps can be achieved at 100 mW power levels for typical orbiter altitudes of 400 km. This translates to rates of 100 kbps at 1 W. In general, orbital passes will last only about 15 min and involve larger slant ranges, so that somewhat lower average rates can be expected.

Estimating total data volume return is more difficult since it requires predictions of orbital pass geometries, antenna patterns, and details of link operation (e.g., fixed rate per pass versus variable rate, and packet overhead). As a benchmark, the Spirit and Opportunity MERs averaged more than 150 Mbits of return data per sol (Martian day) at a fixed 128-kbps rate through the UHF proximity links to the Odyssey and MGS orbiters on 12 W of RF output power [12], [16]. Assuming similar implementation margins, this translates to approximately 12.5 Mb/sol if transmit power is reduced to 1 W and 1.25 Mb/sol if 100 mW is used. Such volumes are sufficient for scout missions that are not photograph-intensive. To provide for mission tradeoffs between data volume and battery capacity (and hence vehicle mass/volume), the microtransceiver is designed to operate at either of these levels, plus a 10-mW level for local links between networked platforms.

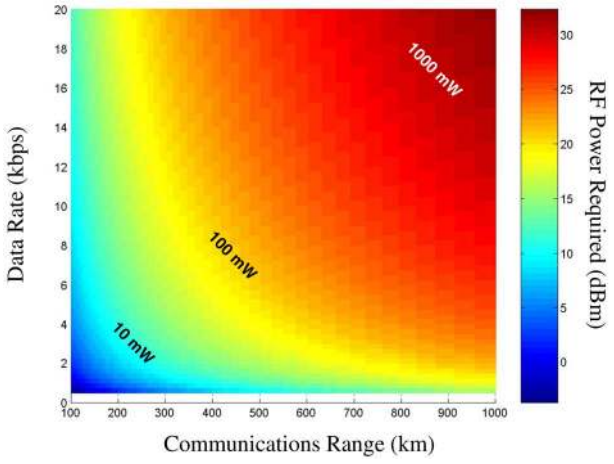


Fig. 3. ***Contour plot of probe-to-orbiter data rate versus slant range and required RF transmit power.***

On receive, data-rate requirements are considerably lower but must be carefully considered to provide reliable communication of command and control from the orbiter. As in the transmit case, the modulation used here is binary phase-shift keying (BPSK) for good energy efficiency. However, to reduce power consumption and die size for the receiver circuits, the microtransceiver is designed for use with no forward error correction coding and relies instead on error-detection and go-back-N repeat-request protocols specified in the CCSDS Proximity-1 space link protocol [17]. Hence, approximately 14-dB Eb/No is required for reliable reception of command and control data, assuming a 3-dB implementation margin and a bit error-rate goal of $< 10^{-6}$. At an 8-kbps rate, this implies the need for a -118 dBm receive power, assuming the microtransceiver system noise temperature requirement is set at 600 K. Comparing this with the received power measurements from the Odyssey orbiter to MER-B (Opportunity) shown in Fig. 4, > 5 dB of link margin will be provided at this rate for the majority of the orbital pass. To provide for even higher margins, a fallback rate of 2 kbps is also provided as discussed in Section IV.

Beyond these basic link-closure considerations, several additional requirements must be met by the microtransceiver. Due to the planet's sparse atmosphere, there is

little protection from solar radiation, so that radiation tolerance must be provided. Meeting this requirement is helped by the rad-hard silicon-on-sapphire (SOS) process employed but must still be considered in selection of items such as the commercial off-the-shelf (COTS) temperature-compensated crystal oscillator (TCXO) shown in Fig. 1. Secondly, since the main goals are reduction in size, mass, and power, it is desired to allow the transceiver to operate outside of the typical "warm box" used on most spaceflight hardware. Whereas warm-box temperatures can be maintained at −50 °C and above, nighttime lows on Mars can fall to −100 °C or below. This resulted in the need for early studies of the IC process variation at cryogenic temperatures and of the variations in frequency of the TCXO and a COTS IF filter used in the radio-frequency IC (RFIC) architecture [18]. These issues are addressed by the architectures of the RFIC and the digital demodulation subsystems described in Sections III and IV. Target specifications for the microtransceiver derived in this section and Section III below are summarized in Table 1.

Table 1 Target Specifications for Microtransceiver

Parameter	*Value (typ)*	*Units*
Environment		
Operating Temperature	-100 to +25	Celsius
Radiation tolerance (total dose)	100	krad
Operating Frequency		
Transmit	390 – 410	MHz
Receive	430 - 450	MHz
Tuning step size	< 100	kHz
TX frequency accuracy		
-40 to +50C	< 10	ppm
-100 to -40C	< 150	ppm
Link Protocols	Prox-1 subset (see text)	
Modulation formats		
Transmit (convolutionally coded)	BPSK / RC-BPSK / QPSK	
Receive (CRC error detection)	BPSK	
Transmit bit rate	1 to 256	ksps
Receive symbol rate	2 and 8	kbps
Receive sensitivity (2 kbps)	< -120	dBm
Power Supply Voltage	3.3	Volts
Power Consumption		
Transmit (10mW out)	100	mW
Transmit (100 mW out)	300	mW
Transmit (1 W out)	3	W
Receive (100% duty cycle)	50	mW
Size		
4-layer PCB version	3 x 3 x 1	cm^3
Metal-case version	3.5 x 3.5 x 1.5	
Mass		
4-layer PCB version	10	grams
Metal-case version	50	

III. RFIC TRANSCEIVER ARCHITECTURE

Translating system-level requirements into a fully integrated hardware implementation requires careful consideration of circuit design options and IC process capabilities. The former is the subject of over 20 years of ongoing research in RFIC design and is covered in papers on topics ranging from the improvement of on-chip passives [7] to the design and optimization of subcircuits [19] to the design of complete radios for selected applications [1]–[5]. Several excellent review articles have also been written on these subjects [20]–[22]. Capabilities of an IC process are generally covered in proprietary vendor data but are sometimes reviewed in papers for select cases and applications. Details relevant to the target silicon-on-sapphire (SOS) process are covered in Section V of this paper.

In the following sections, knowledge from these sources is applied to develop the top-level diagram of Fig. 5 and the overall RFIC architecture shown in Fig. 6. Since this application is somewhat unique, we will periodically step back and review radio system performance issues as a whole to derive practical requirements for the circuit design. This is a luxury not often encountered in the highly regulated industry of cellular telephones but one worth considering by designers of special purpose products, where the goal is high integration.

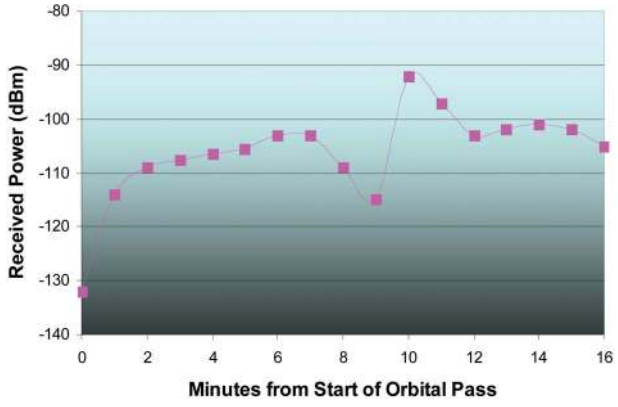


Fig. 4. *Power levels received from Odyssey orbiter by the Mars Exploration Rover during sol 104 p.m. as reported in [16].*

A. Top-Level Diagram

A top-level block diagram of the microtransceiver showing partitioning of functions to ICs is provided in Fig. 5. To manage development cost and risk, the implementation is divided into two primary integrated circuits, an RFIC and a digital IC, plus an optional third IC for the 1-W output option. All are implemented in silicon-on-sapphire so that they can ultimately be integrated into a single die. Also included are a commercial TCXO and 10.7-MHz ceramic IF filter, together with a small collection of surface mount passives (not shown) providing required supply bypassing and optional antenna impedance-matching functions. A 19.2-MHz TCXO frequency was selected to be compatible with commercial offerings, to prevent harmonics of the main system clock

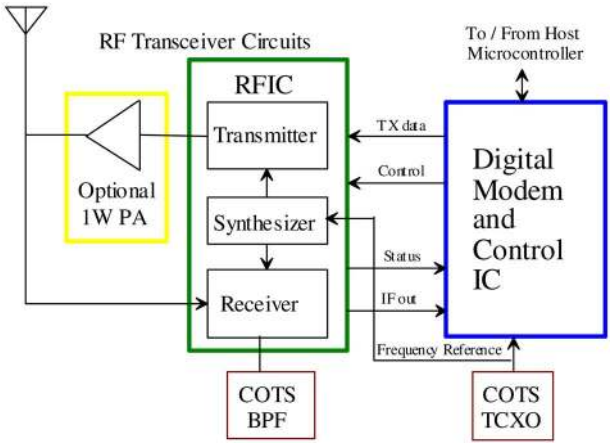


Fig. 5. *Top-level structural breakdown of microtransceiver.*

from falling close to a desired CCSDS receive channel or image frequency, and to allow integer division to data clock rates that conform to Prox-1 standards up to 256 kbps.

A time-division duplex (TDD) mode of operation is adopted to obviate the need for integration-averse duplex filters and to allow a single synthesizer to be shared between transmit and receive modes. TDD operation also allows the use of inductors within both the low-noise amplifier (LNA) and the power-amplifier (PA) circuits on the same die to meet the integration goals and performance requirements.

B. RFIC Block Diagram

The RFIC architecture is elaborated in Fig. 6. The upper half consists of a 100-mW direct-modulation transmitter with options for BPSK, 45° residual-carrier BPSK, quadrature phase-shift keying, and frequency-shift keying (FSK)

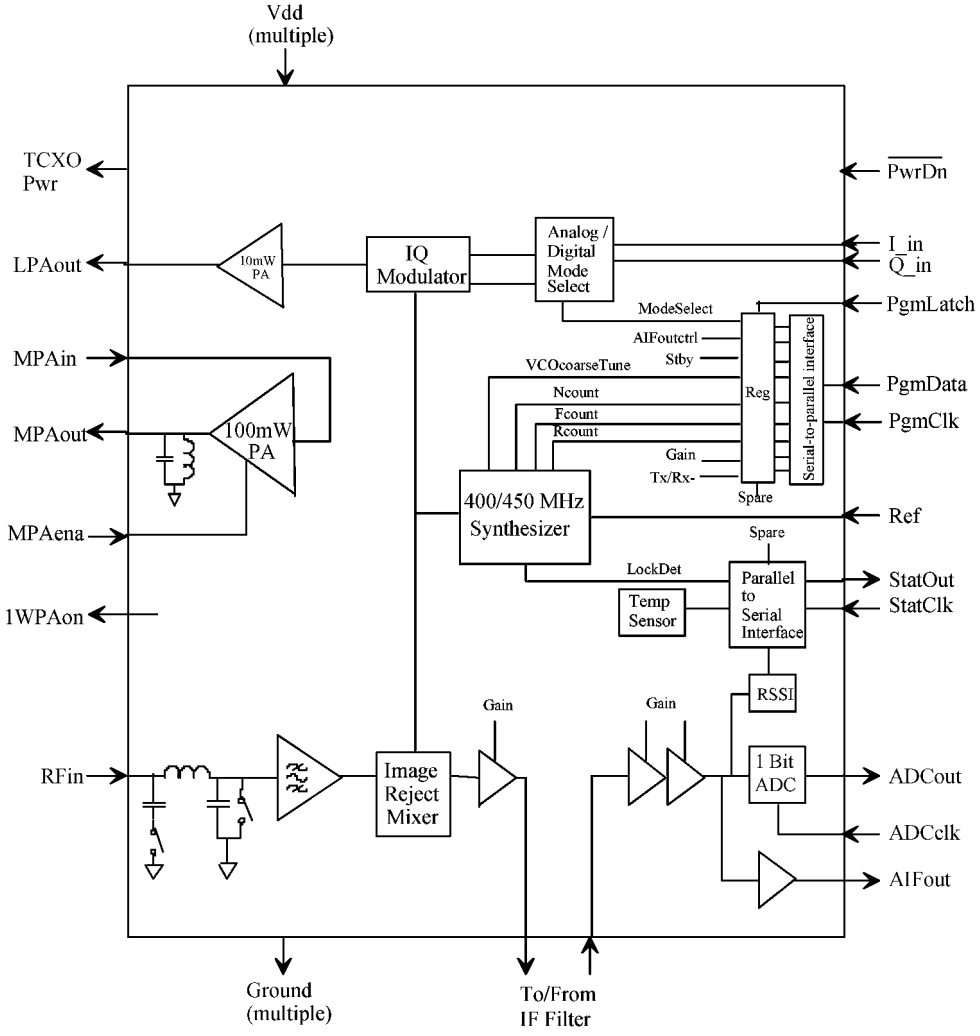


Fig. 6. *RFIC block diagram.*

(using externally generated analog IQ waveforms). The lower half is a classic superheterodyne receiver with off-chip IF filter and 1-bit oversampled analog-to-digital conversion. This combination was selected over a zero-IF or sampling design due to the need to process low-data-rate BPSK modulations at < -120 dBm sensitivity levels in a CMOS process where $1/f$ noise can extend to the megahertz range.

While narrow-band on-chip front-end selectivity can theoretically be achieved with Q-enhanced filtering in superhet receivers to provide good image rejection [24], the use of such filtering was avoided in this design to reduce development risk and to optimize noise-figure performance. Instead, a simple image-reject mixer was implemented to provide the necessary rejection of LNA output noise at the image-frequency.

No explicit transmit–receive (TR) switch is shown since the TR function is built into the LNA and PA circuits, allowing the PA output to be connected directly to the LNA input pin in an application circuit [23]. During receive, the parallel LC tank at the PA output provides a reflective termination, steering received signal power to the LNA. During transmit, the two switches in the LNA are closed to provide a reflective termination at the LNA input. This technique maximizes transmit power efficiency by holding losses to approximately 0.2 dB while noise figure degradation in receive mode is held to approximately 1 dB with virtually no additional IC die area consumption.

C. Transmit-Mode Operation

During transmit mode, the most important circuit-level performance parameter is arguably the efficiency in the power amplifier circuits, which consume the bulk of the transceiver current. At 1-W output, the transceiver will consume > 2 W of power if the PA efficiency is 50% and 3.3 W if the efficiency is 30%. To meet the system goal of reducing power consumption by at least one order of magnitude from existing 45 W levels on the MER's UHF radios, a 30% efficiency is therefore an appropriate lower bound and was specified for the project. Fortunately, integrated amplifiers published over the past several years have achieved this level or better at L- and S-band frequencies (e.g., [25]), suggesting that the specification was achievable even when accounting for decreased inductor Q as designs are adapted to the lower frequency 400-MHz range. The design of the 30% efficiency, 100 mW, and 1-W class-D switching-mode UHF PAs is overviewed in [26] and discussed in Section VI.

Additional transmitter specifications include harmonic and spurious emission levels, synthesizer frequency accuracy and step size, and phase-noise impacts on the BPSK modulation's constellation and hence link performance. Fortunately many of these requirements are less stringent on Mars than in terrestrial environments so that appropriate tradeoffs are possible to further the primary goal of minimizing mass/volume/power.

For example, harmonic emission is not regulated when operating outside earth orbit so that size, weight, and circuit losses associated with harmonic filters at the PA output can be avoided. The 10 mW transmit option outputs a smoothed squarewave with approximately -15 dBc third-harmonic levels, while the 100 mW and 1 W modes use LC tanks in their outputs to achieve good efficiency with > 20 dB of harmonic suppression.

D. Frequency Synthesis

The synthesizer design elaborated in Fig. 7 uses a divided version of the 19.2-MHz TCXO reference to generate accurate frequencies when operating at temperatures of -40 °C and above.

At lower temperatures, the TCXO can drift substantially as shown in Fig. 8. Measured frequency shifts of -140 ppm from -40 to -100 °C in the TCXO translate to -60 kHz at the 435 MHz receive frequency [18] requiring reasonably wide IF prefiltering and additional frequency acquisition tolerance and filtering in the receiver's digital demodulator.

In the transmitter, these shifts must be tracked out by the orbiter. Fortunately, newer Mars orbiter platforms carry relatively high performance reprogrammable radios such as Electra [15] allowing for such tolerances in the microtransceiver's synthesized output frequency. In the receiver, the 60-kHz shift was found to approximately track the IF filter's center frequency as shown in Fig. 9. Hence high-side injection was adopted to keep the IF signal centered in the filter's passband.

The voltage-controlled oscillator (VCO) of Fig. 7 operates at twice the RF output frequency to provide for accurate differential quadrature outputs for IQ modulation on transmit and image-reject mixing on receive. This choice also substantially reduces potential VCO pulling from the on-chip PA inductors during transmit and dc offset concerns in the mixing operation due to pickup by the LNA inductors during receive. Since the transmit and receive frequencies are widely separated (400 versus 435 MHz), a coarse-tuning control is provided to pretune to one of 16 ranges. This relaxes the requirements for on-chip varactors and keeps the VCO sensitivity low for better suppression of noise and crosstalk from on-chip and off-chip digital signals. To provide for a loop bandwidth sufficient to address megahertz range $1/f$ noise in the on-chip CMOS VCO's phase noise spectrum, a fractional-N architecture is implemented. Using a 4.8-MHz divided reference and 10-bit fractional-count accumulators, the synthesizer achieves a tuning step-size of $4.8\ \text{MHz}/1024 = 4.7$ kHz.

E. Receive-Mode Operation

Receiver design is a balance of sensitivity, interference rejection, power consumption, and a host of selectivity and stability concerns. In this project, the RF interference environment is relatively benign so that small signal

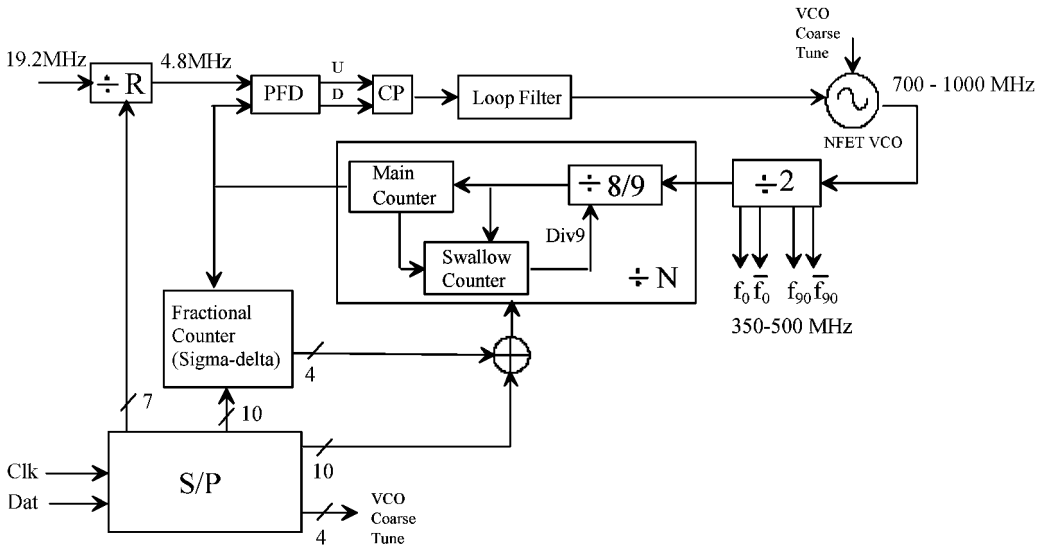


Fig. 7. ***Fractional-N synthesizer simplified block diagram.***

performance (e.g., noise figure) and overall power consumption outweigh large signal requirements (e.g., compression and third-order intercept point). Hence, front-end selectivity and compression point requirements are relaxed and traded off against the integration low-power and sensitivity goals.

In place of the typical preselect filter preceding the LNA, the TR-switch/matching-network provides modest selectivity. In receive mode, the switches of Fig. 6 are in the open position, forming an L-type matching network with a selectivity Q of approximately two, yielding a bandwidth of approximately 200 MHz. At the same

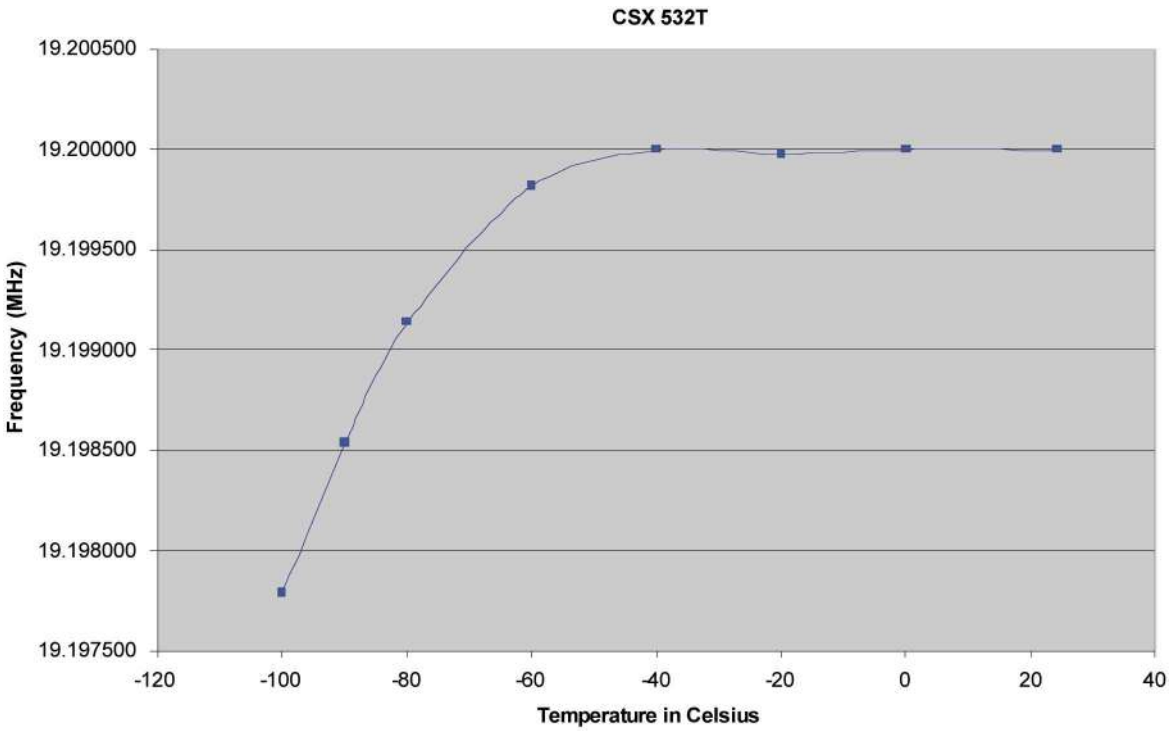


Fig. 8. ***Measured frequency drift of 19.2-MHz TCXO from −100 to +20 °C with 500-Hz per division vertical scale.***

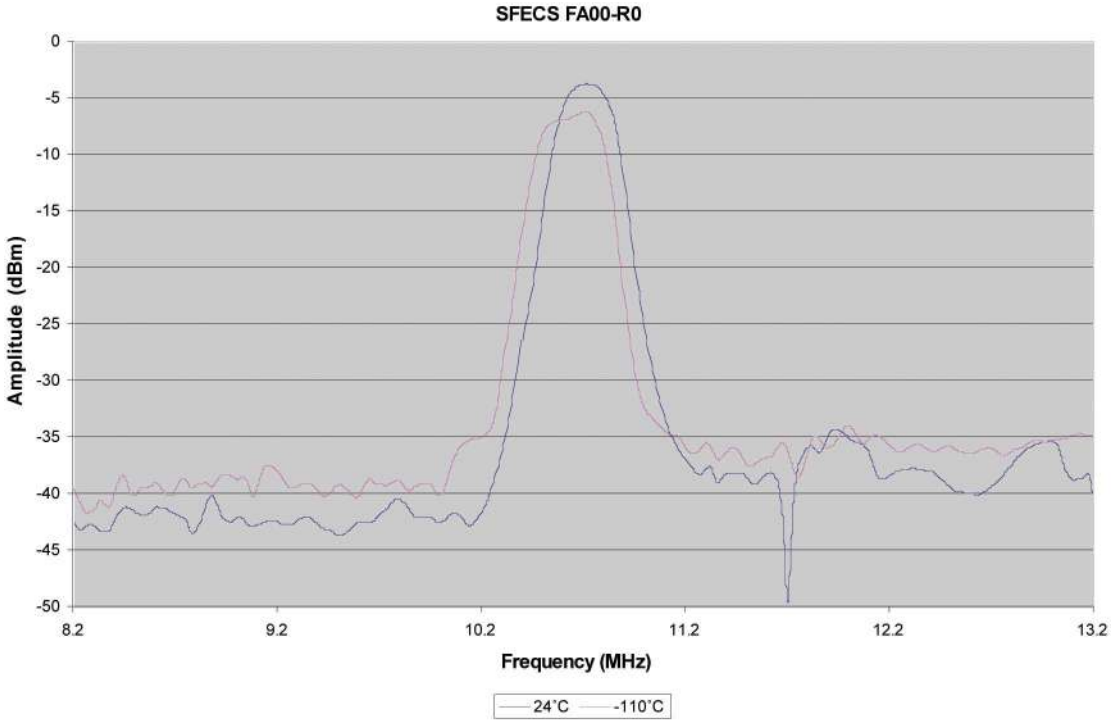


Fig. 9. *Measured frequency shift of IF filter from room temperature (blue) to −110 °C (red).*

time, it provides the required input match (impedance and voltage stepup of 10 and 3.2, respectively) to optimize noise figure performance. Additional selectivity is implemented in the tuned-RF LNA output tank, narrowing the bandwidth to approximately 80 MHz.

Downconversion to the relatively low 10.7 MHz in receive mode is implemented with an image-reject (IR) mixer with approximately 20 dB rejection to hold noise figure degradation from image frequency noise to < 0.1 dB. Following approximately 40 dB of voltage gain in the LNA and 25 dB in the mixer, the subsequent IF chain provides an additional 60 dB of gain prior to analog-to-digital conversion.

F. IF Filtering and 1-bit A-to-D Conversion

The off-chip IF filter in the center of the IF chain of Fig. 6 offers a relatively wide 250-kHz bandwidth to allow for Doppler shifts, TCXO aging, and drift at low temperature and a 35-dB out-of-band attenuation to provide a sufficient signal-to-noise ratio to allow 1-bit analog-to-digital conversion (ADC). Combined with inherent selectivity in the postfilter IF amplifiers and oversampling in the 1-bit ADC (relative to 8-kHz signal bandwidth), these parameters are sufficient to allow good digitization fidelity. To illustrate this point, Fig. 10 shows a representative IF filter output spectrum at a −118 dBm receiver RF input assuming a 600-K system noise temperature T and an 8-kHz resolution bandwidth.

The total noise power at the filter output is

$$P_{\text{noise}} = GkTB_{\text{Nfilt}} + GkTB_{\text{Namp}}(10^{-35/10}) \qquad (1)$$

where k is Boltzmann's constant, B_{Nfilt} and B_{Namp} are the IF filter's noise bandwidth and the noise bandwidth of the post-IF amplifiers, and G is the gain in decibels from the RF input to the filter output. With the given parameters, this results in a noise power of $-117 + G$ dBm and

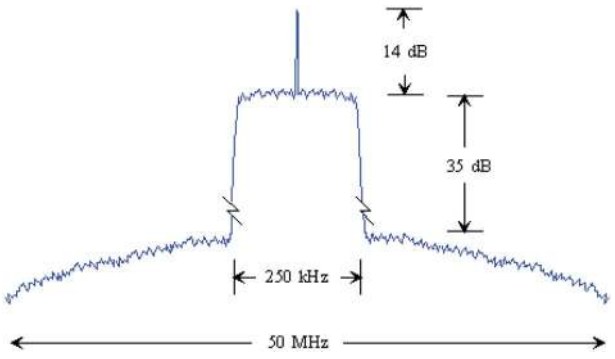


Fig. 10. *Typical spectrum at ADC input shown with signal at receiver sensitivity level.*

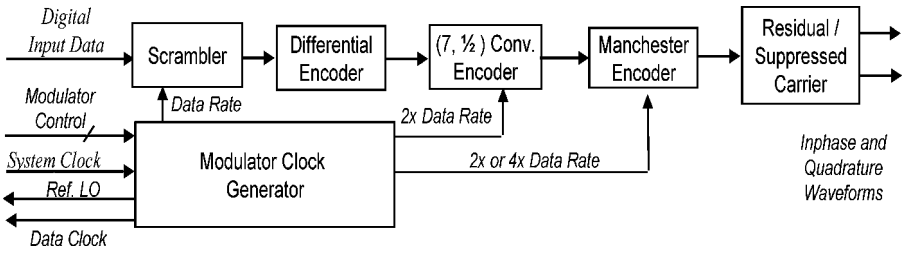


Fig. 11. ***Digital transmitter functions.***

therefore a −1 dB signal-to-noise ratio into the 1-bit ADC. However, 450 times oversampling followed by subsequent digital matched filtering to the 8-kbps datastream provides a 26-dB ADC dynamic range improvement over a simple 1-bit digitization [27] so that the full 14-dB SNR is maintained (to within 0.3 dB).

IV. DIGITAL MODEM DESIGN

The development philosophy of the digital modem is based upon several objectives that require continuous design iteration as the different radio subsystems evolve and their actual performance is measured. These objectives include:

- accepting "reasonable" performance degradation in trade for lowered complexity;
- compensating for signal impairments to prevent overdesign in the RFIC;
- minimizing digital logic and sampling rates for reduced power consumption and die area.

A. Digital Transmitter

The digital transmitter provides basic compatibility with physical layer interfaces supported by Mars in-situ telecommunications assets. Functional aspects of the data formatting are outlined in the transmitter block diagram of Fig. 11. Each element can be individually enabled based upon user needs. Infrastructure compatible data rates range from 1 to 256 kbps in powers of two.

The digital transmitter generates bit-level in-phase and quadrature baseband outputs that interface directly to the RFIC as shown on the right-hand side of Fig. 5. CMOS logic levels are shifted within the complex modulator circuitry of the RFIC to provide a bi-polar waveform for RF modulation. Selection of residual carrier is achieved by simply holding one of the baseband outputs constant and allowing the remaining quadrature output to modulate the carrier. While this results in a 45° modulation index (as opposed to the 60° specified in [17]), the only impact is a slight reduction in transmitter power allocated to the data. Fully suppressed carrier BPSK signaling is achieved by modulating the in-phase and quadrature outputs with identical bits.

B. Digital Receiver

In contrast to the transmitter, our desire to limit the receiver design complexity results in a series of design optimization challenges. Fig. 12 details one of many possible decompositions of the basic receiver processing functions shown as a series of sequential steps. Within each of these steps, algorithms and attendant parameters require definition. In the IF downconversion step, the 1-bit samples from the receiver RFIC are mixed, noncoherently to a nominal baseband, assuming a signal input centered exactly at the 10.7-MHz IF. The coarse frequency correction step performs estimation and compensation of anticipated gross offsets induced by a combination of Doppler and reference oscillator drift due to temperature. The level of correction needed is a reduction in residual offset that is a small fraction of the received data rate. This correction is followed by noncoherent symbol synchronization and matched filtering. The final receiver processing stage then performs carrier phase synchronization and data detection on the outputs of the matched filter. As a matter of efficiency, the design reflects a multirate architecture in which the processing rate is reduced as the signal proceeds through each stage.

In Fig. 13, a block diagram elaboration of the bandpass sampling and frequency correction stages are shown.

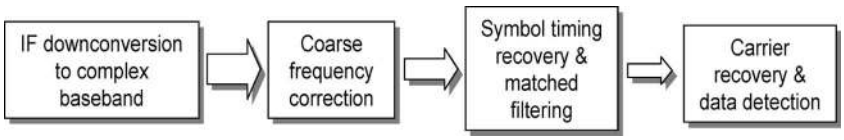


Fig. 12. ***Receiver processing steps.***

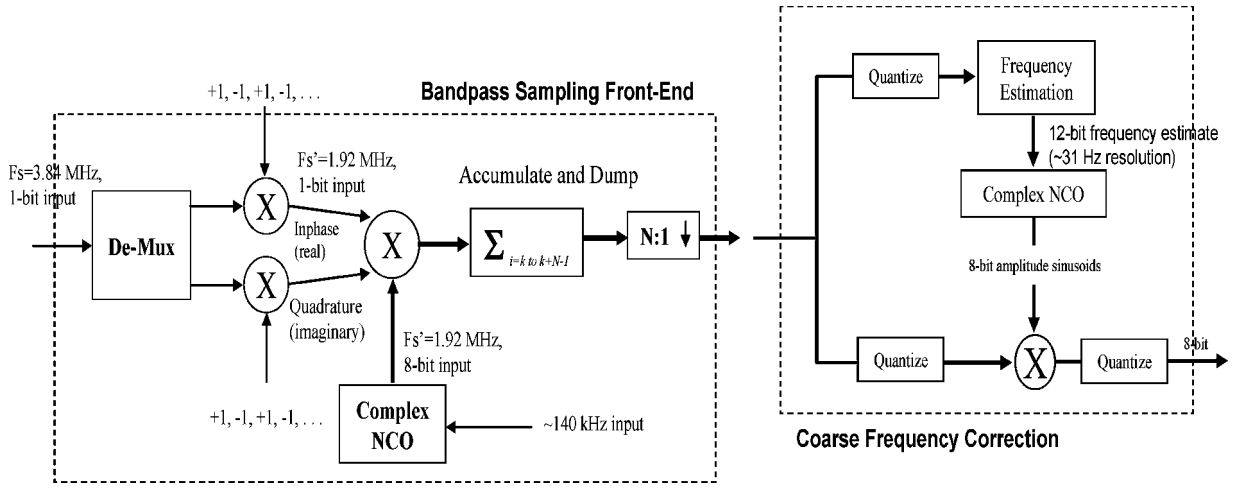


Fig. 13. ***Digital front-end diagram.***

Note the addition of a numerically controlled oscillator (NCO) after the classical quadrature sample demultiplexer. This correction element is required as all digital sampling rate choices based upon an integer submultiple of the 19.2-MHz reference oscillator do not exactly downconvert the 10.7-MHz IF to baseband.

The selection of a bandpass sampling rate can be aided by the type of analysis summarized in Fig. 14. For each choice in sampling frequency, the range of the baseband digital spectrum is shown in relation to the analog bandpass spectrum of the IF filter. An appropriate design choice attempts to minimize the sample rate while insuring that the analog bandpass response is closely centered within the digital spectrum. Choices below 3.2 MHz are unsuitable as the full extent of the analog bandwidth is not completely spanned. Of the next

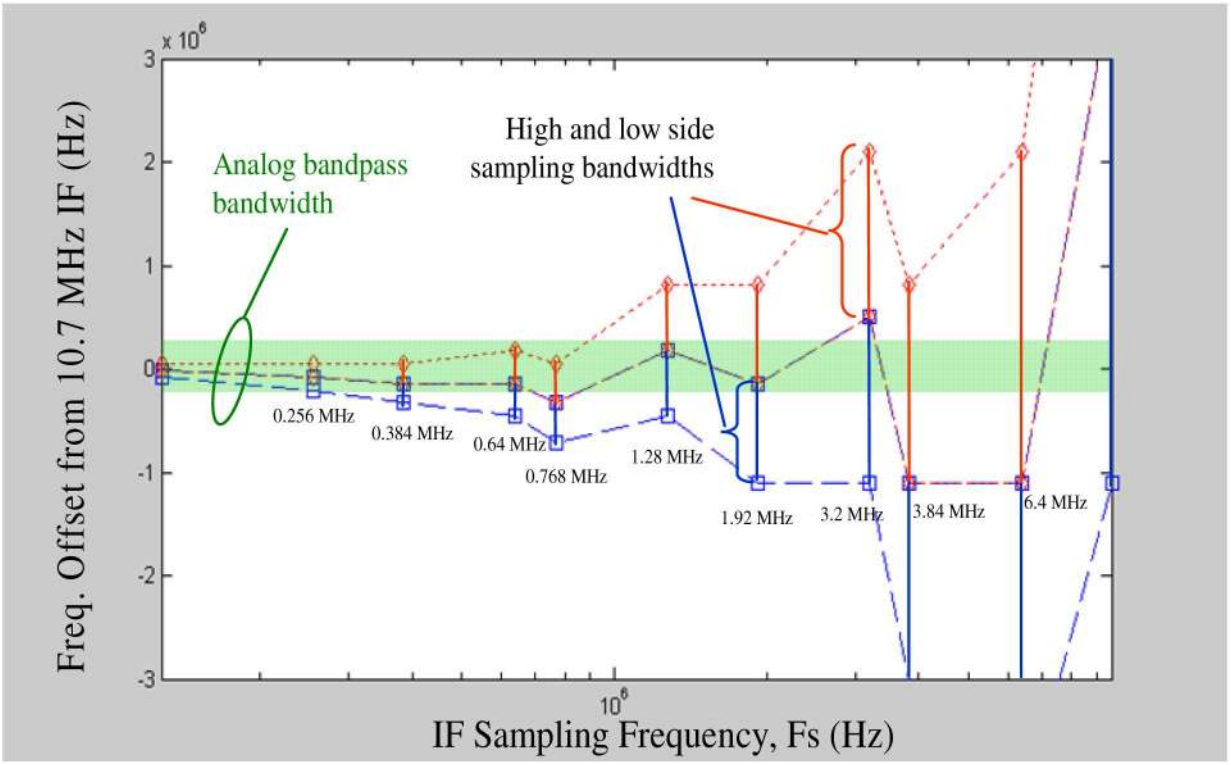


Fig. 14. ***Bandpass sampling options.***

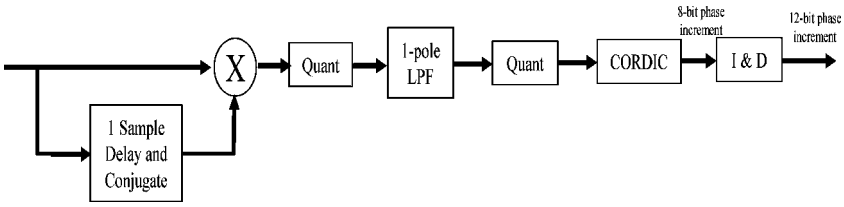


Fig. 15. ***Frequency estimator diagram.***

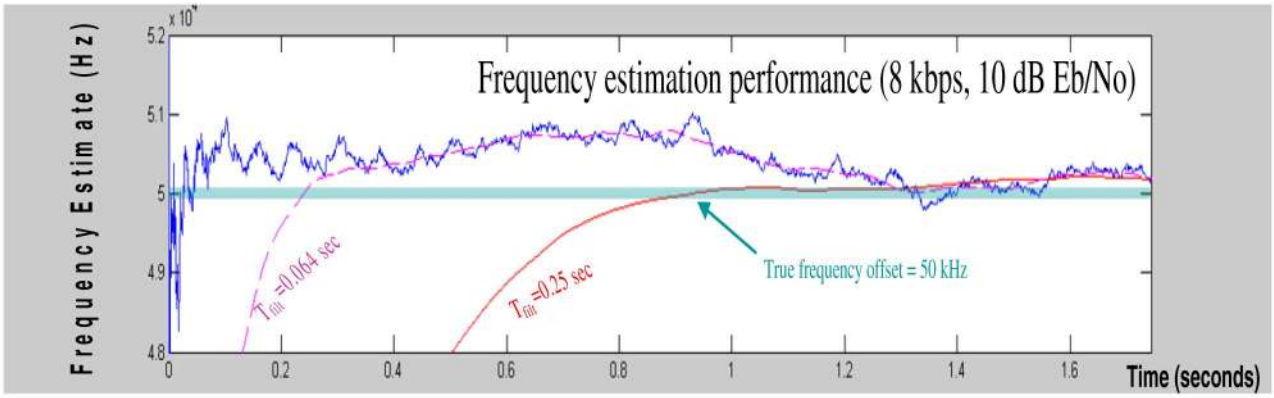


Fig. 16. ***Example frequency estimator performance.***

two possibilities, the 3.84-MHz choice exhibits better centering of the bandpass spectra, represents a negligible addition in overall power consumption compared to 3.2 MHz, and so is therefore chosen as the baseline IF sample rate.

As shown in Fig. 13, the coarse frequency correction stage utilizes a second NCO that is driven by a frequency estimation algorithm. During the receiver development, a number of estimators were conceived, simulated, and implemented in Verilog hardware description language. Designs were evaluated both for performance and complexity (as measured in required logic). One promising fast Fourier transform based estimator was discarded due to design size. Figs. 15 and 16, respectively, describe the estimator algorithm and one example of its dynamic performance in response to a step function frequency offset of 50 kHz. Depending upon the time constant of the smoothing filter, the residual frequency error can be controlled to a level that is $< 10\%$ of the data rate, thereby allowing the baud rate carrier recovery stage to perform coherent detection.

The noncoherent symbol timing recovery is based upon a power type measurement of the matched filter output that is conditioned against different time offsets of the baud phase. The decision statistics are noncoherently averaged over multiple symbols and the maximum hypothesis is selected. In Fig. 17, the impact of different finite symbol time resolutions is shown. Note that the 1-bit ADC input will add an additional degradation of roughly 2–2.5 dB in bit error rate (BER) performance.

The carrier recovery circuit is based upon a standard second-order digital phase-locked loop that operates on the baud sampled outputs of the matched filter. Rules for setting loop parameters are described in [28].

V. SILICON-ON-SAPPHIRE IC PROCESS

The 0.5-μm version of Peregrine Semiconductor's silicon-on-sapphire UltraCMOS process was chosen for its RF integration capabilities, good breakdown voltage handling, and radiation tolerance. The process is a fully depleted CMOS technology made in a 100-nm-thick silicon film on sapphire. The combination of the thin silicon layer and the insulating sapphire substrate results in complete dielectric isolation of devices. This is well suited for high levels of RF and digital integration with minimal mutual interference. The process cross-section is shown in Fig. 18, along with the cross-section of a bulk CMOS process.

The insulating sapphire substrate reduces capacitances, which means the devices run faster and with lower power. One indication is $f_{\max}$, the maximum frequency of oscillation [29]. It is three times higher than the unity-current-gain frequency f_t in this process,

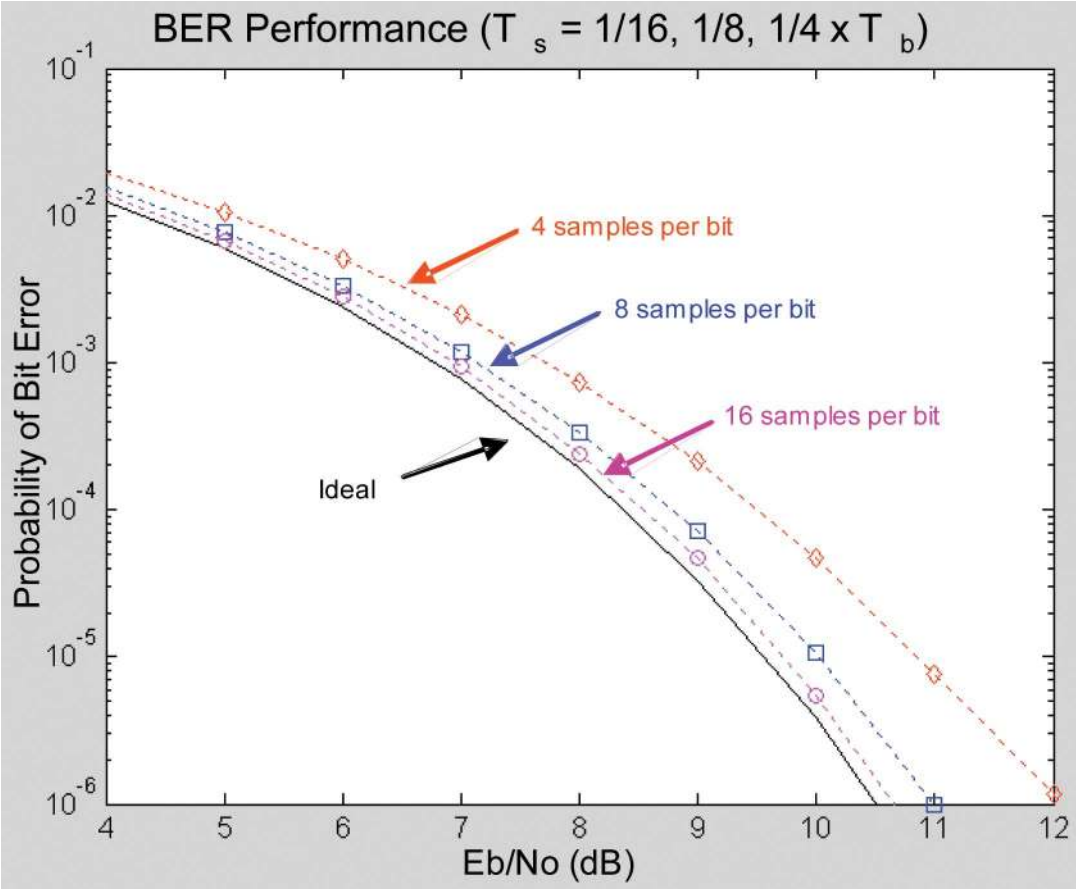


Fig. 17. ***BER performance with different timing resolution in the baud synchronizer.***

compared with $f_{\max}$ approximately equal to f_t in a standard bulk CMOS process. The $f_{\max}$ is 43 GHz in the 0.5-μm process used in this project and 100 GHz in the 0.25-μm process. The devices are fully depleted, thus avoiding common silicon-on-insulator issues such as memory effects. Additionally, the fully depleted devices act as a nearly ideal three-terminal device simplifying and compacting circuit designs. Three threshold voltages are available for NMOS and PMOS devices—an intrinsic threshold voltage device (0 V), a low threshold voltage device (0.2 V), and a standard threshold voltage (0.8 V) device. The intrinsic devices have no channel dopant and are the fastest, highest transconductance (gm) devices. These features are used in the RFIC design to allow stacking of multiple devices for cascoding purposes on the relatively low 3.3-V supply.

Passive devices in the process also take advantage of the insulating substrate. The inductors are not impaired by substrate currents, and the quality factor is limited only by the metal. Additionally, due to the low substrate capacitance, the inductors can be made large to achieve high Q without penalty to the self-resonant frequency. This project was built in the three metal process, featuring a 3-μm-thick top layer of aluminum metallization and also metal–insulator–metal (MIM) capacitors. Inductor Qs of > 40 have been achieved in this process at gigahertz frequencies, while Qs of > 10 are possible at UHF in moderate die areas [30], [31].

High levels of integration without common crosstalk issues are enabled by the sapphire substrate. Additionally, the passive devices do not have voltage coefficients. In a conventional semiconducting bulk CMOS substrate, even with isolation wells, shallow and deep trench isolation walls, and substrate contacts, circuit performance suffers from substrate currents. This can result in digital and phase-locked loop noise coupling into the sensitive receiver and synthesizer VCO circuits, especially in a system such as this where the received signal levels may be at or below -120 dBm. Even the use of large structures such as large MIM capacitors and inductors can create added coupling between RF circuits in a bulk CMOS process. The isolation of the circuits and devices in SOS is limited instead mainly by bondwire coupling and magnetic fields from inductors—issues that can be addressed by techniques discussed in Section VI.

Finally, the thin silicon layer on the sapphire substrate produces an inherently radiation hardened process [32]. The process shows excellent tolerance to ionizing

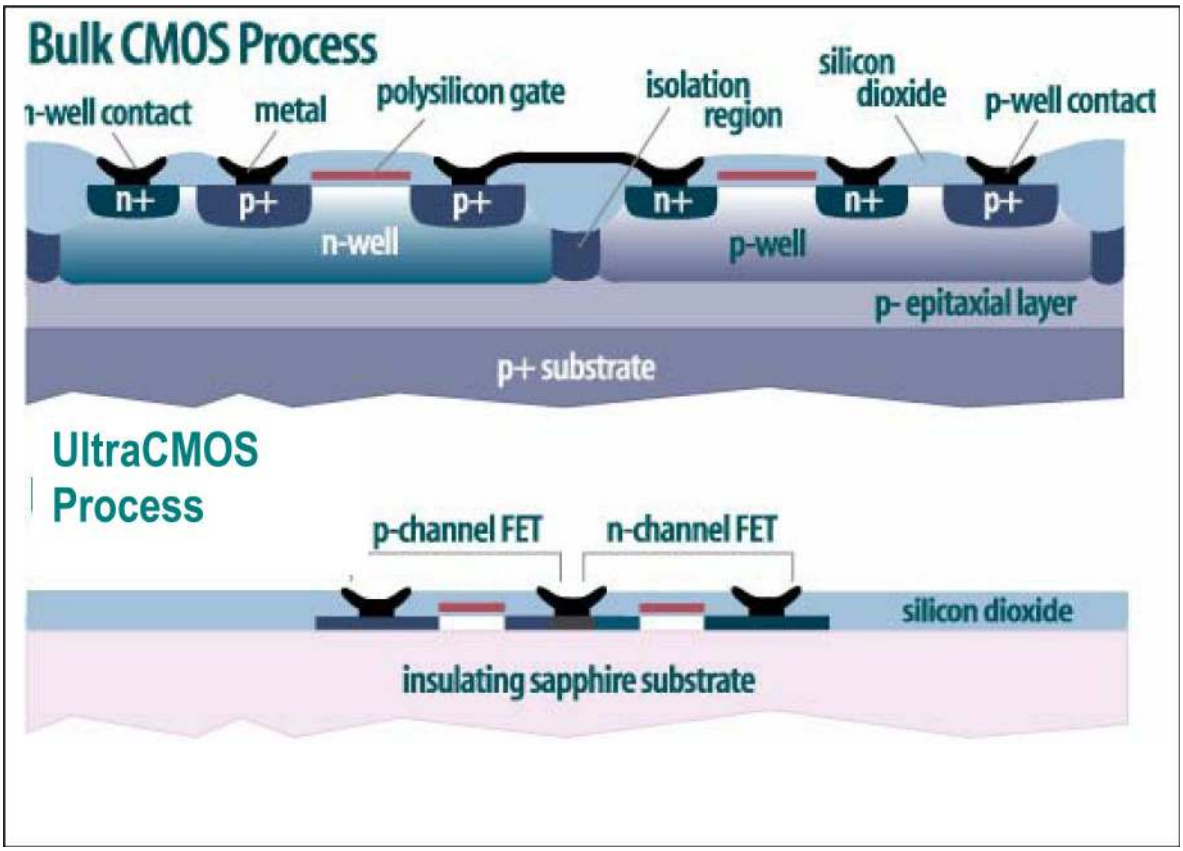


Fig. 18. *Cross-sectional view of (top) bulk Si CMOS and (bottom) UltraCMOS.*

radiation up to 100 krad (Si) levels. There is no possibility of single event latchup, and single-event error rates are less than 1e-9 errors/bit-day. Parametric shifting of the devices is minimal in a total dose environment, with threshold voltages and leakage being the most affected parameters. Threshold shifts are limited to approximately 50 mV for high-threshold devices and 250 mV for zero-threshold devices. These shifts and leakage currents are easily handled by careful biasing in RFIC implementations.

VI. RFIC CIRCUIT DESIGN AND MEASURED PERFORMANCE

Implementing an integrated transceiver in hardware involves detailed circuit-level design and simulation, IC and PC board layout, extensive testing, and iteration as needed to achieve acceptable performance. For space reasons, we present only a sampling of circuits developed during the design, leaving the majority of the discussion to issues that are less documented in the literature. These issues include guaranteeing stability, achieving compatibility between analog and digital circuits, and iterative testing and refinement. Some of the test results presented will include problems encountered along the way to illuminate engineering processes and solutions that too often go unreported in traditional presentations, or at best are found in footnotes of scattered references.

A. Iterative Prototyping of RFIC Circuits

While most digital IC design is now carried out through high-level hardware description languages and then automatically reduced to IC form with place-and-route software, analog and RF design and layout remain largely manual endeavors. With careful design, simulation, and layout-versus-schematic checks, basic performance can be checked and any errors in manual RFIC layouts can be caught before fabrication, but modeling of parasitics present in the fabricated physical circuits remain problematic. On-chip parasitics that may be difficult to model accurately include line-to-line and line-to-substrate layout capacitances not present at the schematic level (some of which are estimated by layout circuit-extraction tools), coupling between circuits (electric, magnetic, and through vdd and ground trace resistances), and resistances in transistor gates and passive elements (especially inductors) that complicate estimating tank-circuit Q. These limitations on modeling generally lead to the need for iterative prototyping to achieve optimal performance. Above the chip level, bondwire parasitics and the signal crosstalk

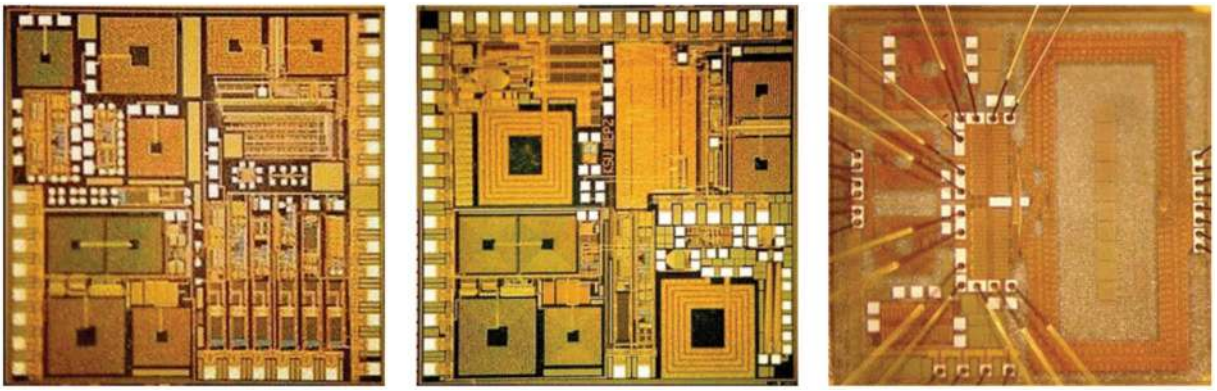


Fig. 19. ***Die photos of first three prototype RFICs.***

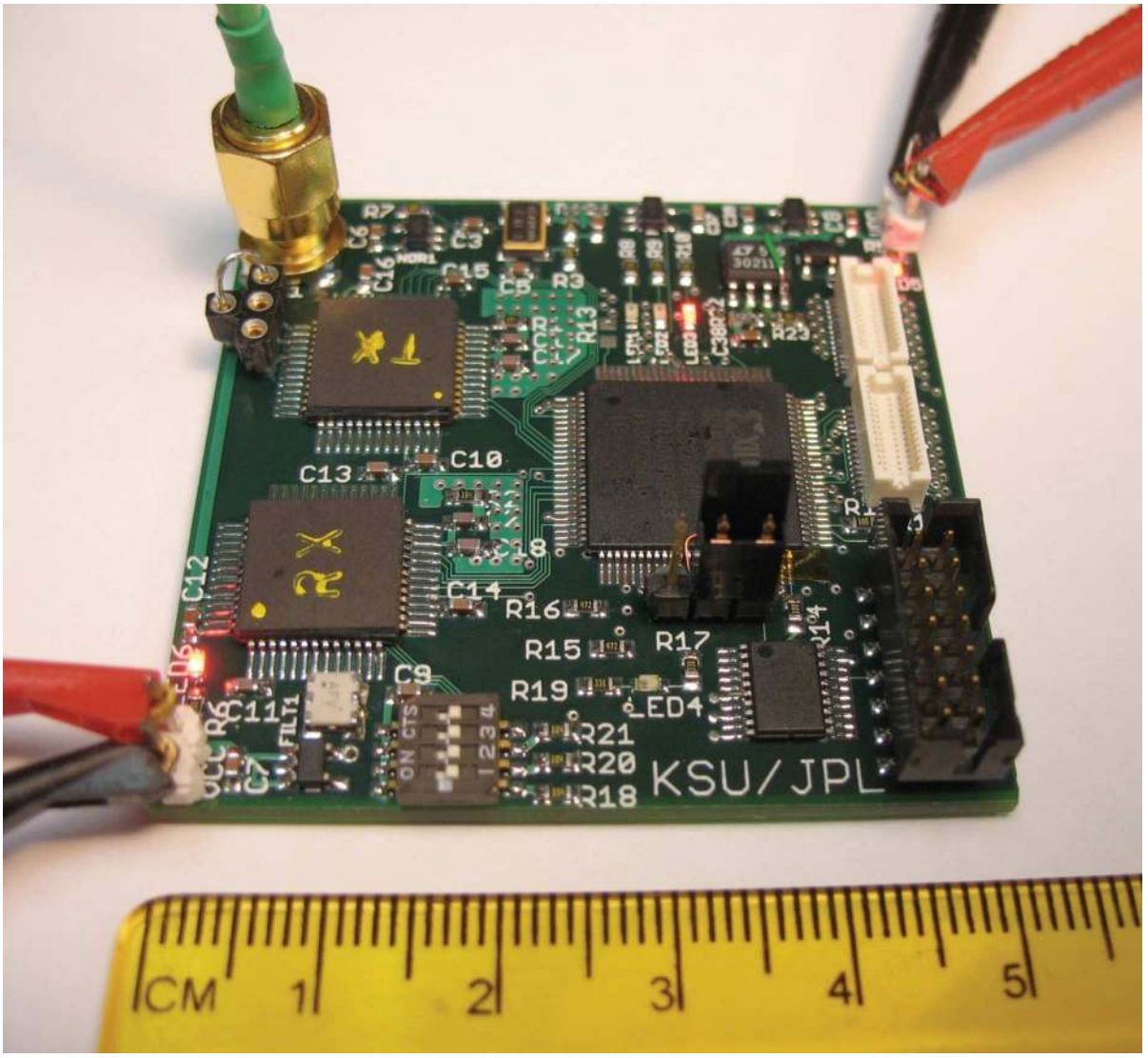


Fig. 20. ***System-level test PC board built from Fab1 and Fab2 prototypes plus FPGA.***

problems they create are significant modeling issues, as are coupling at the PC board level where circuit structures become physically larger.

Recognizing these problems and the need for iterative prototyping, RFIC development was carried out through a sequence of fabrications as shown in Fig. 19. The chips developed include a prototype receiver with simple integer-N synthesizer, a prototype transmitter with fractional-N synthesizer and revised receiver LNA circuits, and a 1-W power amplifier. A complete single-chip 100 mW transceiver incorporating circuits from the transmitter and receiver prototype fabrications has also been successfully developed. This fab-4 die is shown in Section VII.

A working microtransceiver prototype built from these early fabrications has been developed at the PC board level (Fig. 20) to allow simulated system-level testing and proof-of-concept demonstration. Design techniques, measured results, and lessons learned from each fabrication are covered in the following subsections.

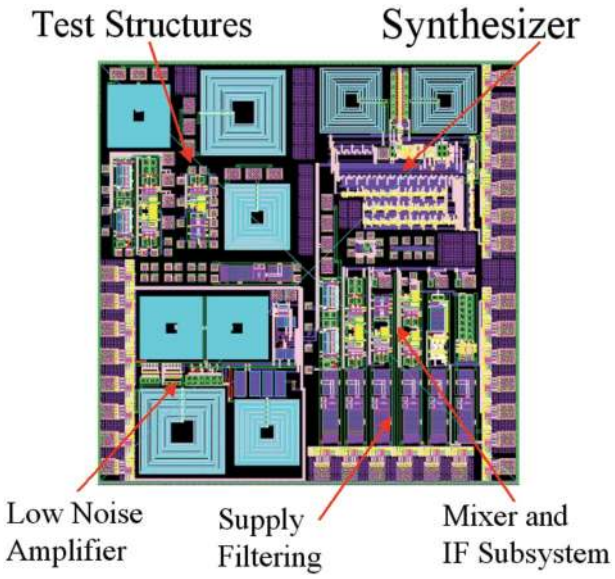


Fig. 21. *Layout/floorplan of first prototype IC.*

B. Receiver RFIC Prototype

The receiver subsystem is perhaps the most complex portion of an integrated transceiver design and was therefore prototyped first. The layout of the Fab-1 die containing the receiver's RFIC circuits is shown in Fig. 21.

The lower left quarter of the die is dedicated to the LNA that employs relatively large value (up to 220 nH) on-chip spiral inductors to achieve good noise figure at UHF frequency using minimal power. To the right of the LNA are the remaining mixer and IF amplifier circuits together with the 1-bit ADC. As discussed below, an integral part of this circuitry is supply filtering used to provide stability in the high-gain IF amplification chain. In the upper right is a simple integer-N synthesizer and associated VCO, while the upper left is devoted to test structures for characterization of individual functional blocks and inductors used in the design. The test-structure area of the floorplan also serves as a placeholder for the 10- and 100-mW power amplifier circuits prototyped in later fabrications.

The principle circuits comprising the receiver are shown in Fig. 22. The combined LNA and T/R switch is a cascoded tuned-RF amplifier with input matching as overviewed in Section III and elaborated below. The LNA outputs a differential signal, for on-chip noise immunity, to an image-reject mixer. The IR mixer and

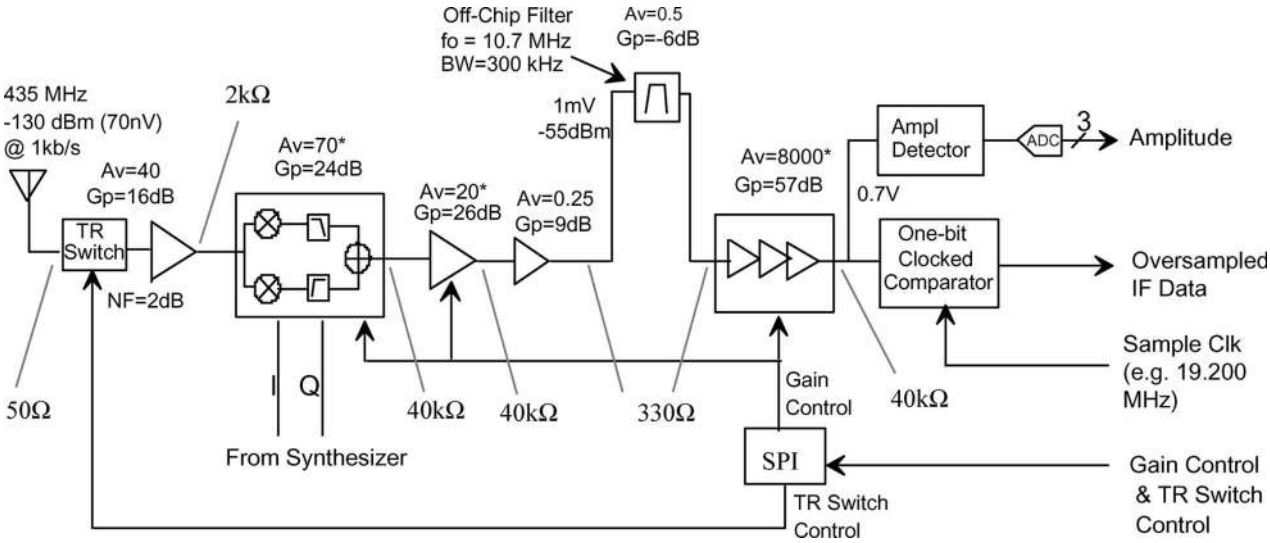


Fig. 22. *Allocation of gain to receiver subblocks.*

subsequent IF subsystem blocks are implemented in fully differential form to simplify circuit design, increase voltage swings, and provide good supply and ground noise immunity.

The IR mixer is created from two classic Gilbert-cell cores driven by the I and Q phase synthesizer signals, with outputs additively combined after $+/-45^\circ$ RC-CR phase shift networks (shown as high- and low-pass filters). The mixer itself offers a conversion voltage gain of approximately three, which is increased to 70 through the use of copies of the core IF amplifier block in each path prior to the summer (implemented simply by parallel combining of the differential IF amplifier outputs).

IF amplification of 26 dB is then provided to elevate the IF signal to a moderate millivolt level before it leaves the IC to be filtered. Differential to single-ended conversion and resistive filter impedance matching is performed prior to the filter interface, resulting in a voltage gain decrease of 0.25 but a power increase of 9 dB due to impedance drop from 40 K to 330 Ω. An on-chip 330-Ω termination is provided for the filter's output, and the signal is subsequently increased in level to approximately 700 mV by IF amplifiers prior to 1-bit conversion. While the 1-bit conversion process is theoretically immune to dynamic range issues (assuming only one signal occupies the IF passband), gain control is provided in each amplifier stage to allow optimization of the receiver's large-signal handling performance.

Detailed circuit-level design of individual subblocks was guided by the gain and impedance allocations shown in Fig. 22. Unlike board and module-level design, maintenance of 50-Ω levels is not important since all on-chip interconnects are short relative to a wavelength. Instead, impedance levels are selected based on power budget, frequency, and gain requirements. With a target consumption of 50 mW for the entire transceiver at 3.3 V, only 15 mA of current is available for the receiver, synthesizer, and companion digital modem IC. Hence, the entire RFIC is allocated approximately 10 mA in receive mode. The majority of this current is dedicated to the synthesizer and to the LNA that have critical phase-noise and noise figure requirements. The remaining mixer and IF subsystem components are designed to operate on approximately 3 mA. This translates to approximately 300 μA per block (e.g., IF amplifier stage). With signal swings in the range of 1-V peak differential on a 3.3-V supply, the impedance levels are therefore in the kilo-ohm range, with higher 40 k-Ω levels used to achieve high gain at IF. While such low power levels have clear consequences for input-referred compression point and intermodulation performance, these specifications are relaxed in this project, as previously discussed. Hence, the design process concentrated on the primary noise figure and stability concerns.

C. LNA Design and Performance

A simplified view of the LNA schematic is shown in Fig. 23. Omitted elements include bias-circuit details, switch-capacitors for 3-bit postmanufacture trimming of the center frequency, and diode-connected field-effect transistors (FETs) at the junction of C1/M1 and L1/C2 added for Electrostatic Discharge (ESD) protection in later designs. Also omitted from this diagram is a 50-Ω output impedance buffer for LNA noise figure measurements and an RC low-pass filter on the supply line used to provide noise immunity.

In receive mode, switch FETs M1, M2 are turned off, allowing L1 and C2 to convert the 50-Ω antenna

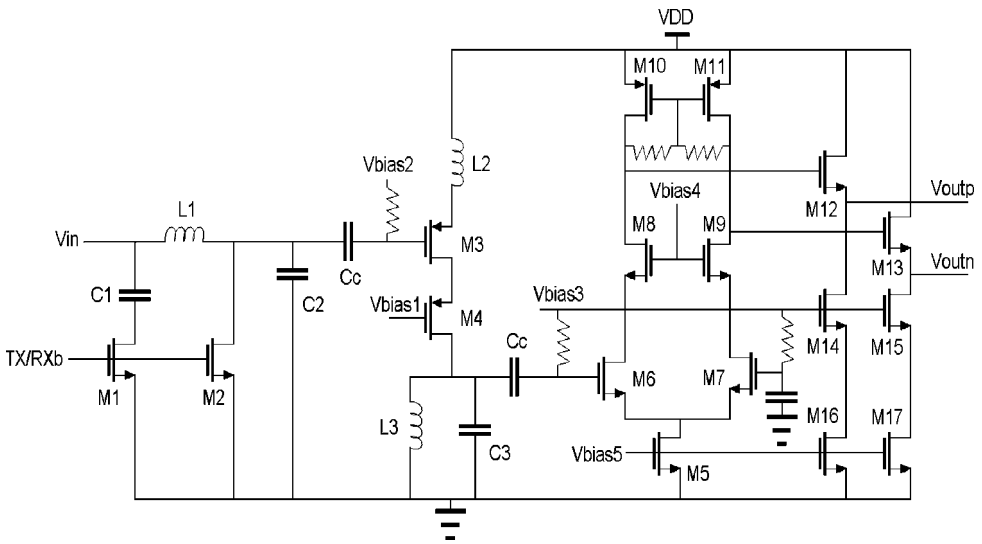


Fig. 23. ***Schematic diagram of LNA with integrated T/R switch circuits.***

Fig. 24. *Measured gain of LNA from 0 to 6 GHz using probing of on-chip output impedance buffer (not shown in Fig. 23). Vertical scale is 10 dB/div.*

impedance to approximately 1 K-Ω. The main cascode amplifier section of the LNA (M3, M4) is allocated 1.5 mA of current, and large 400 × 0.5 μm PFET devices are employed to provide low noise and sufficient gain. Due to the 435-MHz frequency range and low-power design goals, a relatively large 220-nH inductance L3 (composed of two spirals in series to address self-resonance limitations) is used in the LNA tank. Counterwinding of the spiral inductor turns reduces coupling to other circuits (e.g., other LNA and VCO inductors) simplifying modeling and reducing crosstalk noise issues. The remaining two spirals (L1, L2) provide 70 nH each to realize 200-Ω reactances needed in the input match and noise figure optimizing source degeneration. The input-match inductor L1 is located at the lower left corner of the layout in Fig. 21 and is physically large (600 μm) in order to maximize its Q for noise-figure optimization and to provide the needed trace width to handle 10 V_{peak} RF amplitudes when switches M1, M2 are closed during transmit. Following the main input gain stage, the signal is converted to differential form by M6, M7 and buffered by M12, M13 to drive the IR mixer's 2 K-Ω input impedance. Differential circuits are used from this point forward to address stability and supply noise concerns in the high-gain IF amplification as discussed below.

At 3 mA total current consumption, the LNA achieves a measured gain of approximately 22 dB and out-of-band rejection of 50 dB through 6 GHz, as shown in Fig. 24. The measured noise figure was found to be 3.4 dB at room temperature and falls to approximately 2.5 dB at the mean operating temperature of −50 °C. The noise figure is primarily limited by the on-chip inductor L1 and could be improved with a less integrated design. However, system specifications allow for some implementation margins, as discussed in Section III, so that this performance is currently considered acceptable.

D. IF Subsystem Stability and Supply Filtering

The mechanism behind potential oscillation within a high-gain IF subsystem is illustrated in Fig. 25, together with the supply filtering strategy adopted for mitigating it. Note that the model is simplified by showing all grounds as a common (and quiet) analog node. The supply is assumed to be the only source of noise and the only feedback path for oscillation. For this to be valid, careful identification of on-chip and off-chip grounds is mandatory. Here, the ground symbol represents an on-chip ground with low impedance created with wide metal traces.

The RC filter's job at each amplifier is to take noise on the supply and reduce this noise to acceptable levels. This is a critical component of the basic circuit implementation, especially within the low-level signal areas before the IF filter, which are highly susceptible to potential digital circuit noise on the supply. In the analysis of oscillation, this "noise" can also be from injection of IF signals onto the supply by the single-ended filter driver circuit or the final IF stage. If, for example, the output stage has a mismatch in its differential architecture half-circuits, an IF signal current will be drawn from the node Vdd′, producing a common-mode signal voltage on this node. If this is allowed to reach the main Vdd buss and the supply-path inductance

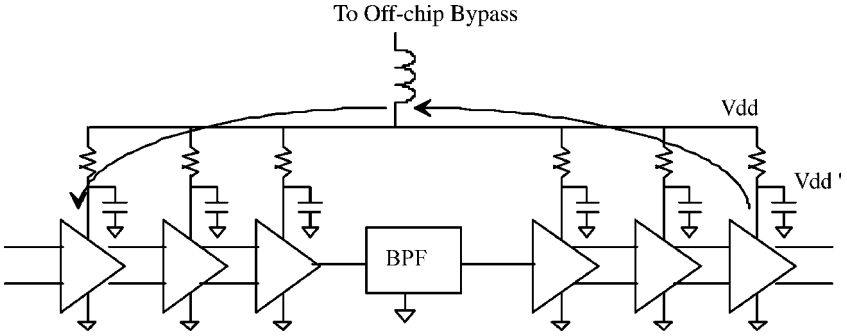


Fig. 25. *Signal feedback path for oscillation in high-gain IF amplifiers.*

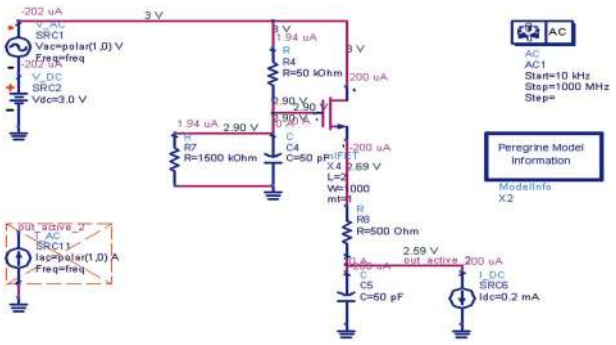


Fig. 26. *On-chip supply filters used in IF subsystem blocks.*

(bondwire and PCB trace to the off-chip bypass cap) is sufficiently high at IF, this signal voltage will be present on the Vdd node as well. If not sufficiently attenuated in the RC filter of the first IF amp, the signal will then couple into the first amp's signal path (due to mismatch in its diff-pair), and oscillation may result.

To quantify this problem, we assume the following values (selected from initial circuit design studies and conservative mismatch estimates):

- RC filters consist of 1-k resistors and 100-pF capacitors;
- transistor mismatch in the output stage $= 10\%$ (due to use of short-channel input pair);
- maximum current swing in output stage $= 200\ \mu$A (1 Vpk/5 k Ω) at min gain;
- supply line impedance of approximately 1 Ω at 10.7 MHz (15-nH path inductance);
- attenuation in first amplifier supply filter $= 16$ dB (from RC filter pole at 1.6 MHz);
- mismatch in input amp diff-pair $= 10\%$, yielding 20-dB supply rejection.

Under these conditions, the voltage on the output amp's internal Vdd line is approximately 28 mV (Xc $= 140\ \Omega$ times 200 uA), and the attenuation from this node to Vdd is approximately 1 Ω/1 k-$\Omega = 0.001$. The resulting 28-μV signal is attenuated by 16 dB in the input filter and an additional 20 dB from the amplifier's differential architecture, yielding an equivalent input signal of 450 nV. After amplification by the cascade gain of 400 000, the resulting output becomes 0.18 V. Hence, the loop gain is 0.18 V/1 V $= 0.18$, which is (marginally) acceptable.

Obviously the largest attenuation is the voltage division from the output stage Vdd′ node to the low impedance supply line. Thus, as in most high-frequency IC applications, it is critical to minimize the inductance in the Vdd path and to provide an adequate off-chip bypass.

In this project, the simple RC low-pass filters were replaced by the active circuit of Fig. 26, which provides superior rejection at lower supply voltage burdens for a given current. Using a low-threshold FET offered in the process, a measured 40-dB supply rejection is achieved at 10.7 MHz with only 0.4 V (0.7 V) burden at 0.3 mA (0.9 mA) current draw.

E. Ground Bounce Issues and Layout Planning

As previously noted, it is critical for all IF gain blocks in Fig. 25 to share a common, quiet ground node. This can be achieved as shown in Fig. 27 using a single-point connection strategy on-chip.

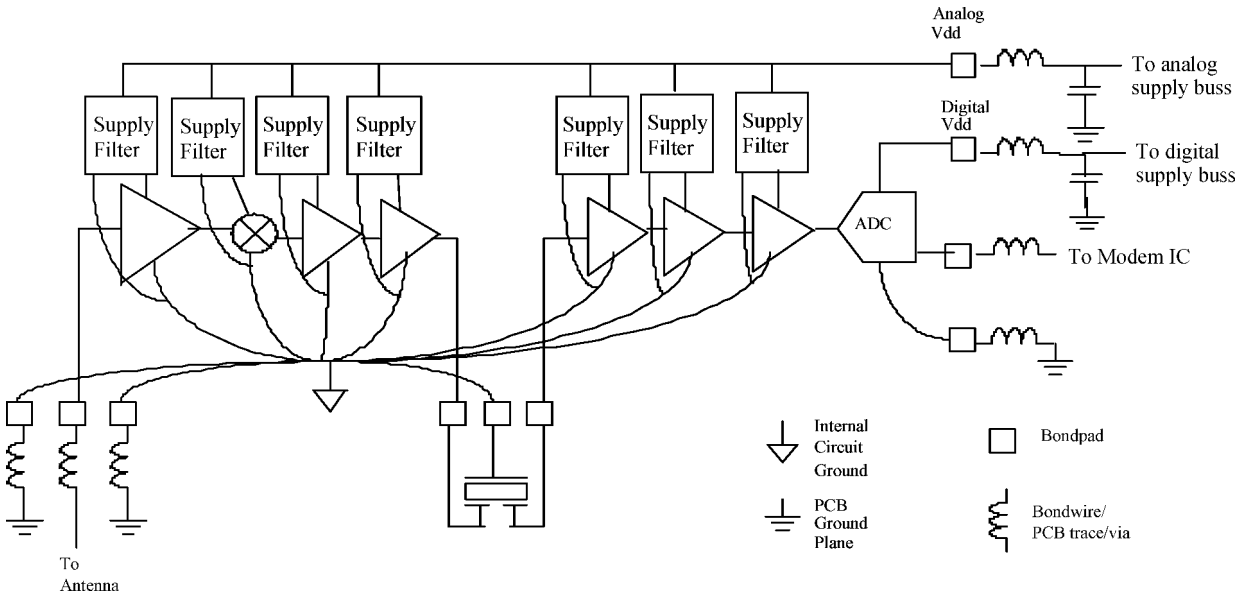


Fig. 27. *Identification of on-chip and off-chip grounds.*

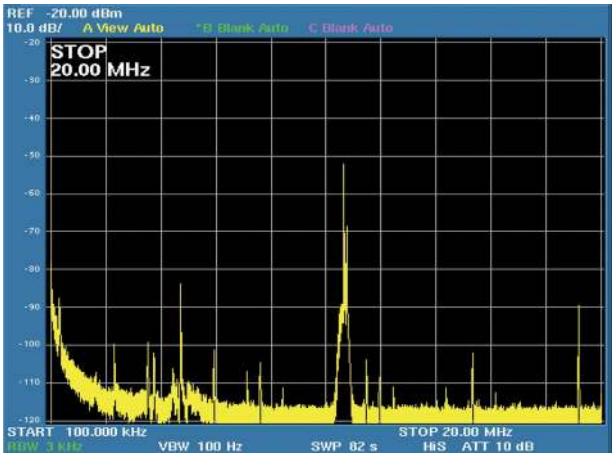


Fig. 28. *IF filter output spectrum from 0 to 20 MHz with −90-dBm RF input. Vertical scale is 10 dB/div.*

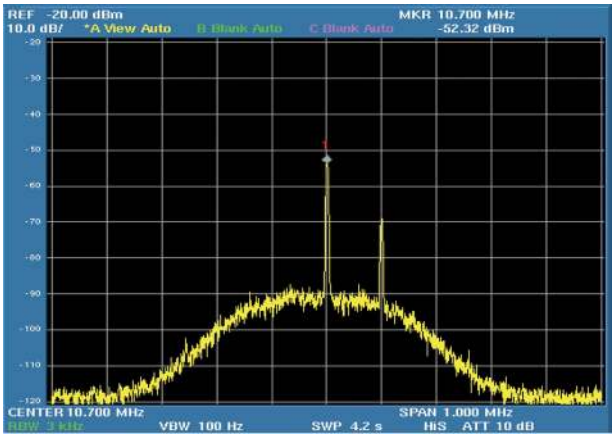


Fig. 29. *IF filter output spectrum with 1 MHz span, showing in-band spur to right of downconverted −90 dBm RF input signal.*

As illustrated in Fig. 27, the bondwire, package leadframe, and PC-board via inductances create impedances between the PC board (PCB) ground and the on-chip ground node, with nonnegligible "ground bounce" to any RF, IF, or digital currents flowing through them. However, this simply means that the PCB ground is not ground as viewed by the on-chip circuits.

Ground-bounce voltages across these inductances can therefore be viewed as adding to any supply noise, since the voltage drop in these inductors is now in series with the off-chip supply voltage. The on-chip ground trace is the actual signal ground for all RF and IF signals except the antenna. Thus, it is important to keep the ADC ground and grounds of other on-chip digital circuits separate to prevent coupling of high-frequency spurs from logic gate switching from entering the LNA or early IF stages.

Finally, note that a separate ground pin is routed out to the IF filter. The filter's ground is not attached to PCB ground, but rather attaches only to this pin on the IC. Ground bounce will then not affect the low-level IF signal routed off and back on to the chip. Instead, the filter becomes (electrically) an additional "on chip" element sharing the internal quiet ground.

While these strategies were developed in advance of the first prototype's layout and were found to be successful, lessons of ignoring such considerations were learned in other areas of the RFIC development. For example, ground bounce in the chip's TCXO receiver circuits (synthesizer clock input circuits) resulted in significant problems in synthesizer phase-locked-loop stability. In this case, ground-bondwire ac voltage drops caused by the RF output signal modified the synthesizer clock input threshold and hence the reference phase sufficiently to destroy the intended loop transfer function—especially when operating at the higher 100-mW mode. A workaround consisting of adding a fast edge-time inverter between the TCXO's sinewave output and the synthesizer clock input corrected the problem. All of these problems have been addressed in the final single-chip design through proper adherence to the guidelines above. For further guidelines important at the PCB design level, see [33].

F. Receiver RFIC Prototype Test Results

The receiver prototype's overall performance was measured in a sequence of PC board test vehicles beginning with a simple 40-pin DIP packaging and plug-in protoboard and progressing to the final proof-of-concept demonstration board shown previously in Fig. 20. No IF stability problems were noted for any of the test vehicles, validating the performance of the stability measured adopted. Digital noise coupling into the monitored IF signal degraded

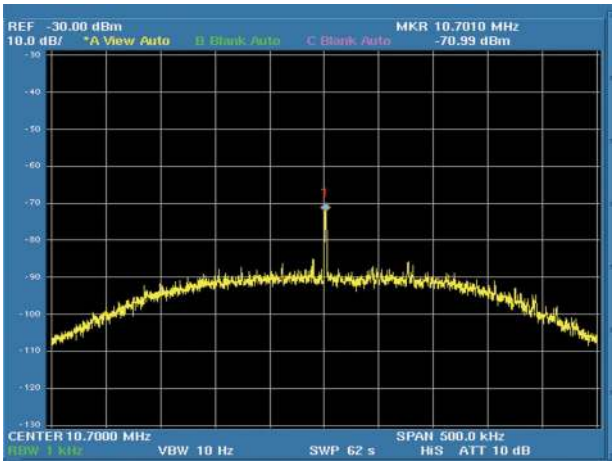
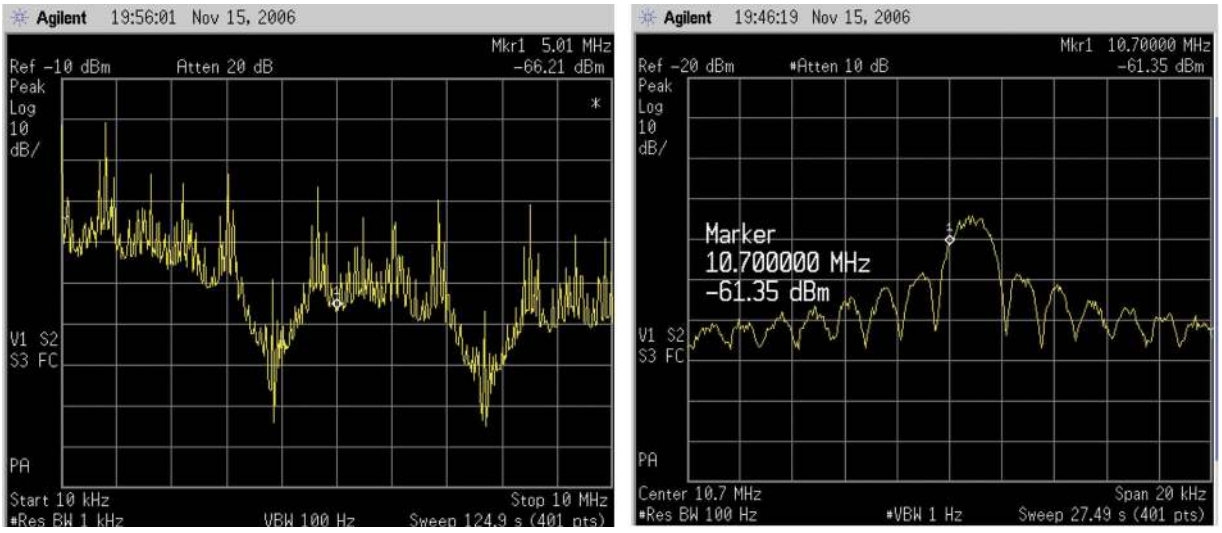


Fig. 30. *Mixer output spectrum from full-transceiver (fab-4) die with −120 dBm RF input signal.*

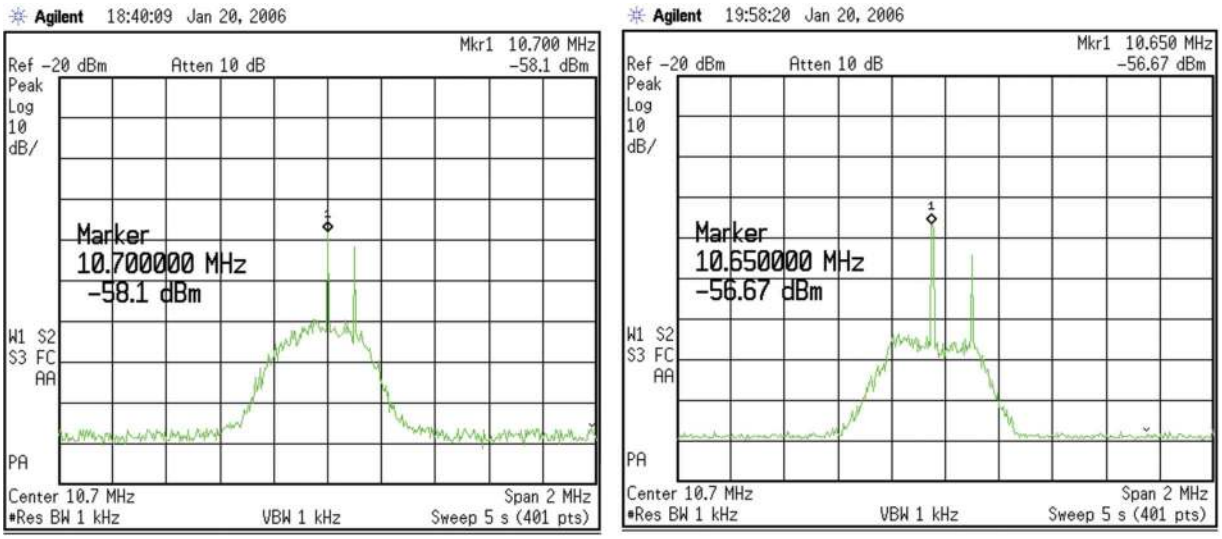


(a) (b)

Fig. 31. ***Spectrums of final ADC output. (a) 0–10 MHz and (b) 10.7-MHz center with 20-kHz span.***

receiver performance at low signal levels in the protoboard and early PC boards as expected for circuits with poor or absent ground planes. However, this injected noise is sufficiently low in the final four-layer PC board design of Fig. 20 to allow full-sensitivity testing, as seen in the wideband filtered-IF spectrum of Fig. 28. This spectrum was taken with a −90 dBm RF input and with the full digital modem receiver code running in the onboard FPGA. The downconverted signal is 40 dB above the IF noise floor (see Fig. 30) so that the IF noise floor is equivalent to −130 dBm at the RF input. In Fig. 28, the only spectral lines above this IF noise floor other than the downconverted RF signal (and an associated inband spur discussed below) are the 4.8-MHz divided reference and the 19.2-MHz TCXO. Both of these are attenuated sufficiently by the subsequent IF stages before reaching the ADC.

Fig. 29 shows a 1-MHz span view of the IF passband output where a significant spurious response 100 kHz above the main signal is evident. This spur was traced to an image response to the three hundred eight-first harmonic of the 1.2-MHz divided reference frequency used in the first receiver prototype's integer-N synthesizer. To



(a) (b)

Fig. 32. ***Spectrums at IF output of fab-1 prototype with 2 MHz span, taken at (a) room temperature and (b) −100 °C.***

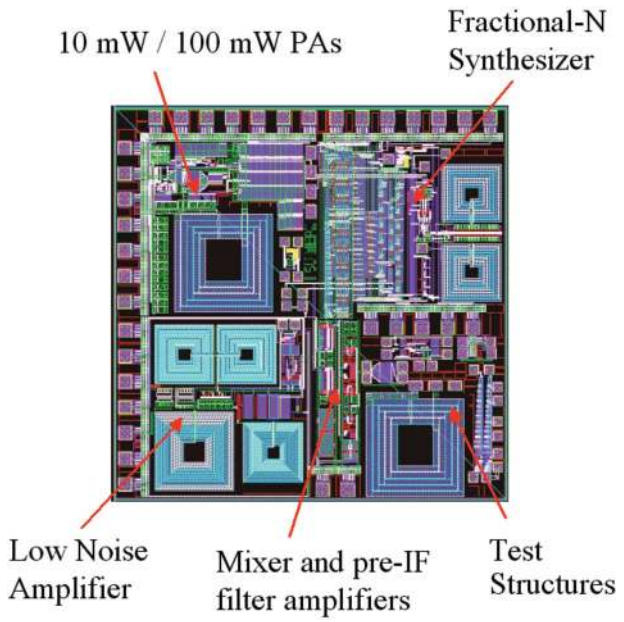


Fig. 33. *Transmitter prototype layout floorplan.*

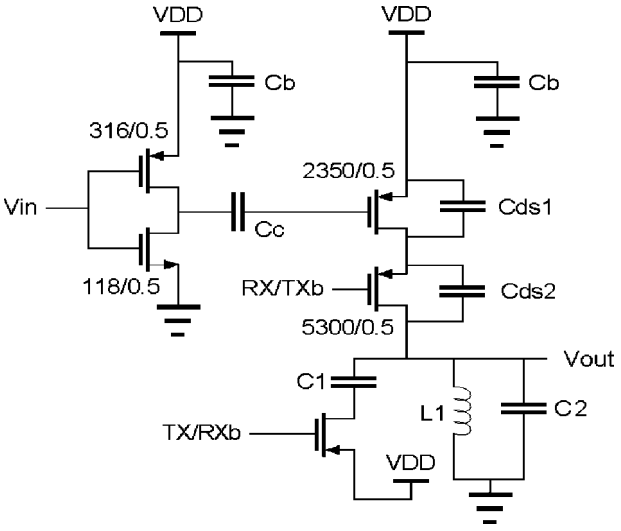


Fig. 34. *Ten- and 100-mW power amplifier circuits (bias details omitted).*

eliminate the spurious response, the later prototypes included an improved synthesizer with fractional-N design to allow a 4.8-MHz divided reference frequency. Extensive on-chip bypassing was also added to all on-chip digital circuitry to reduce the size of power-to-ground loops that digital switching current spikes travel through. This reduces the potential for crosstalk from digital circuit produced magnetic fields coupling into the LNA inductors. In addition, top-metal in the process was placed over the full digital circuitry to serve as a ground plane. This creates image currents that cancel magnetic fields in the same manner typically practiced by board-level designers.

The IF filter output spectrum shown in Fig. 30 was taken from the fab-4 full transceiver, validating that these techniques were successful. With an RF input signal at the designed sensitivity level of −120 dBm, the IF spectrum within the filter passband achieves a signal-to-spur ratio of greater than 15 dB, sufficient for full sensitivity reception, while 20-MHz span plots closely match the levels of Fig. 28 outside the passband.

As an end-to-end validation of the RFIC receiver prototype, Fig. 31 shows spectrum analyzer displays of the final 1-bit digital data stream leaving the ADC for the case of a BPSK modulated −100 dBm RF input. Although the spectrum is aliased to several frequencies due to the 3.84-MHz sample clock delivered to the RFIC from the FPGA, and is sinc-shaped due to the nonreturn-to-zero ADC output pulse-shape, a clear replica of the BPSK signal spectrum is evident at the 10.7-MHz frequency used for the right-hand plot. Thus, the received signal is faithfully digitized with good dynamic range, as discussed in the system-design presentation of Section III.

Receiver testing at cryogenic temperatures also shows good results. Fig. 32 shows the IF passband at room temperature and at −100 °C for the fab-1 prototype. The signal stays roughly in the center of the passband, thanks to the high-side injection strategy. Further, the overall signal-to-noise ratio improves at low temperature, as expected due to reduced circuit noise.

G. Transmitter RFIC Prototype Test Results

The second IC fabrication was devoted to transmitter circuit prototyping and to synthesizer and LNA circuit improvements as previously discussed. The layout floorplan is shown in Fig. 33, where the 10- and 100-mW power amplifier circuits are seen in the upper left corner previously occupied by receiver subcircuit test structures.

The power amplifier schematics are shown in simplified form in Fig. 34. The inverter at the left implements a simple 10-mW driver while the cascade-

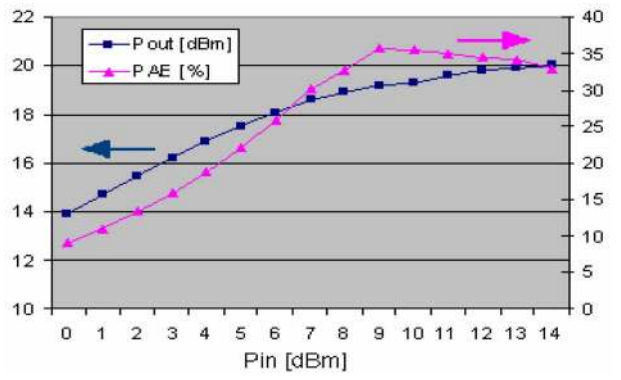


Fig. 35. *One hundred mW power amplifier measured performance.*

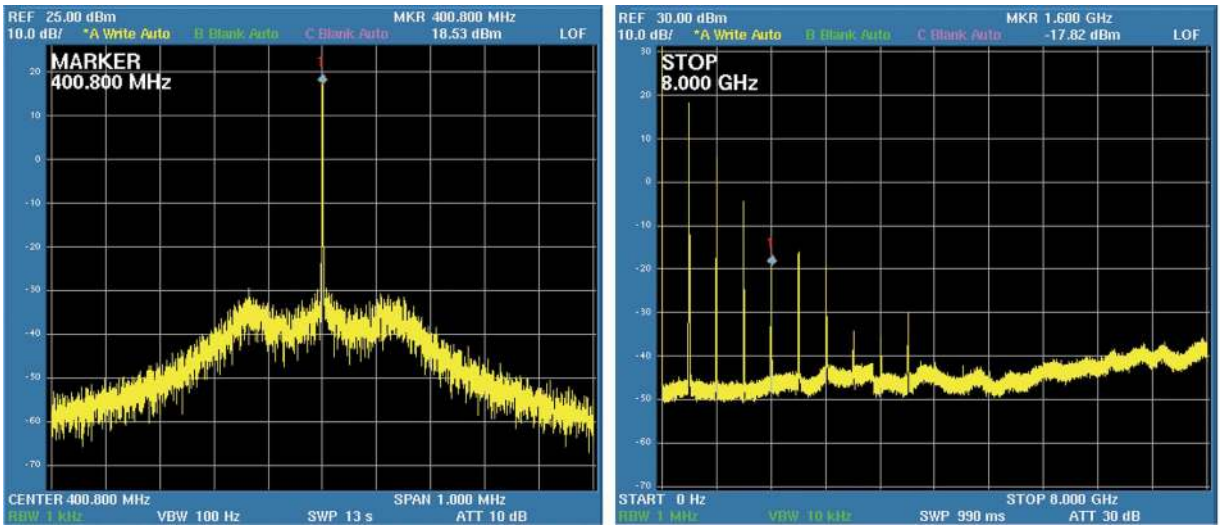


Fig. 36. ***One hundred mW power amplifier measured output spectrums at 1-MHz span and zero to 8 GHz.***

switching circuits on the right implement a high-efficiency 100-mW output amplifier. The control signal input Tx/Rxb modifies the output tank circuit to present a high impedance at 435 MHz in receive mode as part of the TR switching function discussed previously in Section III.

Measured performance for the 100-mW PA is shown in Fig. 35. Output power at 10-mW drive is slightly low (19.5 dBm). This problem was traced to a frequency offset in the resonant tank, placing the peak response at 350 MHz rather than 400 MHz, and has been corrected in the final fabrication runs through LC tank modifications. The measured power-added efficiency (PAE) is 35%, which matches well with simulation results. At 3.3 V, the amplifier consumes 83 mA, or 275 mW of dc power. Together with other circuitry, the total power consumption is under 350 mW, in general keeping with project goals outlined in Table 1 of Section II.

To verify the overall fidelity of the output signal to be received by the Mars orbiter, spectrums and signal constellations were measured as shown in Figs. 36 and 37, respectively. In the case of the constellation measurement, a noncoherent signal generator reference was used with the HP8981A vector signal analyzer, and no baseband filtering

Fig. 37. ***One hundred mW power full transmitter measured constellations in BPSK and residual-carrier BPSK modes.***

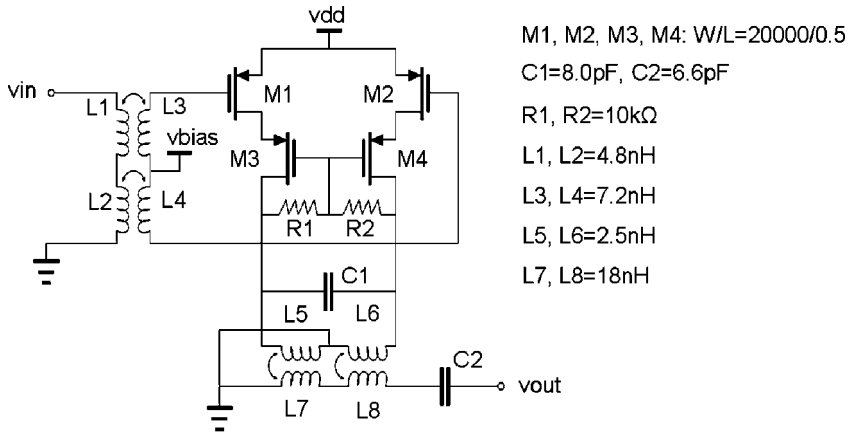


Fig. 38. ***Simplified schematic of 1-W power amplifier.***

was used. Hence, the small arcs shown include the full integrated phase noise of the VCO (and some phosphor tracks due to rotation during photography).

As seen in Fig. 36, measured continuous-wave phase noise is a relatively low −85 dBc/Hz at a 50-kHz offset, while harmonic content is relatively high at −10 dB at the second harmonic (reduced to −14 dBc when the 100 mW output is connected to the LNA input to form the TR switch function). The measured phase noise is sufficiently low to achieve an acceptable constellation, as shown in Fig. 37. While harmonic content is high relative to terrestrial radios, it is considered an acceptable tradeoff here for the level of integration achieved.

H. One-Watt PA Prototype

As discussed in Section II, the microtransceiver design offers a 1-W output power option for missions requiring large data-return volumes. While no fully integrated UHF watt-level power amplifiers existed at the start of the project, successful 1-W power amplifiers had been reported at cellular frequencies [25]. Using the high-Q passives offered by the SOS process, it was therefore plausible to propose such a design at UHF, provided sufficient die area was used.

The design developed in this project is shown in Fig. 38 [26]. It consists of an on-chip balun (center-tapped transformer structure), a differential amplifier core to provide power-combining functionality and bond-wire immunity, a cascode switching transistor topology to address low-breakdown voltage issues, and an output transformer. The output transformer is critical to the design, providing the needed step-down from the 50-Ω load impedance to approximately 10 Ω needed to achieve 1-W output on a 3.3-V supply. Not shown in this figure is the bias circuitry and switching circuits used to shut down the large transistors to prevent noise injection into the receiver when used with the TR switching technique previously described.

The only off-chip components are bypass capacitors and a single series output matching capacitor (which will be incorporated into C2 in future implementations).

Measurements of the amplifier show good performance, reaching 29-dBm output power at 29% efficiency on 20 dBm of input power. The amplifier has been successfully mated with the transmitter prototype IC without oscillation problems and has withstood operation at 4-V supply without failure suggesting good reliability. The amplifier has also been characterized for use with the TR switching technique. In receive mode, no noise floor increases over thermal background levels were observed when using a 4-dB noise figure test amplifier,

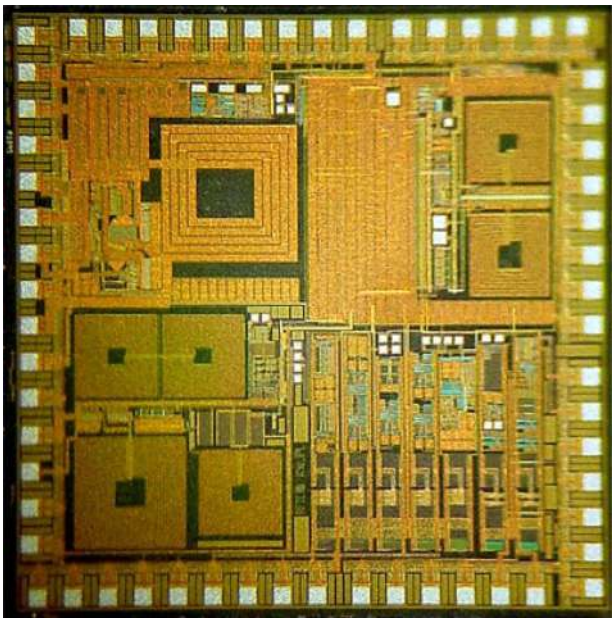


Fig. 39. ***Die photo of fully integrated single-chip 100-mW transceiver.***

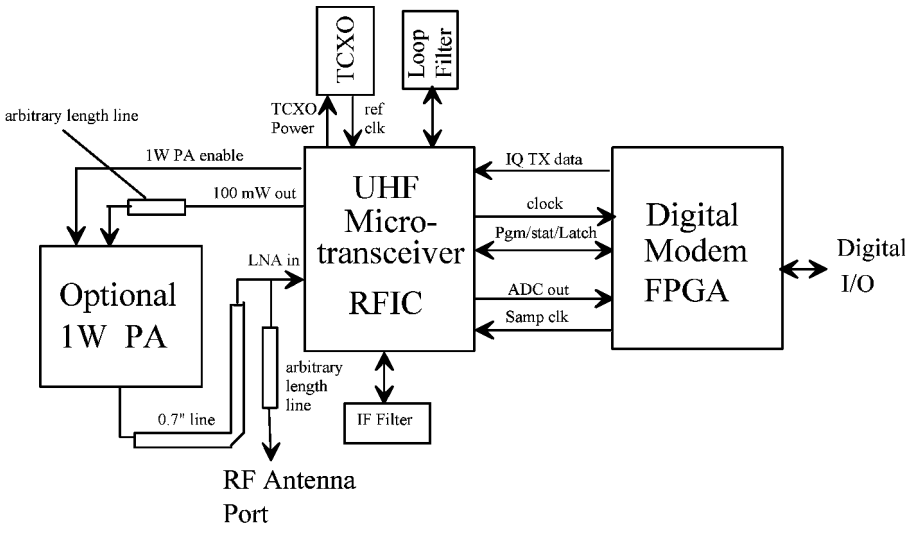


Fig. 40. ***Final three-chip 1-W transceiver solution.***

implying that degradations to receiver noise figure will be at most a fraction of a decibel. Details of this design are reported in [34].

VII. CONCLUSIONS AND FUTURE DIRECTIONS

Existing radio transceivers carried aboard the highly successful Mars Exploration Rovers are too large to allow development of miniature scout vehicles envisioned for certain future missions such as aerobots, expendable dropoff probes, and small networked landers. This project has targeted a demonstration that UHF transceivers compatible with the Mars environment and communication infrastructure can be fully integrated to reduce mass, volume, and power by one to two orders of magnitude. Through iterative prototyping of core circuits in an RFIC-friendly rad-hard process, this goal has been met. The demonstration board of Fig. 20 was constructed using early prototype ICs and implements a full 100-mW transceiver with mass, volume, and power consistent with the project goals. Testing of these circuits shows good performance and confirms that the full specifications of Table 1 in Section II are achievable.

A single-chip 100-mW transceiver built from the prototype circuits discussed in this paper was recently received from fabrication and is currently being tested. The chip, shown in Fig. 39, measures 3.2 × 3.2 mm^2 and incorporates all circuits discussed, plus the receive-strength signal indicator, on-chip sensor for temperature measurement, and optional analog I/Q transmitter inputs for additional modulation types such as FSK, as shown in Fig. 6. Measurements to date indicate that the single-chip design meets or exceeds the performance of the fab-1 and fab-2 prototypes detailed in this paper.

The final transceiver envisioned for use on future Mars missions is a three-chip solution illustrated in Fig. 40, where the 1-W power amplifier option of Fig. 38 is included.

Based on the demonstrated performance and techniques discussed in this paper for addressing signal coupling mechanisms, it is expected that a full 1-W transceiver including the low-complexity digital modem design described in Section V can be integrated into a single die as small as 6 × 6 mm^2 in future development projects. ■

Acknowledgment

The authors gratefully acknowledge the work of the following individuals who have assisted in the early prototyping and testing processes: M. Hartter, E. Cullens, K. Kovala, and J. Harder.

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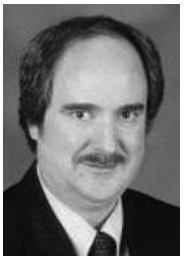

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