A Miniaturized Wilkinson Power Divider With CMOS Active Inductors

Liang-Hung Lu, *Member, IEEE*, Yu-Te Liao, and Chung-Ru Wu

***Abstract*—A miniaturized Wilkinson power divider implemented in a standard 0.18-μm CMOS process is presented in this letter. By using active inductors for the circuit implementation, a significant area reduction can be achieved due to the absence of distributed components and spiral inductors. The power divider is designed at a center frequency of 4.5 GHz for equal power dividing with all ports matched to 50 Ω. Drawing a dc current of 9.3 mA from a 1.8-V supply voltage, the fabricated circuit exhibits an insertion loss less than 0.16 dB and a return loss better than 30 dB at the center frequency while maintaining good isolation between the output ports. The active area of the miniaturized Wilkinson power divider is 150 $\times$ 100 μm^2, which is suitable for system integration in monolithic microwave integrated circuit (MMIC) applications.**

***Index Terms*—Active inductors, lumped power divider, miniaturization, monolithic microwave integrated circuit (MMIC), regulated cascode, Wilkinson power dividers.**

I. Introduction

THE Wilkinson power divider has been widely used in microwave systems for decades. Typically, the power divider is a three-port network which divides or combines incident power at the output. Due to the use of transmission line sections in conventional circuit implementation, the size of a Wilkinson power divider is proportional to the wavelength at the center frequency. The nature of the transmission line length has long impeded its applications in monolithic microwave integrated circuits (MMICs), especially for frequencies below 10 GHz. Consequently, efforts have been made to miniaturize the size of a Wilkinson power divider by using three-dimensional (3-D) technologies [1], lumped-distributed techniques [2], and capacitive loading [3]. However, it is still a challenging task to implement a power divider with a chip area suitable for monolithic system integration.

In order to reduce the circuit size effectively, the concept of replacing the transmission line sections with lumped passive components has also been adopted [4], [5]. Though a smaller circuit size can be achieved, it suffers from higher insertion loss and limited bandwidth due to the lack of high-Q on-chip passive components. In this letter, a lumped Wilkinson power divider with active inductors is proposed to overcome the limitations of the on-chip passive components. The circuit has been implemented in a standard 0.18-μm CMOS technology for demonstration.

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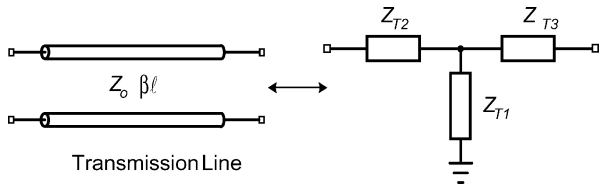

Fig. 1. Transmission line section and its lumped T-network.

Section II describes the lumped equivalence of the Wilkinson power divider. The design of the miniaturized power divider in 0.18-μm CMOS is presented in Section III. Experimental results are shown in Section IV and conclusions are given in Section V.

II. Lumped Wilkinson Power Divider

At the center frequency, a transmission line section with a characteristic impedance Z_0 and electrical length $\beta\ell$ can be replaced by its lumped equivalent T-network [6] as shown in Fig. 1. The lumped passive components required in the equivalent network can be obtained by equating the ABCD matrices

$$\begin{bmatrix} \cos\beta\ell & jZ_0\sin\beta\ell \\ jY_0\sin\beta\ell & \cos\beta\ell \end{bmatrix} = \begin{bmatrix} 1+\frac{Z_{T2}}{Z_{T1}} & 2Z_{T2}+\frac{Z_{T2}^2}{Z_{T1}} \\ \frac{1}{Z_{T1}} & 1+\frac{Z_{T2}}{Z_{T1}} \end{bmatrix}. \quad (1)$$

For a lumped equivalent network, the loss of the transmission line section is not directly correlated to the electrical length. Therefore, the Wilkinson power divider can be implemented by 1/4λ or 3λ/4 branches [7] without the penalty in insertion loss. Since shunt inductance is preferable for the implementation of active inductors, an electrical length of 3λ/4 is employed in the proposed circuit topology. By replacing the transmission line sections with the T-networks, the equivalent circuit of the lumped Wilkinson power divider is illustrated in Fig. 2.

To investigate the influence of the inductor Q-factors on the performance of the lumped power divider, a simulation was performed. Based on the simulation results, it is observed that the quality factor of the inductor plays an important role in the divider performance. If an insertion loss of a lumped power divider equivalent to that of its distributed counterpart is desirable, inductors with a Q-factor of 30 or higher are required.

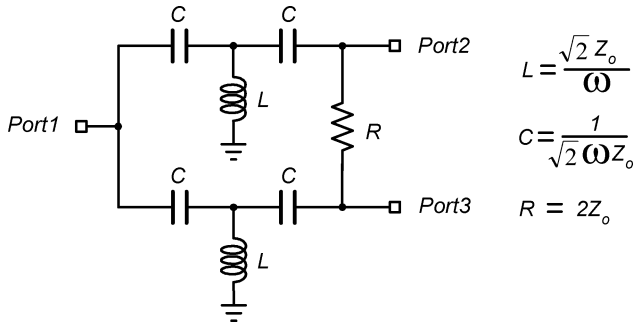

Fig. 2. Equivalent circuit of the lumped Wilkinson power divider.

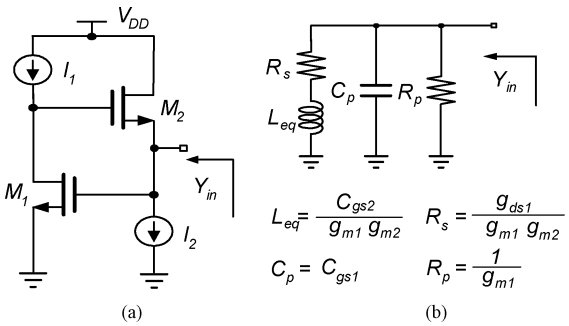

Fig. 3. (a) Schematic of the regulated cascode active inductor. (b) The small-signal equivalent circuit.

III. Circuit Design

To alleviate the design limitations due to the substrate losses and the inferior Q-factors of the on-chip passive components, active inductors have been employed in the design of the Wilkinson power divider. The regulated cascode active inductor [8] and its equivalent circuit are shown in Fig. 3(a) and (b), respectively. As illustrated in Fig. 3(a), a back-to-back configuration of transistors M_1 and M_2 is used for the implementation of the active inductors. Based on the small-signal analysis, the input admittance of the active inductor can be expressed as [9]

$$Y_{\text{in}} \approx \frac{g_{m1}g_{m2}}{g_{ds1} + sC_{gs2}} + g_{m1} + sC_{gs1}. \tag{2}$$

The simplified expression of the input admittance can be modeled by an equivalent inductance (L_{eq}) with a series resistance (R_s), a shunt capacitance (C_p), and a shunt resistance (R_p) as shown in Fig. 3(b). Since the Q-factor of the active inductor is determined by the values of the resistances R_p and R_s, it can be optimized by choosing the circuit parameters to minimize R_s and to maximize R_p. In the design of high-Q active inductors, gain-boosting techniques have been employed by replacing transistor M_1 with a cascode stage. Using a standard 0.18-μm CMOS process under a 1.8-V supply voltage, an active inductor with an inductance value of 2.5 nH is designed for the 4.5-GHz Wilkinson power divider.

Fig. 4 shows the complete schematic of the proposed lumped Wilkinson power divider. The shunt inductances in the lumped equivalent circuit, as shown in Fig. 1, are replaced by the regulated cascode active inductors while polysilicon resistors and metal–insulator–metal (MIM) capacitors provided by the standard CMOS process are used for the resistive and capacitive elements, respectively. By employing the active inductors, no distributed elements and spiral inductors are required for the circuit implementation. Several orders of magnitude in area reduction can be achieved in this design. In addition, the resulting high Q-factor of the inductors also enhances the performance of the lumped power divider.

Another important feature of the proposed Wilkinson power divider is the reconfigurability in the center frequency. As indicated in Fig. 3(b), the equivalent inductance L_{eq} and Q-factor of an active inductor depend on the bias currents of transistors M_1 and M_2. By adjusting the bias currents I_1 and I_2, the center frequency of the power divider can be manipulated by the value of L_{eq}. Therefore, it can be used to realize reconfigurable radio frequency (RF) front-ends for multiband and multistandard applications.

IV. Experimental Results

The lumped Wilkinson power divider is designed and fabricated in a standard 0.18-μm CMOS technology. Fig. 5 shows the microphotograph of the fabricated power divider. The total chip area is 700×550 μm^2 including the pad frame, where the active area occupy only 150×100 μm^2. To characterize the S-parameters of the Wilkinson power divider, on-wafer probing was performed using multiport vector network analyzer. No on-chip termination is required and the impedance mismatch during the measurement can be minimized for better accuracy. Good agreement was obtained between the simulation and the measurement.

When operating at a center frequency of 4.5 GHz, the power divider draws a dc current of 9.3 mA from a 1.8-V supply voltage. The measured S-parameters are shown in Fig. 6. With the high Q-factor provided by the active inductors, the power divider exhibits an insertion loss of 0.16 dB for -3 dB power coupling. The measured bandwidth, defined as the frequency range where $|S_{11}| < -15$ dB, is 11.1%. Within this bandwidth, insertion loss maintains lower than 0.5 dB, while the isolation, characterized by $|S_{23}|$, is better than 15 dB. The measured noise figure and $P_{\text{in}-1\text{ dB}}$ are 11.7 dB and -10 dBm, respectively. Fig. 7 illustrates the reconfigurability of the proposed circuit. By adjusting the bias currents I_1 and I_2, the center frequency of the Wilkinson power divider can be tuned from 4 to 5 GHz while maintaining an insertion loss lower than 0.7 dB. The performance of the power divider is summarized in Table I.

V. Conclusion

A miniaturized 4.5-GHz Wilkinson power divider employing active inductors has been designed and fabricated in a standard 0.18-μm CMOS technology. Due to the absence of transmission lines and spiral inductors, a significant area reduction is achieved, especially for applications at frequencies below 10 GHz. The enhanced Q-factors of the active inductors result

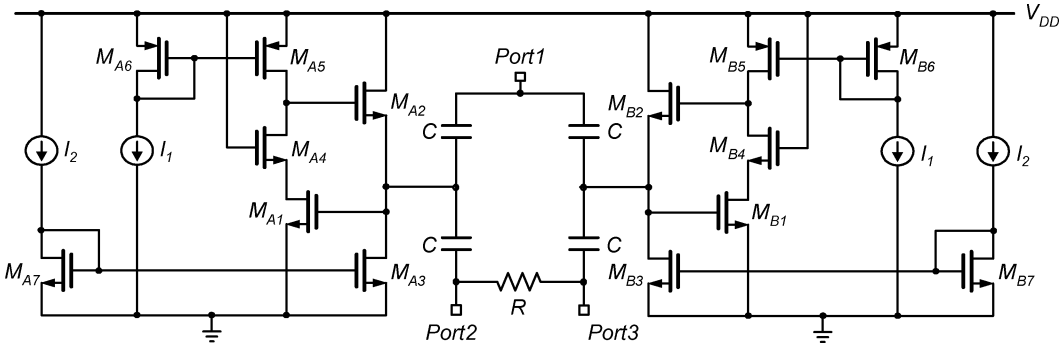

Fig. 4. Complete schematic of the lumped Wilkinson power divider with CMOS active inductors.

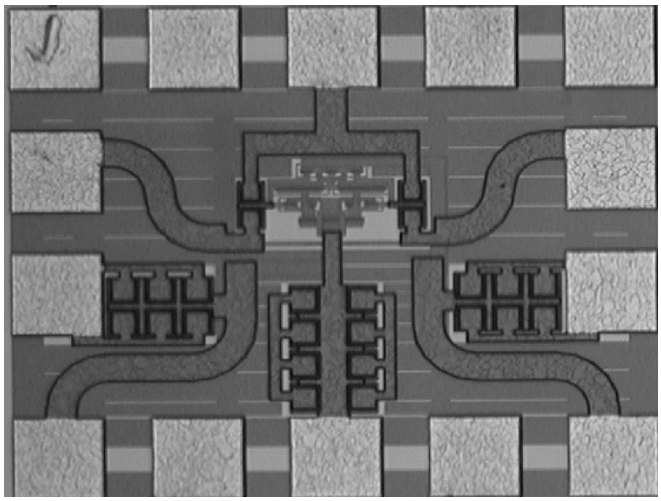

Fig. 5. Die photograph of the fabricated Wilkinson power divider.

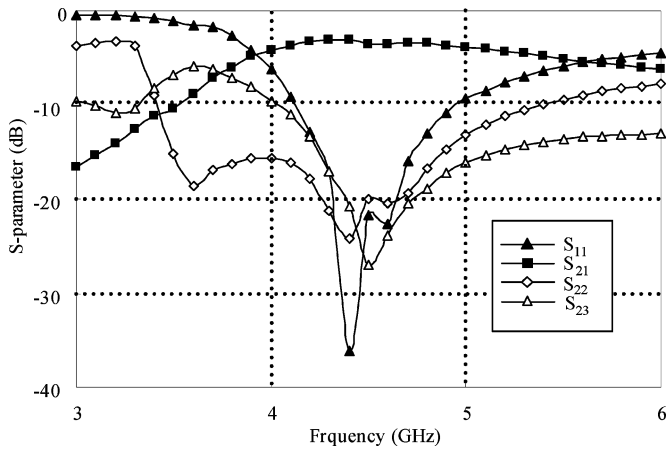

Fig. 6. Measured S-parameters of the Wilkinson power divider.

in an insertion loss of 0.16 dB and a return loss better than 30 dB at the center frequency.

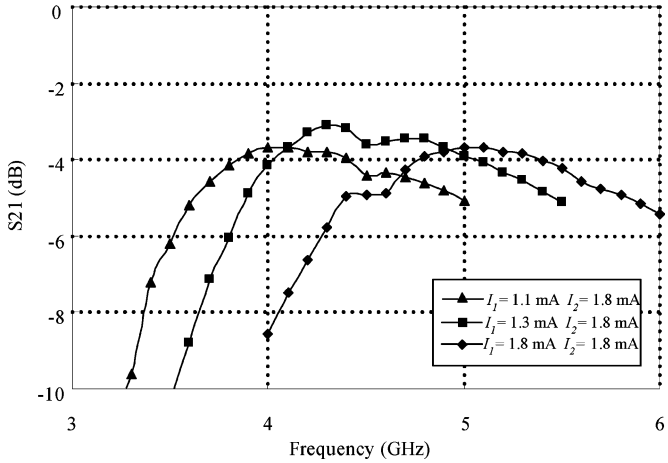

Fig. 7. Reconfigurability of the Wilkinson power divider.

TABLE I
PERFORMANCE SUMMARY OF THE WILKINSON POWER DIVIDER

Technology	0.18-μm CMOS		
Chip size	700×550 μm^2		
Center frequency (GHz)	4.0	4.5	5.0
Insertion loss (dB)	0.68	0.16	0.70
Return loss (dB)	26.0	30.4	22.6
Isolation (dB)	19.7	27.0	23.0
Power consumption (mW)	15.6	16.7	19.4

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