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Authors

Muller, R
Le, HP
Li, W
[et al.](#)

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A Minimally Invasive 64-Channel Wireless μ ECoG Implant

Rikky Muller, *Member, IEEE*, Hanh-Phuc Le, *Member, IEEE*, Wen Li, *Student Member, IEEE*, Peter Ledochowitsch, *Member, IEEE*, Simone Gambini, *Member, IEEE*, Toni Bjorninen, *Member, IEEE*, Aaron Koralek, *Student Member, IEEE*, Jose M. Carmena, *Senior Member, IEEE*, Michel M. Maharbiz, *Senior Member, IEEE*, Elad Alon, *Senior Member, IEEE*, and Jan M. Rabaey, *Fellow, IEEE*

Abstract—Emerging applications in brain-machine interface systems require high-resolution, chronic multisite cortical recordings, which cannot be obtained with existing technologies due to high power consumption, high invasiveness, or inability to transmit data wirelessly. In this paper, we describe a microsystem based on electrocorticography (ECoG) that overcomes these difficulties, enabling chronic recording and wireless transmission of neural signals from the surface of the cerebral cortex. The device is comprised of a highly flexible, high-density, polymer-based 64-channel electrode array and a flexible antenna, bonded to 2.4 mm \times 2.4 mm CMOS integrated circuit (IC) that performs 64-channel acquisition, wireless power and data transmission. The IC digitizes the signal from each electrode at 1 kS/s with 1.2 μ V input referred noise, and transmits the serialized data using a 1 Mb/s backscattering modulator. A dual-mode power-receiving rectifier reduces data-dependent supply ripple, enabling the integration of small decoupling capacitors on chip and eliminating the need for external components. Design techniques in the wireless and baseband circuits result in over 16 \times reduction in die area with a simultaneous 3 \times improvement in power efficiency over the state of the art. The IC consumes 225 μ W and can be powered by an external reader transmitting 12 mW at 300 MHz, which is over 3 \times lower than IEEE and FCC regulations.

Index Terms—Brain, ECoG, EEG, implant, *in vivo*, low power, neural, recording, rectifier, wireless.

I. INTRODUCTION

IN ORDER to realize the vision of fully autonomous brain-machine interface (BMI) systems, neural implant devices must not only be effective in their function, but should also meet clinical constraints such as ease of implantation, longevity, safety, and small size. Substantial improvements in neural implant safety, longevity, and form factor are needed to translate existing multisite neural recording systems into technology suitable for long-term use in patients.

Table I shows the tradeoffs in commonly used neural recording modalities, particularly highlighting issues that affect clinical viability and information content relevant to the design of neural prosthetics. Until recently, the neuroscience community has largely focused on action potential (AP) recording as the modality of choice for BMI. Today, AP recording remains the highest resolution recording modality but comes at the price of tissue scarring in the brain, resulting in signal degradation over the course of several months [1]. The least invasive solution, electroencephalography (EEG), does not provide sufficient resolution for most BMI applications [2]. Electrocorticography (ECoG) is an electrophysiological technique where electrical potentials are recorded from the surface of the cerebral cortex. Since the implant does not pierce the cortex, ECoG has the potential for longer signal stability than AP recording [2]–[4] and provides a higher resolution signal than EEG. Furthermore, ECoG is commonly used in neurosurgical procedures to perform functional cortical mapping. Because of its lower invasiveness and higher longevity, ECoG is gaining popularity in a variety of BMI applications. However, today's clinical ECoG implants are large, have low spatial resolution (0.4–1 cm)¹ and offer only cumbersome wired operation.

In this paper, we describe a minimally invasive, 64-channel wireless ECoG microsystem [5] that overcomes these limitations and enables chronic and stable neural recording. All implantable components are placed at the surface of the cortex, reducing surgical complexity and enabling complete closure of the surgical site, greatly reducing the risk of infection. Wireless

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R. Muller is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA, and also with Cortera Neurotechnologies Inc., Berkeley, CA 94704 USA.

H.-P. Le is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA, and also with Lion Semiconductor Inc., Berkeley, CA 94720 USA.

W. Li is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA.

P. Ledochowitsch is with the Department of Bioengineering, University of California, Berkeley, CA 94720 USA and University of San Francisco, San Francisco, CA 94143 USA, and also with the Allen Institute for Brain Science, Seattle, WA 98103 USA.

S. Gambini is with San Francisco, CA 94103 USA.

T. Bjorninen is with Tampere University of Technology, FI-33101 Tampere, Finland.

A. Koralek is with the Hellen Wills Neuroscience Institute, University of California, Berkeley, CA 94720 USA.

J. Carmena is with the Department of Electrical Engineering and Computer Science and the Hellen Wills Neuroscience Institute, University of California, Berkeley, CA 94720 USA.

M. Maharbiz is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA USA, and also with the Department of Bioengineering, University of California, Berkeley, CA 94720 USA and University of San Francisco, San Francisco, CA 94143 USA.

E. Alon, and J. Rabaey are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

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¹[Online]. Available: www.adtechmedical.com

TABLE I
NEURAL SIGNAL COMPARISON



	EEG	ECoG	LFP	AP
Bandwidth	0.5-50Hz	1-500Hz	1-500Hz	250-10kHz
Amplitude	1-50 μ V	1-500 μ V	10 μ -1mV	10 μ -1mV
Spacing	3cm	0.2-10mm	0.1-1mm	0.1-1mm
Invasive	No	Craniotomy, no neural damage	Craniotomy, neural damage	Craniotomy, neural damage
Area Coverage	Whole Brain	\sim cm ² , whole brain	\sim mm ²	\sim mm ²
Stability	Decades	Decades	Years	Months

powering and readout are combined with a microfabricated antenna and electrode grid that has $>10\times$ higher electrode density than clinical ECoG arrays, providing spatial sampling of cortical function and volitional decoupling in BMI [4] approaching today's penetrating electrodes. Area and power reduction techniques in the baseband and wireless subsystem result in over an order of magnitude in integrated circuit (IC) area reduction with a simultaneous $3\times$ improvement in power efficiency over the state of the art. The low power consumption of the IC, together with the antenna integration strategy, enables remote powering at a power level three times lower than established safety limits [6], while the small size and flexibility of the implant minimizes the foreign body response.

This paper describes the design, fabrication, and characterization of the complete ECoG microsystem and focuses in detail on the design of the IC. The rest of this paper is organized as follows. In Section II, we introduce the μ ECoG system concept and discuss the advantages, challenges, and technologies involved in the realization of the system. Section III details the design of the IC, emphasizing designs that are key to miniaturization and power efficiency. Electronic and *in vivo* measurement results are described in Sections IV and V, respectively. Finally, conclusions will be given in Section VI.

II. SYSTEM ARCHITECTURE

A. μ ECoG System Concept

The wireless μ ECoG device pictured in Fig. 1 has four main components, given here.

- 1) A microfabricated, sub-mm resolution ECoG grid for neural recordings. The electrode grid is manufactured using only materials that have been approved by the FDA for chronic implantation, specifically, Parylene C (a class-IV bioimplantable polymer) and platinum. The 10 μ m thin Parylene C substrate has a Young's modulus $E = 2.75$ GPa, and is comparable in flexibility to 3.5 μ m thin Polyimide ($E = 7.5$ GPa). The grid is sufficiently flexible to conform to the highly folded cortical surface.
- 2) An IC capable of digitizing the voltage present on the electrodes and that integrates circuitry to receive power and

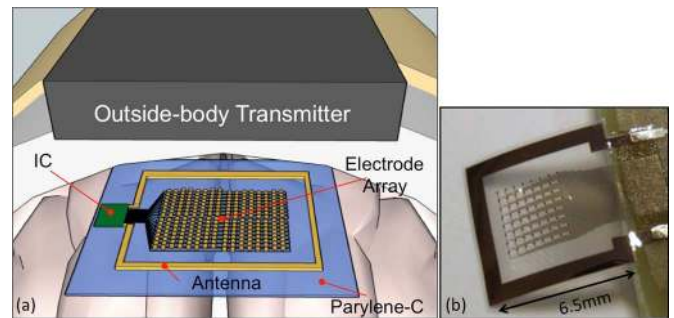


Fig. 1. (a) μ ECoG system concept. (b) Photograph of microfabricated components.

transmit the recorded signals wirelessly across the skull, removing the need for percutaneous plugs and cables.

- 3) An antenna that is monolithically integrated with the ECoG sensor grid and is used to couple wireless power and transmit data wirelessly across the skull.
- 4) An external reader that provides power to the implant and receives backscattered signals that are decoded into a data stream.

B. System Consideration: Microfabricated High-Density Electrodes

In the last decade, high-density micron-scale ECoG (μ ECoG) grids have gained increased traction among neurosurgeons for more precise mapping of seizure onset zones, eloquent cortex, and for clinical research [7], [8]. For a clinically relevant μ ECoG device, the overall form factor should meet the following conditions: 1) higher density than any μ ECoG available for clinical use (400 μ m electrode pitch, 8×8 channels); 2) sufficiently large area to be interesting for use in humans, e.g., for communication BMI [9] (4 mm \times 4 mm total area of the sensor array); and 3) sufficiently small that it can still be tested on the cortex of a rat (6.5 mm \times 6.5 mm total head size, including antenna). Fabrication of these μ ECoG grids using traditional manufacturing techniques has proven difficult. For example, Ad-tech Medical, the current market leader in clinical ECoG electrodes, had to recall μ ECoG arrays manufactured using microwires embedded in silastic pillars because of adverse reactions including seizures and hemorrhaging.² Informed by pioneering contributions [10] and [11], in 2011, we reported a multilayer large-area high-density μ ECoG (256 channels, 500 μ m electrode spacing) [12]. Parylene C was used as both substrate and insulator between conductive layers and employed a thermocompression-bonding paradigm to simplify interconnection. This technology is also used to realize the sensors used in this work.

1) *Wafer-Level μ ECoG Fabrication:* Fig. 2 shows cross-sectional diagrams of the individual processing. Parylene C (poly-para-chloro-xylelene, 5 μ m/layer) was conformally deposited onto a silicon carrier wafer. A stack of Pt-Au-Pt was electron-beam evaporated and patterned by lift-off. A second layer of parylene was deposited and vias were patterned in the parylene by oxygen plasma reactive ion etching (RIE). The above process

²See Class 1 recall notice: <http://www.fda.gov/medicaldevices/safety/listofrecalls/ucm342797.htm>

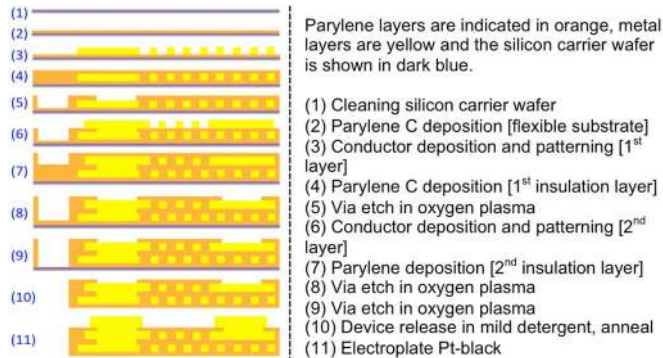


Fig. 2. Sensor and antenna fabrication in a cross section.

flow allows for devices that comprise multiple conductor layers. For device simplicity and robustness, the μ ECoG electrodes and antenna were patterned in a single layer by following steps 1)–5) in Fig. 2. Steps 6)–8) can be executed to achieve devices with more conductor layers at the expense of complexity. As a final step, a high-temperature (200 °C) anneal was performed in a nitrogen atmosphere to improve device lifetime [13], [14].

2) *Interconnection*: Bonding of metalized Parylene C devices to rigid structures can be a formidable challenge. Conventional solder bonds very poorly to platinum, and even if gold was patterned as the top layer of the metal stack, the metal-Parylene adhesion is not sufficient to robustly support the mechanical load. As a result, anisotropic conductive film (ACF) bonding utilizing a bench-top bonder was adapted to connect high-density ECoG grids with printed circuit boards (PCBs). A similar process can be adapted to perform direct chip-to-flex bonding.

The μ ECoG system uses a 4 mm \times 4 mm, 64-channel array. The electrodes have diameter 260 μ m and an electrode trace spacing of 20 μ m as shown on the right-hand side of Fig. 3. Platinum black is electrochemically deposited onto the electrodes, lowering their impedance and thermal noise contribution by approximately 1000 times resulting in an average electrode impedance of 10 k Ω at 100 Hz. The electrodes were sized as large as possible, allowing space for routing. Two reference electrodes are patterned on either side of the array to provide a good spatial average reference, and are sized with 64 times the area of an individual electrode in order to balance the electrode impedances and mitigate 60 Hz noise. In addition, the electrode diameter D_E and the electrode edge-to-edge spacing d obey the ‘‘Spatial Nyquist’’ condition $D_E > d/2$, acting as a spatial anti-aliasing filter [7] necessary for consistent spatial (spectral) pattern analysis of ECoG activity.

C. System Consideration: Microfabricated Antenna and Power Transfer

A thin film loop antenna is monolithically integrated with an array of neural recording electrodes on the parylene substrate. The antenna and electrodes were patterned in the same micro-fabrication process, on the same conductor layer. This integration strategy allows the system to utilize an antenna diameter that is significantly larger than the IC, but with the micron-scale thinness that provides a high degree of mechanical flexibility of

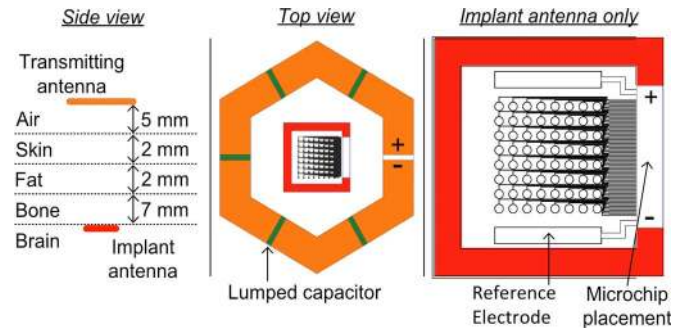


Fig. 3. Antenna/electrode diagram and simulation model [17].

the structure, thus keeping the volume of implanted rigid structures to a minimum. This is a significant advantage with respect to current state-of-the-art, which utilizes either small-diameter and inefficient on-chip loops [15] or large, rigid off-chip loops [16].

A single-loop antenna was chosen for the implant geometry for ease of fabrication with the electrodes in a single mask process. As described in [17], the ohmic loss in a 250 nm sub-skin-depth conductor is significant, making it favorable to use a single-turn geometry where the conductor length is minimal. The electrode grid dimensions determined the loop inner diameter of 5.8 mm. A gap is left on one antenna edge for microchip placement or routing of the electrode leads, as shown in Fig. 3. The loop trace width was optimized to minimize ohmic loss in the sub-skin-depth conductor due to current crowding. A width of 0.7 mm degrades the link gain by only 0.5 dB and was therefore chosen for this design. The loss can be reduced to 0.1 dB by increasing the width to 1.2 mm at the expense of metallization and implant area.

Simulations of the antenna pair were conducted with ANSYS HFSS to predict overall link power transfer efficiency. The simulation model is illustrated in Fig. 3. It consists of a layered tissue model of the human head with frequency-dependent dielectric properties given in [18], a single-turn loop implanted antenna enclosing the array of 64 electrodes, and an external transmit antenna. The external antenna utilizes a segmented-loop structure with series capacitors connecting each loop segment. This geometry forces the current in-phase and reduce electric-field hot spots that violate regulated limits on the Specific Absorption Rate (SAR) of human tissue, as described in [19]. Simulations show that a 15 mm external antenna diameter optimizes link gain between the antenna pair. The simulated link gain of the antenna pair is shown at the top of Fig. 4, with a local maximum at 300 MHz corresponding to a -15.5 dB unidirectional gain. Measured link gain versus simulated link gain is detailed in [17] and exhibits good agreement. At 300 MHz, the maximum RF power that can be transmitted safely into tissue (Fig. 4, center) is 35 mW, which is limited by the SAR of tissue and is regulated by the IEEE [6]. The corresponding maximum power available from the implant antenna is 800 μ W, which over 3 times greater than the power demands of the IC, leaving a safe margin to compensate the any additional loss due biological variability or implant misalignment by increasing the transmission power.

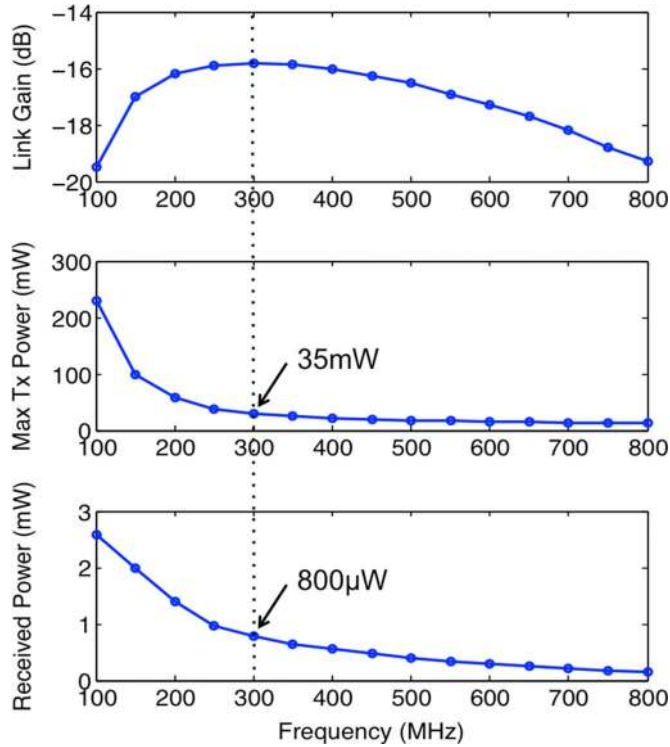


Fig. 4. Top: simulated link gain. Center: maximum allowable transmit power, Bottom: corresponding received power versus frequency.

III. INTEGRATED CIRCUIT

A. Chip Architecture

The IC is the core of the microsystem. This IC should be optimized for both low power consumption (to minimize the power transmitted by the reader and prolong its battery life) and area occupation. Since the IC is the only rigid component of the system, low area occupation is particularly critical. In addition, no external components other than the antenna and electrodes should be utilized, demanding innovative power conversion techniques to minimize the use of energy-storage devices.

A block diagram of the IC is shown in Fig. 5. The baseband signal acquisition consists of a 64-channel front-end array. Digital outputs of 1 kS/s, 16 bit are serialized into a 1 Mbps data stream. Wireless transmission is performed by modulating the impedance of an on-chip matching network in order to backscatter the incident RF to the external reader. The data stream is Miller-encoded prior to backscattering to minimize the effect of carrier leakage on bit-error rate (BER) in the interrogator. The power management unit (PMU) consists of RF-to-dc conversion, a low-dropout linear regulator (LDO) and a dc-to-dc converter [20], that provide 0.5 V and 1.0 V to the chip, respectively. Clock recovery and division are also implemented as part of the wireless subsystem. Design techniques in the front-end signal acquisition circuits and in the codesign of the power management/communication subunit are key to miniaturization and power efficiency and will be discussed in detail in this section.

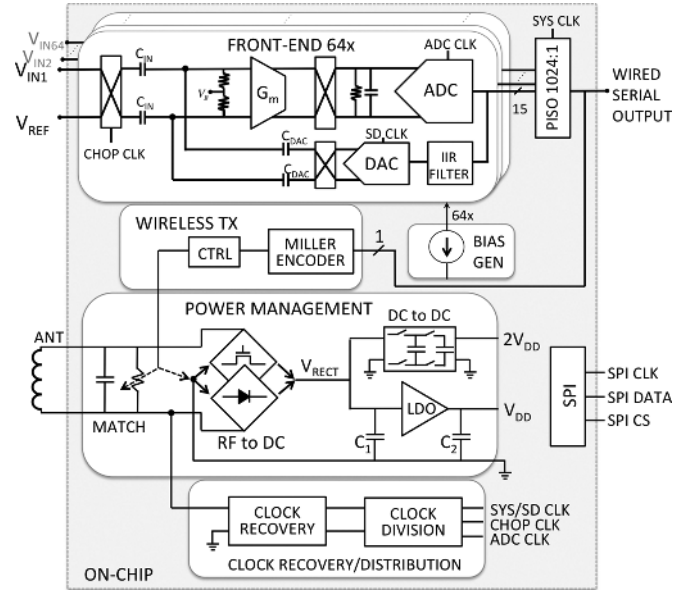


Fig. 5. Integrated circuit block diagram.

B. Neural Signal Acquisition

ECoG signals have low amplitudes of tens to hundreds of μ Vs and occupy a low frequency of approximately 1–500 Hz. The power spectrum of the signal exhibits a low-pass $1/f^N$, $N \sim 2$, profile. ECoG signals are commonly analyzed in the frequency domain. Higher frequency bands such as the high- γ (above 65 Hz) have low signal power, but are often the signals of interest when monitoring awake, sensorimotor activity [21]. In addition, a large dc offset of up to tens of mV, caused by electrochemical processes at the electrode/brain interface, can be present at the input. The front-end must amplify and digitize the small in-band signal in the presence of a large offset, while only introducing $\sim 1 \mu$ Vrms additional noise. Due to the low-frequency nature of the signals, mitigation of $1/f$ noise is vital to this end.

1) *State-of-the-Art and Proposed Architecture:* Several low-noise EEG/ECoG amplifiers have been reported in recent literature [22]–[25]. While good power efficiencies have been achieved [22], the resulting die area per amplifier in even the smallest implementations [24] makes arrays of more than eight amplifiers impractical, thus necessitating substantial reduction in die area. The state of the art has utilized chopped neural instrumentation amplifiers for this purpose, which can suffer from large area occupation for two reasons. In one implementation, the chopper switches are placed between the ac coupling capacitors and the input devices of the amplifier core. This causes the switched capacitor resistance introduced by chopping to realize a high-pass filter with the ac coupling capacitors themselves, demanding prohibitively large values of capacitance and area [25]. For example, for 10 kHz chopping frequency (f_{chop}) and 100 fF parasitic capacitance, input capacitors on the order of 1 nF/side are required to keep the high-pass pole below 1 Hz. In a second implementation, the chopper switches are placed before the input capacitors thereby upmodulating the offset together with the input signal. The upmodulated offset is

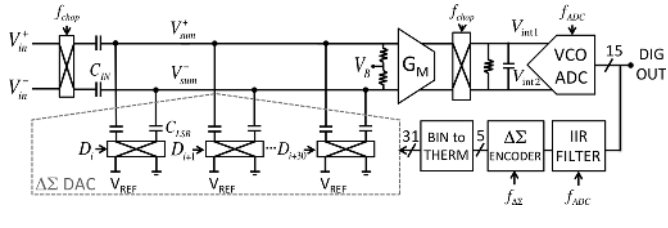


Fig. 6. Front-end architecture.

canceled in the high frequency domain by a feedback loop that tracks dc with an integrator and upmodulates its output [22]. Offset estimation is typically performed with analog integrators with unity-gain frequency of the order of 1 Hz or less, also demanding large capacitors.

The proposed architecture for the ECoG front-end is shown in Fig. 6 and is centered around a chopper stabilized, open-loop amplifier with mixed-signal feedback. Low-noise dc offset cancellation is performed prior to any amplification by a DAC built with passive components as opposed to transistors. The forward path is composed of a broadband instrumentation amplifier and a VCO-based ADC. The chopper switches are placed between the electrode and input capacitors, substantially reducing the area because these capacitors now act as summing rather than pole-setting elements. The capacitor sizes are therefore only limited by layout considerations and parasitic capacitance on the summing node.

As in [27], the feedback path is comprised of a digital accumulator and a DAC, which realize a servo loop that suppresses the offset and reduces the dynamic range requirement of the instrumentation amplifier and ADC cascade. The mixed-signal feedback loop takes the place of an analog integrator, allowing the large time constant necessary to cancel dc to be realized in a compact footprint using digital gates. The architecture in Fig. 6 holds many of the same advantages as the action potential architecture of [27] such as low area, programmability and per-channel digitization, which eliminates the complicated routing of analog signals at the top level. The efficient realization of this architecture presents a few new challenges that are discussed in detail in the following subsections.

2) *Mixed-Signal Feedback and DAC Design*: Open-circuit potentials in the hundreds of mV have been observed for platinum black microelectrodes in solution [28]. The dc resistance of our microfabricated ECoG electrodes were measured prior to electroplating through dc I - V curves and estimated to be on the order of hundreds of M Ω s (plated) to 10 s of G Ω s (unplated), therefore an input impedance on the order of M Ω s would diminish the offset to <10 mV. 100 mV (\pm 50 mV) of offset cancellation range was allocated to the system. To maintain signal swing in a low-supply-voltage environment the offset is cancelled with a DAC at the input of the first stage.

To suppress the quantization noise of the DAC well below the ~ 1 μ V thermal noise level, a DAC resolution greater than 17 bits is required. To save area, an oversampled, Delta-Sigma ($\Delta\Sigma$) modulated DAC is implemented. To prevent the $\Delta\Sigma$ noise from generating nonlinearity in the amplifier, we employ a 5 bit converter. This choice results in a signal swing at the input of ~ 3 mV, which is within the linear range of the input

stage and does not degrade the signal to noise ratio (SNR). With first-order $\Delta\Sigma$ modulation, an oversample ratio of at least 256 is required to achieve 17 bit resolution. The 1 MHz system clock provided by the clock recovery unit was chosen to clock the $\Delta\Sigma$ DAC since it simultaneously provided sufficient DAC resolution and occupied a sufficiently high frequency that the $\Delta\Sigma$ noise could be subsequently filtered with reasonable component sizes.

$\Delta\Sigma$ noise can further degrade the front-end SNR in two ways. First, band-limiting the $\Delta\Sigma$ signal prior to chopper downconversion will result in noise folding in-band. To prevent this, the amplifier must be broadband with respect to the DAC clock frequency. Second, the inherent filtering of the VCO-based ADC provides insufficient suppression of $\Delta\Sigma$ noise in this design. A single-pole filter is placed in the forward path after the downconversion chopper to provide additional anti-aliasing and to suppress signal amplitude at the input to the ADC, keeping the signal within the ADC linear range. Behavioral simulations show that a filter bandwidth of 50 kHz or smaller is sufficient to eliminate this error source.

The digital feedback has the same basic architecture as the one described in [27]. The integrator is clocked at a Nyquist rate of 1 kHz while the $\Delta\Sigma$ modulator is clocked at 1 MHz. The higher ADC resolution demands higher resolution and word lengths in the digital filter, growing the area occupation. The high forward path gain also necessitates a greater degree of signal attenuation in the feedback path in order to decrease loop gain and increase phase margin to maintain loop stability. A barrel shifter implements this attenuation with 12 bit tunability and serves to both stabilize the loop and to tune the location of the high-pass filter pole.

3) *Chopper Stabilization*: The front-ends utilize chopper stabilization to attenuate low-frequency interferers such as amplifier offset and $1/f$ noise [29]. One drawback to using chopper stabilization is that the switched-capacitor resistance degrades the input impedance of the amplifier. A significant advantage to using an open-loop architecture is that the effective input capacitance is reduced since the capacitors are not used to set low frequency filter pole locations. A simplified model of the in-band front-end input shown in Fig. 7(a). The input capacitance of the amplifier at each positive and negative input to ground is C_{IN} in series with $C_{DAC} + C_{PAR}$, where C_{PAR} is the parasitic capacitance on the summation node and is caused by bottom-plate capacitance, gate capacitance of the input devices and other layout parasitics. Since $C_{IN} \gg C_{DAC}$, the differential input resistance of the amplifier can be shown to be approximately

$$|Z_{in}| \approx \frac{1}{4f_{chop}(C_{DAC} + C_{PAR})}. \quad (1)$$

Since a high f_{chop} will degrade the input impedance, it is important to consider both capacitance and chopper frequency simultaneously. Z_{in} can be maximized in the following ways:

- 1) Minimize C_{DAC} : in this implementation the size of C_{DAC} is limited by the minimum sizing of a MIM capacitor, however, C_{DAC} cannot be arbitrarily small and should be significantly larger than C_{PAR} in order to not have its effect diminished. Therefore C_{DAC} is a function of C_{PAR} .

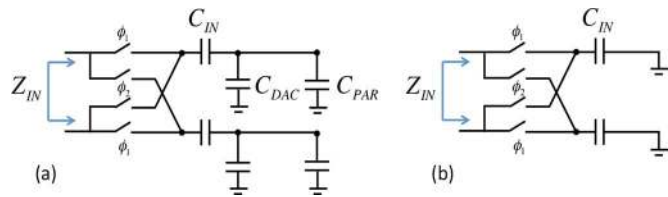


Fig. 7. Simplified circuit diagram of switched-capacitor resistance of the input chopper (a) in-band and (b) at dc.

- 2) Reduce f_{chop} : this can be achieved by selecting a type of amplifier input transistor with low $1/f$ noise spectral density ($S_{1/f}$), and by increasing the size of that device.
- 3) Minimize C_{PAR} : this can be achieved by selecting a type of amplifier input transistor with low gate capacitance and by decreasing the size of that device. Techniques 2 and 3 are seemingly at odds with each other; therefore in selection and sizing of the amplifier input device, the product of the $1/f$ noise spectral density and capacitance, $S_{1/f} \cdot C_{\text{PAR}}$, must be minimized. Standard threshold PMOS input devices were chosen in order to minimize this metric.

Unlike traditional chopper-stabilized feedback amplifiers, the switched-capacitor input resistance of the front-end is also frequency-dependent. At low frequency, the mixed-signal feedback loop becomes active, changing the impedance characteristics. Fig. 7(b) shows an equivalent circuit model for the input of the front-end at dc. The feedback loop tracks the dc voltage and cancels it at the summing nodes, creating a virtual ground. In this case, C_{IN} dominates the input impedance characteristics of the front-end and the input impedance becomes

$$|Z_{\text{in}}| \approx \frac{1}{2f_{\text{chop}}C_{\text{IN}}}. \quad (2)$$

Since $C_{\text{IN}} \gg C_{\text{DAC}}$, the dc input resistance will be significantly lower than the impedance in-band. This lower impedance helps to attenuate the dc offset present at the electrodes and stabilize the baseline.

4) *Circuit Design*: A 5 bit thermometer-coded charge redistribution feedback DAC is employed. Fig. 6 shows a simplified schematic of the DAC. Each unit capacitor C_{LSB} is minimum sized to minimize area and maximize impedance. The capacitors are implemented as metal-insulator-metal (MIM) capacitors with 5% relative matching, thus maintaining low DNL. In this implementation, $V_{\text{REF}} = 0.5$ V and is tied to V_{DD} . To cancel a full-scale voltage of 100 mV or 50 mV on each differential input $C_{\text{IN}} = 10C_{\text{DAC}}$, where $C_{\text{DAC}} = 31C_{\text{LSB}}$, and $C_{\text{LSB}} = 41$ fF. The summation nodes are biased (V_B) through a high-resistance pseudoresistor, which does not influence filter pole locations, minimizing the affect of pseudoresistor variation. Each unit cell of the feedback DAC is comprised of two capacitors C_{LSB} that are switched in opposite polarity at each phase of the chop clock. Since the chop clock guarantees switching at every cycle, the capacitors do not need to be explicitly reset. Thermometer-coded digital control bits, D, control the polarity of each unit cell modulating the amount of charge that is balanced by the DAC every time the chop clock changes.

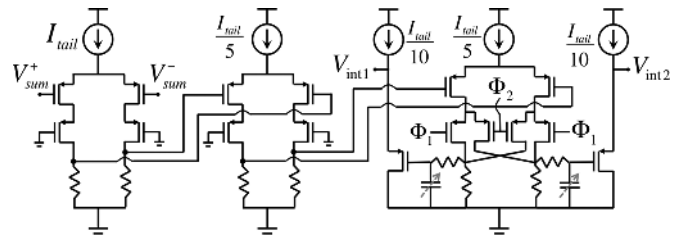


Fig. 8. Schematic of front-end chopper stabilized amplifier.

Since the input devices are PMOS, the amplifier input/summing junction is biased at low voltage, necessitating NMOS devices for the input chopper switches. One-volt gate drivers reduce the on-resistance and noise contribution of the NMOS input switches. The 1 V signal is generated by boosting the unregulated supply voltage with a switched-capacitor voltage doubler in the power management unit (PMU) and distributing the 1 V signal to each front-end.

The forward path amplification (Fig. 8) must be broadband compared with the signal, at least one to two octaves above the $\Delta\Sigma$ modulation frequency. In order to achieve more than 3 MHz of bandwidth in 1 to 2 μW of power, three cascaded low-gain stages were used. Each stage is comprised of a PMOS input differential pair, a PMOS cascode device to extend the bandwidth by decreasing the Miller capacitance at each input gate-drain junction, and a resistive load comprised of polysilicon resistors that provide good noise and linearity at the cost of increased die area. A tunable (from a broadband 3.3 MHz down to 40 kHz) single-pole filter is implemented to perform antialiasing and reduce the $\Delta\Sigma$ noise to be within the linear range of the ADC and is realized at the output of the third gain stage with the addition of tunable capacitance in parallel with the resistive load. Series resistance is added between the load resistor and the capacitor to reduce the low-pass filter pole without affecting the gain and output swing of the stage. The chopper down-modulation switches act simultaneously as cascode devices and current-domain modulation devices. Down-modulating in the current domain enables the seamless integration of a single-pole filter for filtering the $\Delta\Sigma$ noise. If the chopper switches were realized in the voltage domain at the output of the third stage, an additional buffer would be required to prevent the switched-capacitor resistance from affecting the gain of the stage.

5) *ADC*: The system employs a pseudo-differential, current-driven, ring-oscillator-based ADC as shown in Fig. 9. This architecture exhibits boxcar sampling, which prevents aliasing of the instrumentation amplifier noise [27], while also removing chopper ripple and suppressing $\Delta\Sigma$ noise. To take advantage of this effect, both f_{chop} and $f_{\Delta\Sigma}$ clock frequencies are placed at harmonic multiples of f_{ADC} where the nulls of the sinc transfer function eliminate chopper ripple and suppress $\Delta\Sigma$ noise, thereby eliminating the need for a ripple reduction loop and extensive anti-alias filtering.

In order to keep the quantization noise well below the thermal noise floor an ADC resolution of at least 12 bits is required. A 13 bit range is provided by each of the ring oscillators at 1 kS/s. Each oscillator is designed such that the minimum and maximum oscillation frequencies f_{min} and f_{max} satisfy $|f_{\text{max}} -$

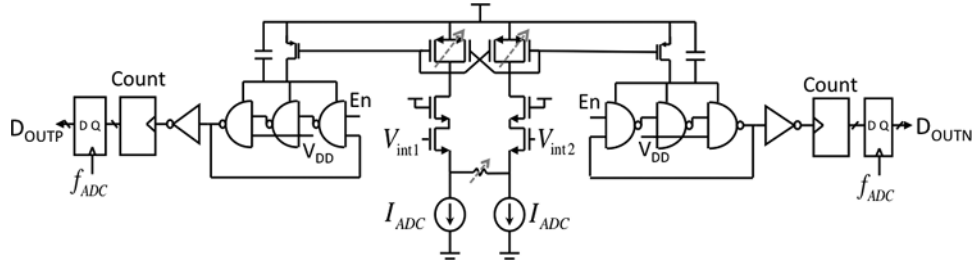


Fig. 9. Schematic of the VCO-based ADC.

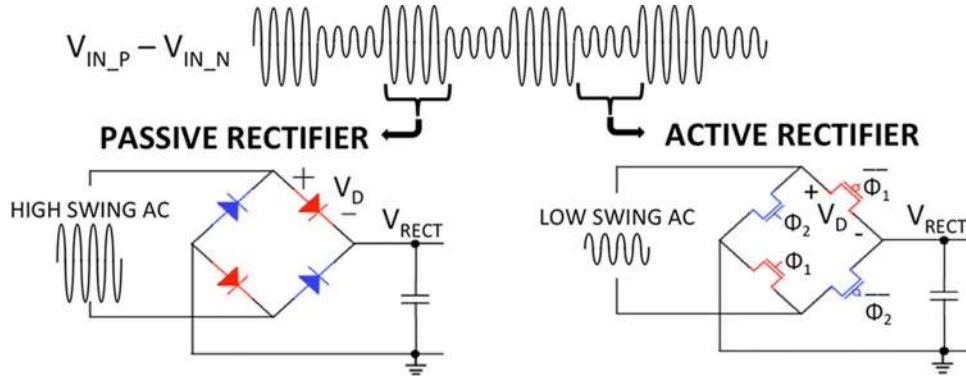


Fig. 10. Dual-mode RF-to-dc rectifier.

$f_{\min} > 2^{13}f_s$ with $f_s = 1$ kHz. The counters are not reset with each clock period and are allowed to wrap. Digital correction is implemented to unwrap the codes prior to subtraction. The driver consists of a differential-pair V-to-I converter cascaded with a current-mode programmable gain block as shown in Fig. 9. Variable degeneration resistors are used to further trade-off gain for linearity. Since chopping does not reduce the $1/f$ noise of this stage, all devices are sized with large area for the purpose of reducing the noise corner. $1/f$ noise of the ADC driver accounts for 2% of the total input-referred noise power when chopped at 8 kHz.

C. Wireless Subsystem

Similar to an implantable RFID tag, the wireless subsystem of the μ ECoG uses electromagnetic field backscattering to transmit data. However, rather than using packet-based communication, this system aims to be constantly powered and transmit a continuous stream of data. Architecting the system in this manner avoids the need for large on-chip power and data storage. In order to achieve this, communication modulation depth is traded for matching network impedance that is always finite and allows power to be rectified continuously. To illustrate this tradeoff, consider the amplitude of the reflected wave as a function of the matching network resistance and capacitance. The maximum modulation depth occurs when the load (Z_L) is modulated between matched impedance and either an open circuit or a short circuit, however, when the antenna is either in an open or short condition power cannot be received and rectified. In order to receive power continuously, the system is designed to modulate the impedance of the matching network between a matched condition and finite high impedance. While this results in a lower modulation depth, it

allows the incident RF to be received on-chip and be rectified at all times, resulting in continuous-wave power transfer with continuous data modulation.

Using the proposed modulation scheme, it is possible to extract power in both matched and unmatched states. However, as shown in Fig. 10, the two impedance modulation states lead to large voltage swing variation at the antenna terminals. If such a signal is fed to a conventional rectifier with constant voltage drop, it will cause a big voltage ripple in the output V_{RECT} . If a conventional backscatter modulator is used to transmit 1 Mbps data, there will be $1 \mu s$ intervals (i.e., corresponding to shorted antenna or symbol "0") in which no power is collected from the RF and the active circuitry is powered solely by the supply decoupling capacitor. For example, maintaining 1 mV of ripple while drawing $300 \mu A$ for $1 \mu s$ requires an impractical 300 nF capacitor. On the other hand, if a single rectifier and LDO are used, the LDO would need to attenuate the V_{RECT} ripple of ~ 200 mV down to 1 mV necessitating >40 dB input noise rejection at 1 MHz, which undesirable in this system due to its power consumption. In the μ ECoG system, a dual-mode rectifier is used to smooth the voltage at V_{RECT} and mitigate the need for a large capacitor or a high-performance LDO. The dual-mode rectifier efficiency (voltage drop) is modulated inversely to the data modulation and therefore the available input power (input voltage swing), in order to maintain a constant output power (constant output voltage at V_{RECT}). This technique reduces the ripple by a factor of 10 at V_{RECT} when compared to a single active rectifier and is exploited to reduce the supply decoupling capacitance to 4 nF, eliminating the need for external capacitors.

1) *Dual-Mode Rectifier*: The dual-mode rectifier, shown in Fig. 10, is composed of a passive rectifier and an active rectifier connected in parallel. The passive rectification mode

operates during the high impedance modulation state when the antenna voltage swing is high. In this mode, the rectifier drops a higher voltage across four diode-connected transistors. During the matched impedance modulation state when the antenna voltage swing is low, the system uses the active rectification mode, implemented with synchronous switches that have small voltage drops. The inverse relationship between input swing and voltage drops over the dual-mode rectifier smooths the output voltage ripple at V_{RECT} and eliminates the need for a large output capacitance. The following section will describe design considerations for each rectification mode.

Passive Rectification Mode: In order to reduce ripple by rectifier mode switching, the rectifier voltage drop V_D is controlled so that it satisfies the condition $V_{LOW-SWING} - V_{D_ACTIVE} = V_{HIGH-SWING} - V_{D_PASSIVE}$. In this design, the passive rectifier utilizes diode-connected NMOS transistors whose sizes are scalable with seven binary-coded bits to satisfy the equation above in presence of process variations. Calibration can be automated in future designs through an on-chip feedback loop that minimizes V_{RECT} ripple magnitude in real time.

Active Rectification Mode: Since the active rectifier operates on low-input RF voltage and therefore requires high rectification efficiency, which is achieved using a synchronous switching architecture. Conventionally, in order to control the timing of these power switches, a continuous-time comparator is used to detect the voltage different across the drain and source of a power transistor as shown in Fig. 11 [30]. In operation, when V_{IN_P} (or V_{IN_N}) crosses V_{RECT} , the comparator turns the power switch on or off to rectify the input current to the dc load. The power consumption of the comparators is quickly offset by the increased efficiency in applications utilizing a low carrier frequency and high output power. However, our system requires rectification at 300 MHz while delivering less than 200 μ W. While the main power switches need to operate at 300 MHz, any effort to reduce the switching power of any other circuit is desirable. The self-driven synchronous rectifier shown in Fig. 11 [31]–[33] takes advantage of the antenna terminal signals to drive the four transistors, leading to minimal switching power. However, since the turn-on/off timing of the switches depends only on the transistor threshold and the RF input amplitude, this rectifier imposes a specific requirement for the input RF signal to achieve high efficiency. For example, with a 1.0 V_{ptp} RF input, a 0.8 V output, and a 0.5 V threshold, rectifier efficiency can be degraded due to reverse current caused by switch early turn-on at 0.5 V every cycle.

2) *Clock-Retimed Strong-Arm Comparator:* In order to enable a high-efficiency active rectifier with flexibility in choosing the input RF power and swing, it is desirable to design a rectifier in which the switches are operated based on the cross-point of the RF signal V_{IN_P} and V_{RECT} , but with minimal power spent on this cross-point detection circuit. Since the input signal from the antenna is repetitive, it is unnecessary to detect the cross at every cycle of $V_{IN_P} - V_{RECT}$. While rectifying switches of the active rectifier still operate at the RF frequency, the cross detection can be triggered at a lower speed (once every 8 RF clock cycles in this design) to save power. Using this technique, we can decouple the speed (power) and accuracy requirements

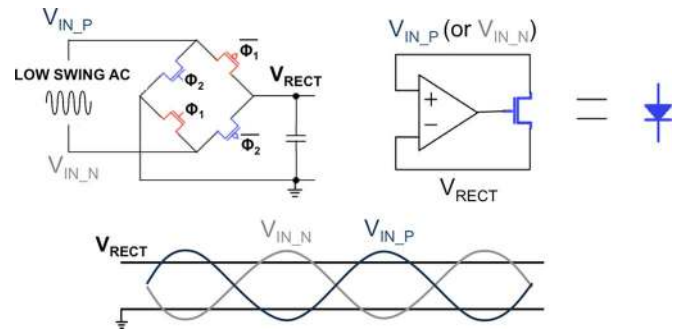


Fig. 11. Conventional implementation of a synchronous rectifier.

of the cross-detection comparator. As shown in Fig. 12, the active rectifier utilizes two mixed-signal feed back loops to control the timing of the synchronous switches and prevent reverse conduction. One loop controls the timings of the gate signal including the turn-on delay t_{D1} and the other manages the ON period t_{D2} . The turn-on time delay t_{D1} (the ON period t_{D2}) loop consists of current-starved delay cell t_{D1} (t_{D2}), integrator INTGR1 (INTGR2) and Φ_1 switch drivers and clocked comparator COMP1 (COMP2). The current-starved delay cell t_{D1} also serves as the RF clock recovery unit. In operation, comparator COMP1 (COMP2), triggered by the gate signal Φ_1 (Φ_1 plus a t_{D2} delay), detects and controls the t_{D1} (t_{D2}) loop to zero the difference between V_{IN_P} and V_{RECT} at the turn-on and turn-off instant of the Φ_1 signal. Since V_{IN_N} and V_{IN_P} are the same signals with 180° out of phase, the same loop can be used to generate t_{D1} and t_{D2} for the Φ_2 signal.

The comparators COMP1 (COMP2) are clocked at $1/8$ th of the carrier frequency Φ_1 ($\overline{\Phi_1}$) and cut the total switching power of the rectifier peripheral circuits by a factor of 3. Although the comparators are clocked at a slower rate, the switching must still be triggered by the high frequency gate signal Φ_1 ($\overline{\Phi_1}$) in order to have an accurate $V_{IN_P} - V_{RECT}$ cross detection. Accurate cross detection is obtained by using a clock-retimed Strong-Arm comparator architecture shown in Fig. 13 and requires retiming of the low frequency comparator clock CLK ($CLK + t_{D2}$) to Φ_1 ($\overline{\Phi_1}$). To enable this feature, the tail clock switch of the Strong-Arm comparator is modified with two series switches M1 and M2, where M1 is clocked by CLK ($CLK + t_{D2}$), and M2 is driven by Φ_1 ($\overline{\Phi_1}$). As shown in the timing diagram in Fig. 12, this configuration allows the comparator to operate at low frequency but to be triggered at the time that the power switches are on. A keeper, comprised of switch M3 and inverter INV1, is added to the tail node to ensure that the node stays low even as Φ_1 ($\overline{\Phi_1}$) is switching. A pre-charge switch is added to the tail to ensure that the inverter does not sink crowbar current during the pre-charge phase.

IV. MEASUREMENT RESULTS

The chip was fabricated in a 65 nm low-power CMOS process with one polysilicon and seven metal layers from STMicroelectronics. A chip microphotograph is shown in Fig. 14. The chip contains 64 integrated front-ends and one stand-alone front-end test block. Power conversion and management, wireless transmission, clock recovery and division

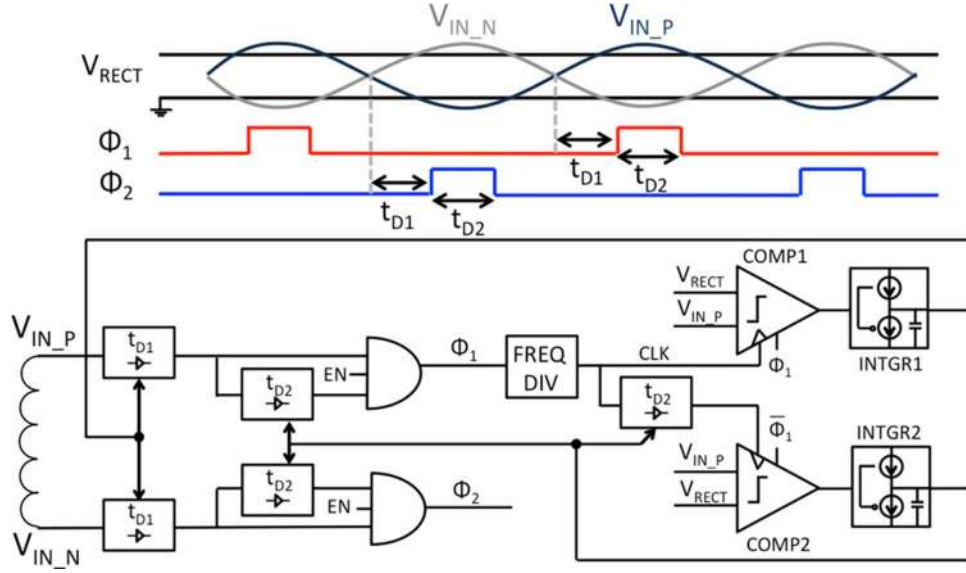


Fig. 12. RF-to-dc rectifier gate driver circuit and timing diagrams.

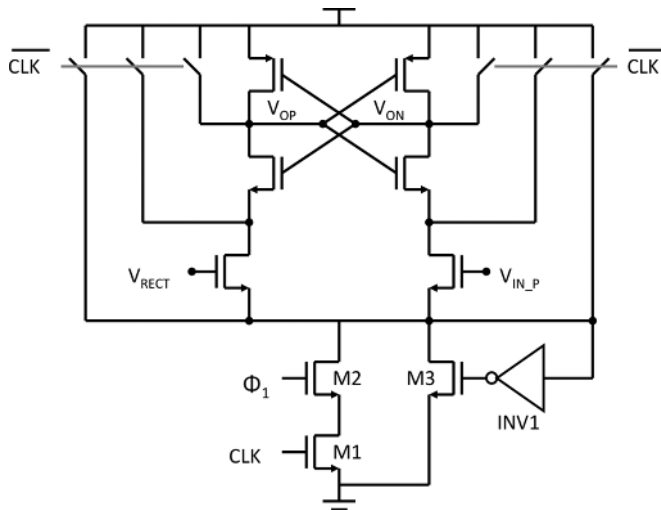


Fig. 13. Schematic of modified Strong-Arm comparator COMP1.

as well as bias circuitry are all integrated on the die. Table II summarizes the overall system performance. The total chip area is pad-limited to $2.4 \text{ mm} \times 2.4 \text{ mm}$, while the active area of the circuits is 1.72 mm^2 . The area and power consumption of IC are dominated by the 64 front-ends, which consume $2.3 \mu\text{W}$ and 0.025 mm^2 each. Table III lists the power and area breakdowns by block.

A. Neural Signal Acquisition

Electrical characterization of the front-ends was performed on a test-PCB with an Opal Kelly FPGA interface. All measurements were performed through the full acquisition channels including the on-chip ADCs. Unless otherwise noted, all measurements were performed with $f_{\text{chop}} = 8 \text{ kHz}$ and the low-pass filter bandwidth set to 40 kHz . Post-processing of the digital outputs was performed using MATLAB. Differential sine-wave inputs were produced using a Stanford Research Systems low-dis-

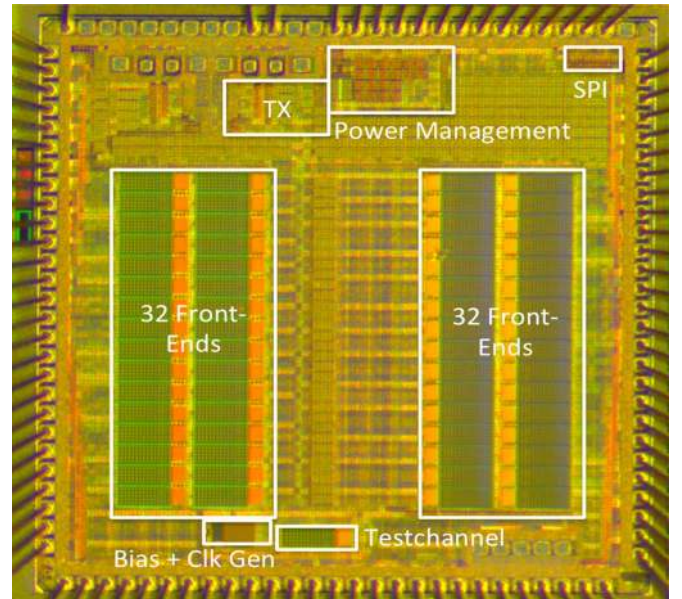


Fig. 14. Die microphotograph.

tortion signal generator and attenuated to proper input levels at the acquisition channel input.

Fig. 15 shows an oscilloscope capture of the analog waveform at the input of the ADC from a $1 \text{ mV}_{\text{ptp}}$ input with zero input offset. The analog signal exhibits chopper ripple after down-modulation as a result of amplifier offset. Superimposed on the chopper ripple is the $\Delta\Sigma$ signal. With a filter bandwidth of 50 kHz , the total amplitude of the two signals is 60 mV after amplification and is in addition to the gained up analog output waveform. The corresponding ADC output waveform is also shown in the figure. It is clear from visual inspection that the ADC filters the majority of both the chopper ripple and the $\Delta\Sigma$ noise. The remainder of this section will quantify the front-end performance.

TABLE II
SUMMARY OF SYSTEM PARAMETERS AND PERFORMANCE

SYSTEM PARAMETERS	THIS WORK
Sensors and Recording	
Electrodes	Thin film Pt/Au on Parylene C
Electrode grid thickness	10 μm
Electrode pitch	0.5 mm
Total chip area	2.4 mm x 2.4 mm
Number of channels	64 simultaneous
Integrated or Discrete	Integrated, no external components
Wireless Communication and Power	
Implanted antenna diameter	6.5 mm
External antenna diameter	1.5 cm
Communication distance	Transcranial, 12.5 mm
Carrier frequency	300 MHz
Data encoding scheme	Miller
Bit error rate	< 1.7E-7
Link gain	-16.5 dB, simulated
Transmit power	13 mW
Received power	225 μW
Power conversion efficiency	70%

TABLE III
IC POWER AND AREA BREAKDOWNS BY BLOCK

	Area (mm^2)	Power (μW)
64 Front End Array	1.6	147.2
Tx & Encoder	0.015	2.4
Clock Recovery	0.012	10.6
Power Management	0.09	64.1
Total	1.72	224.3

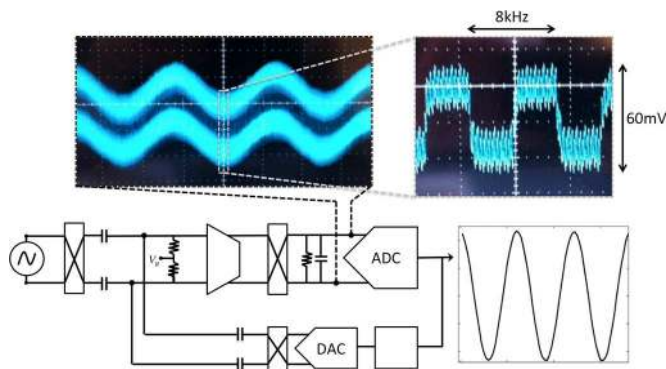


Fig. 15. Oscilloscope capture of analog input to ADC and corresponding measured output of ADC from a 1 mV_{ptp} sine-wave stimulus.

The measured closed-loop transfer functions of the ECoG front-end from the input to the ADC output are shown in Fig. 16. The transfer function exhibits a first-order (-20 dB/decade) high-pass filter profile with a pole that is digitally programmable in the feedback loop. The analog gain prior to analog to digital conversion is 30 dB. As a result of open-loop amplification, channel-to-channel gain mismatch was measured to be 15%, which was then calibrated upon startup by forcing a common

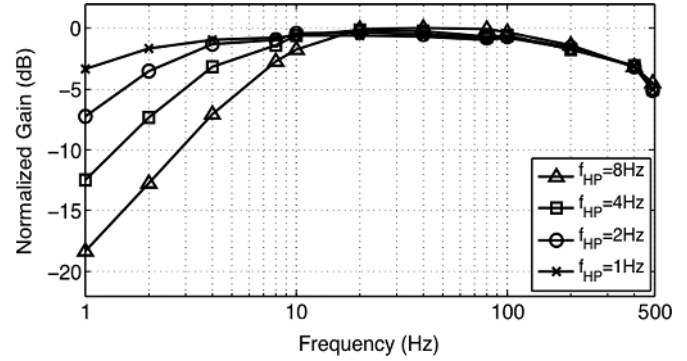


Fig. 16. Front-end closed-loop transfer function, digital feedback path tunes the high-pass filter pole.

signal at the input of all channels, storing the output digital codes, and normalizing the gains in the digital post-processing step. In this prototype, the test signal used for calibration was not generated on chip, but can be implemented in future generations (i.e., by modifying the feedback DAC). Fig. 16 shows transfer functions for four programmed states with poles at 8, 4, 2, and 1 Hz. The high-frequency roll-off is due to the sinc transfer function of the ADC [27].

Fig. 17(a) shows the normalized measured output spectrum of the acquisition system for a $0.5 \text{ mV}_{\text{ptp}}$ input sine wave at 40 Hz. The signal power is normalized to the peak power. At this input level no harmonic tones are visible above the noise floor. With the input amplitude increased to $1.0 \text{ mV}_{\text{ptp}}$, second and third harmonic tones are clearly visible in the spectrum [Fig. 17(b)]. At this input range, the complete system, including the ADC, exhibits an SFDR of 52 dB and a total harmonic distortion (THD) of 0.4%.

The input-referred noise spectral density (NSD) is plotted in Fig. 18. The NSD is plotted for a range of chopper frequencies as well as for the open-loop system with chopping disabled. In the absence of chopper stabilization, the NSD of the amplifier is dominated by $1/f$ noise that is more than two orders of magnitude larger than the thermal noise floor. Integrated over the bandwidth, the noise of the amplifier without chopper stabilization would be $570 \mu\text{V}$. The large integrated noise is a result of small device size and susceptibility to interferers such as 60 Hz noise, which impact the measured noise performance. The chopper stabilized closed-loop system reduces the $1/f$ noise corner to between 100–200 Hz. The measured input-referred noise, integrated over the 500 Hz bandwidth, is plotted vs. f_{chop} in Fig. 19 and shows good agreement with simulated values. Higher values of f_{chop} lower the $1/f$ noise corner frequency and reduce total input-referred noise, however, chopping beyond the $1/f$ noise corner of the devices results in a diminished return in noise performance [29], while still degrading input impedance. For this design, a chopper frequency of 8 kHz results in an optimal tradeoff for this design. For $f_{\text{chop}} = 8 \text{ kHz}$, the noise efficiency factor (NEF) of the entire front-end, including power dissipated in the ADC is 4.76 and the corresponding power efficiency factor (PEF) [27] is 11.3. The amplifier alone consumes $1.4 \mu\text{W}$. Assuming all the system input-referred noise was generated by the amplifier (in reality the noise would be less), the NEF of the amplifier alone becomes 3.7 and

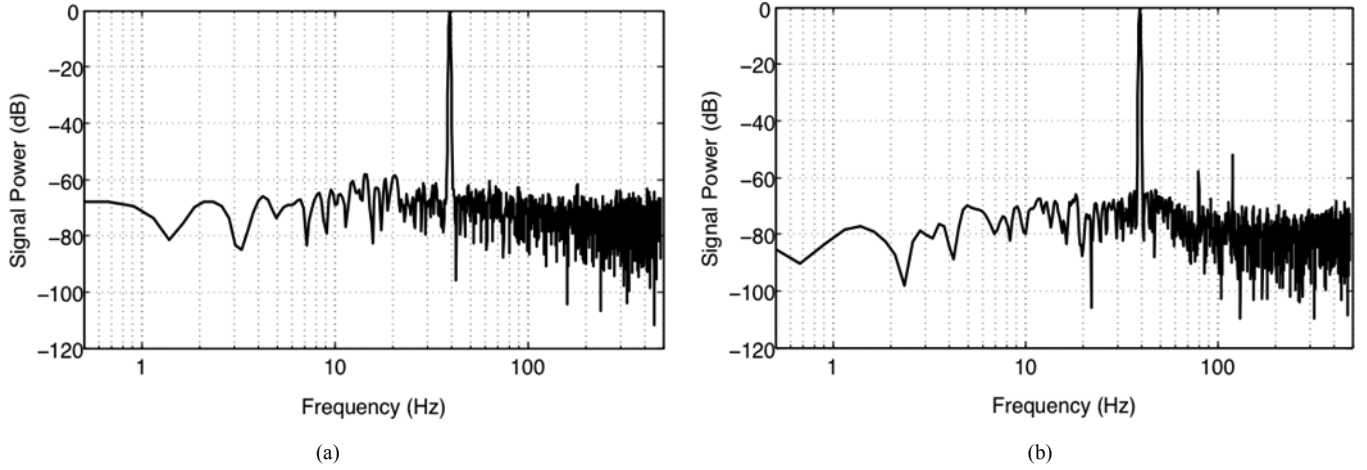


Fig. 17. Power spectral density of output waveform with (a) 0.5 mVptp and (b) 1 mVptp sinusoidal input voltage.

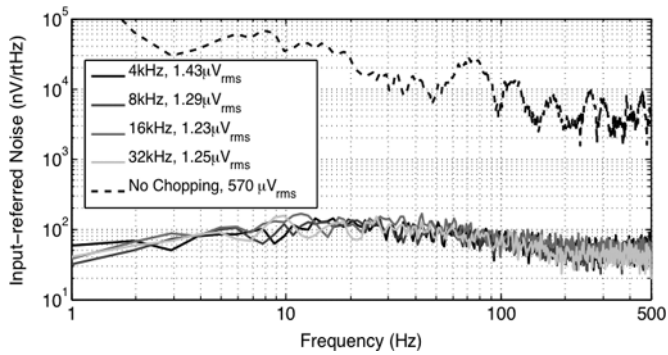


Fig. 18. Input-referred noise power spectral density across a range of chopper stabilization frequencies.

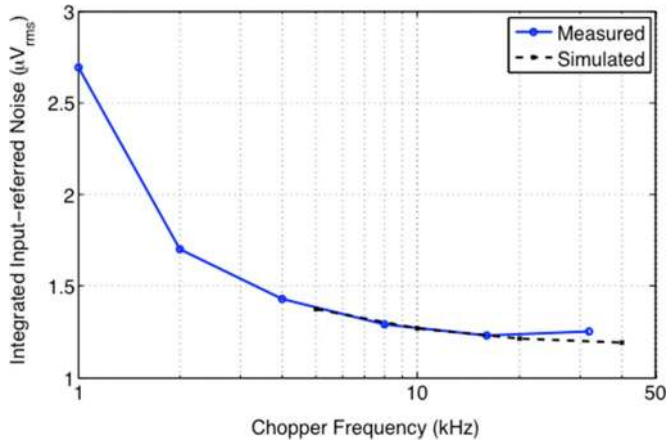


Fig. 19. Integrated input-referred noise as a function of chopper frequency.

the corresponding PEF is 6.9. No impact in noise performance was observed when the chip was wirelessly powered.

Input impedance was measured for all possible values of f_{chop} and plotted in Fig. 20. The measurements were made at dc and at 100 Hz (designated “in-band”). According to (1) and (2), at 8 kHz the calculated input impedances at dc and in-band are 4.9 and 25 M Ω respectively. The measured impedance shows good agreement with calculation and stays constant to within

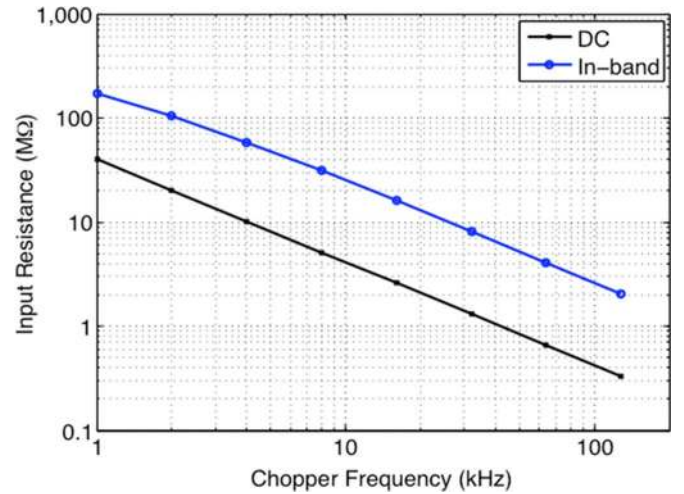


Fig. 20. Input resistance versus chopper frequency for dc and in-band signals.

5% across all offset values. The full-scale range of the DAC was measured and found to be able to cancel a total of 98.6 mV (-49.1 to $+49.5$ mV).

The common-mode rejection ration (CMRR) and the power-supply rejection ration (PSRR), each measured at 60 Hz, were measured for the complete system in feedback with $f_{\text{chop}} = 8$ kHz. CMRR was measured to be 88 dB. With the inputs grounded the PSRR was measured to be 67 dB. The measured PSRR and CMRR remained stable over a range of dc offsets applied at the input. PSRR can be improved by decoupling the DAC reference from V_{DD} . Channel-to-channel crosstalk was measured at the output of all channels when stimulating a single channel with a 100 mV_{ptp} in-band input while the inputs to all other channels were grounded. The measurement was repeated for multiple separate channels. A worst-case crosstalk of -85 dB was measured at the output of the adjacent channels.

B. Wireless Subsystem

The wireless data and power measurement setup is illustrated in Fig. 21. The transmit antenna is spaced in air 10 mm away

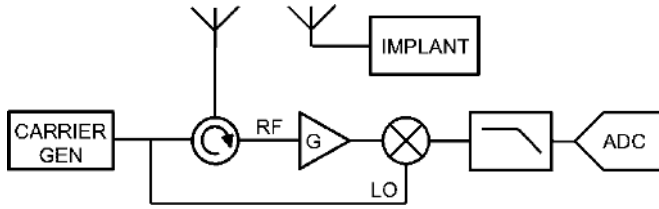


Fig. 21. Wireless measurement setup.

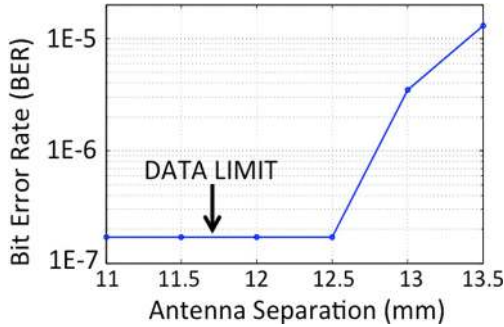


Fig. 22. Wireless transmission bit error rate versus antenna separation.

from the implant antenna. The implanted antenna was measured to have a $Q = 1.2$, a resistance of 67Ω , and an inductance of 32 nH . The interrogator/external reader is built from off-the-shelf components, a custom segmented loop antenna, and test equipment. Segmenting lumped capacitors with low series resistance ($50 \text{ m}\Omega$) were used to resonate out the inductance of each segment at 300 MHz . An Agilent E4438C ESG Vector Signal Generator is used to output a 300 MHz continuous wave at 11 dBm power. The transmit antenna is matched to have a S_{11} of less than -12 dB . A directional coupler is used to differentiate the back-reflected data wave from incoming wave. After amplification, the RF signal is converted to baseband using the I-Q function of an Agilent N9010A EXA Signal Analyzer. The maximum decoded data length is 6 MB , limited by the capture memory of the signal analyzer. The performance of the wireless link is verified by wirelessly transmitting a PRBS-7 data pattern generated on-die. Zero errors were found in 6 Mb of data resulting in a $\text{BER} < 1.7\text{E}-7$ both in air and *in vivo*. Robustness of the link was verified by varying the link distance and zero errors were found up to 12.5 mm in air, as shown in Fig. 22. For a constant transmit power, BER degrades with increased link distance, until a clock can no longer be recovered from the incident RF (14 mm of antenna separation at 11 dBm).

The PMU subblocks, including the dual-mode rectifier, switched-capacitor step-up dc-dc and LDO, are also verified in experiment. Fig. 23 shows the voltage waveform at the rectifier output attenuated $\sim 20\times$. The measurement demonstrates that switching from using a single active rectifier to using a dual-rectifier reduces V_{RECT} fluctuation by ten times. The PMU delivers $160.2 \mu\text{W}$ from $\sim 225 \mu\text{W}$ from the implant antenna. The $\sim 70\%$ total efficiency is the series combination of the dual rectifier ($\sim 84\%$ efficient) and LDO ($\sim 82.5\%$ efficient).

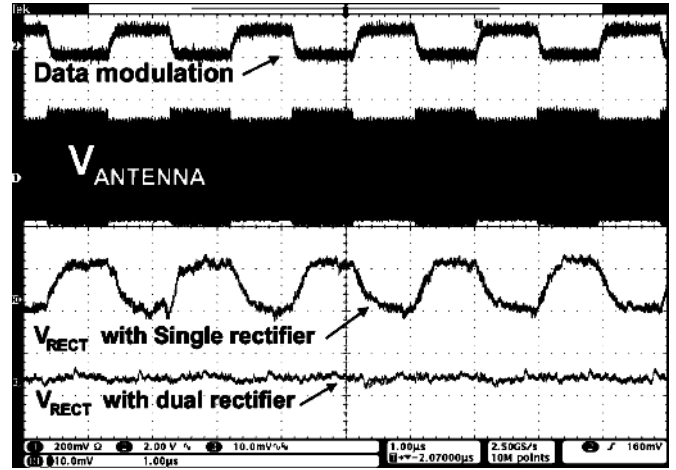
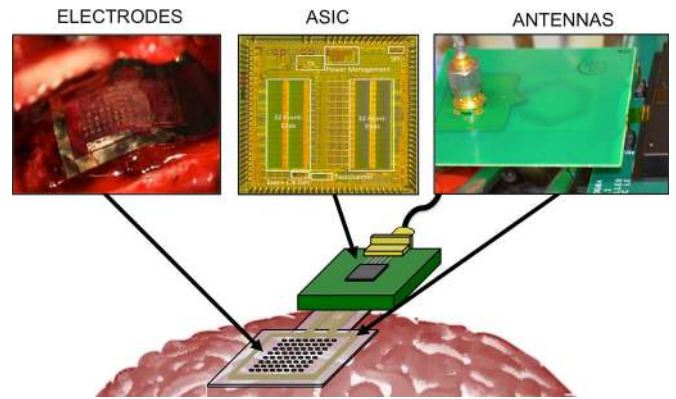


Fig. 23. Power rectifier measurements.

Fig. 24. *In vivo* test setup.

C. Comparison With the State of the Art

Table IV summarizes the performance of the μECoG front-end as compared to state-of-the-art designs from industry and academic researchers [22]–[26]. Limited work has been published on ECoG designs, therefore this work is compared also to EEG front-ends, which have a similar set of specifications. State-of-the-art noise efficiency is achieved, and, together with a reduced power supply, this work achieves the lowest reported PEF, 3 times lower than state-of-the-art [22]. The small area enables the highest degree of integration achieved to date in low-frequency high-precision bio-signal acquisition with a 64-channel array in only 1.6 mm^2 of active silicon area and no external components required.

V. *In Vivo* MEASUREMENTS

A. Experimental Setup

The complete system was verified through *in vivo* experimentation in a live rodent. The IC was assembled together with the microfabricated ECoG electrodes and antenna on a PCB and implanted in an anesthetized Long-Evans rat. All experiments

TABLE IV
COMPARISON OF COMMERCIAL AND RESEARCH ECoG AND EEG FRONT-ENDS

	[20] JSSC '07	[21] JSSC '08	[22] TCAS, '11	[23] JSSC '10	[24] Intan RHD2000	THIS WORK
V_{DD} (V)	1.8	3.0	1.2	1	3.3	0.5
Power (μ W/ch)	2	33.3	3.24	6.5	100	2.3
IRNoise (nV/rtHz)	100	60	85	130	-- ^c	58
NEF	4.6	4.3	5.38	9.37	--	4.76 ^a
PEF	38.1	55.5	34.7	87.8	--	11.3 ^a
R_{IN} (M Ω)	8	1000	4	700	13	28
Max Input Offset (mV)	+/-50mV	45mV	0mV	--	+/-400mV	+/-50mV
CMRR (dB)	100	120	80	60	82	88
PSRR (dB)	--	--	60	--	75	67
THD	0.1% (5mVptp)	1% (1.65Vptp)	--	--	0.1% (4mVptp)	0.4% (1mVptp)
Area (mm ² /ch)	0.8	0.5	0.4	0.6	0.5 ^b	0.025
ADC Resolution	none	11-bit	none	12-bit	16-bit	15-bit
# of Channels	1	8	1	1	32	64
Crosstalk (dB)	N/A	--	N/A	N/A	-68	-85
Technology	0.8 μ m	0.5 μ m	0.13 μ m	0.18 μ m	--	65nm
Wireless	No	No	No	No	No	RF Power 1Mbps Tx
Off-chip components	No	No	Input Filter	Coupling Caps	Decap	No

^aincludes ADC

^bestimated

^clow-frequency noise not reported

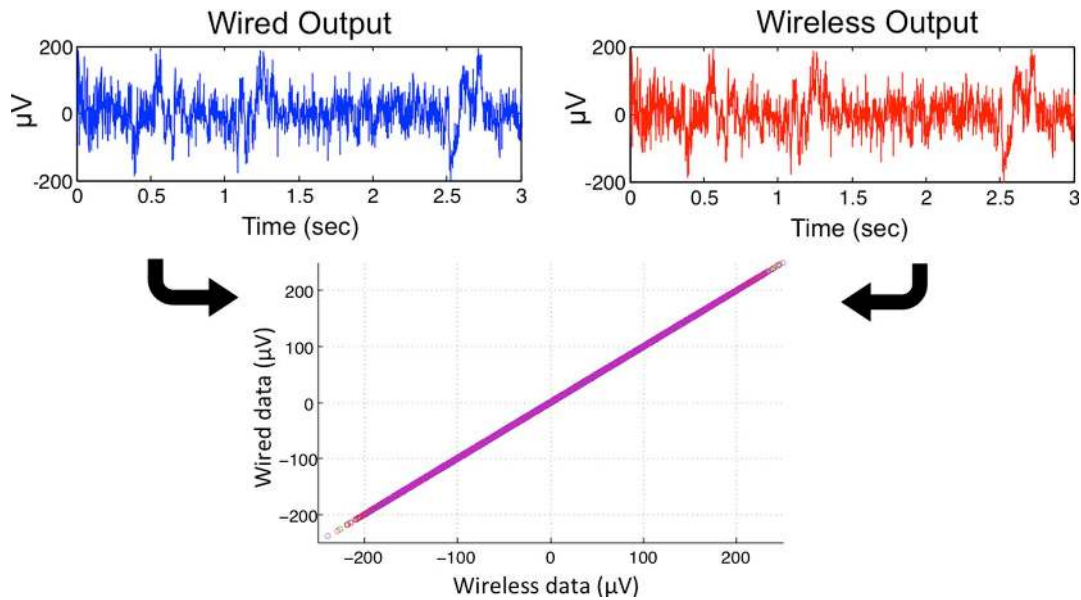


Fig. 25. Scatterplot of wired and wireless data taken *in vivo* showing zero errors between the two data sets.

were performed in compliance with the regulations of the Animal Care and Use Committee at UC Berkeley. Rats were implanted with μ ECoG grids over the left cortical hemisphere. The surgical setup is pictured in Fig. 24. The ECoG grid was lowered onto the cortical surface using micromanipulators, which suspended the PCB in the air above the head of the rat as shown in the upper left of the figure. The external reader antenna was then suspended 10 mm over the implant site as shown in the upper right.

B. Measurement Results

Recordings of microstimulation pulses from a sub-cortical tungsten microwire array were used to confirm simultaneous 60-channel recording. Four inactive channels resulted from poor ACF bonding yield of the flexible array to the PCB. The wireless link was confirmed *in vivo* with a BER test. Zero errors were detected in over 6 Mb of data at a rate of 1 Mbps and an antenna separation of 1 cm, with the external antenna transmitting

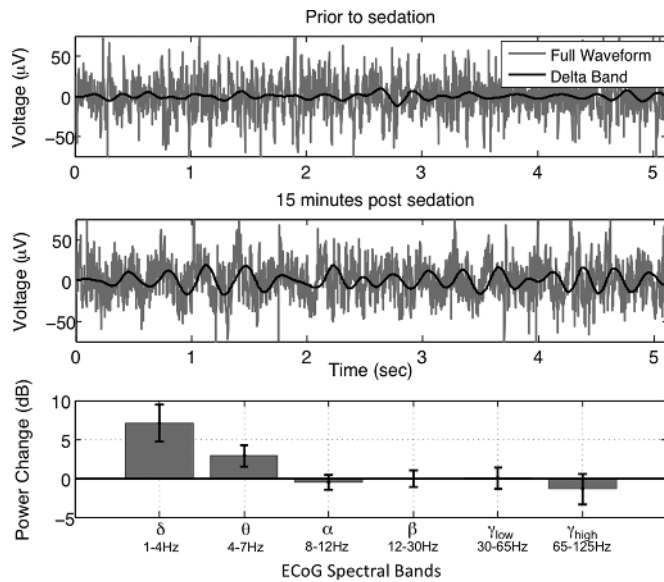


Fig. 26. *In vivo* recordings from a single channel before and 15 min after sedative administration; spectral band power changes are plotted for all channels.

11 dBm. With the entire system active and wirelessly powered, cortical surface potentials from all electrodes were recorded simultaneously through the wired readout and through the wireless link, limiting the data capture length to 3 Mb. A scatterplot, shown in Fig. 25, of the two data sets plotted against each other show zero errors in over 3 Mb of data.

An experiment was performed to monitor the level of sedation of the anesthetized rodent. Electrical recordings of subdural cortical surface potentials were made on all channels prior to and 15 min after the administration of Pentobarbital, a sedative. Oscillations in the δ -band (1–4 Hz) and θ -band (4–8 Hz) are commonly observed in deep and moderate anesthetic states, respectively, while high- γ (60–125 Hz) activity correlates well with awake sensorimotor functions. It is known that anesthesia causes increased δ band oscillations and depressed high- γ activity [34]. Fig. 26 (top) shows a recorded waveform of a representative channel and the filtered δ band activity of that waveform plotted together prior to sedative administration. Fifteen minutes after the administration of the sedative, a distinct increase in δ -band activity is clearly visible (Fig. 26 (center)). All relevant ECoG spectral band-powers across all electrodes are plotted in Fig. 26 (bottom). An average of 7 dB increase in δ -band power and a 2 dB decrease in high- γ activity is observed, consistent with published neuroscientific results [34].

VI. CONCLUSION

We have presented a 64-channel wireless ECoG microsystem. Area and power reduction techniques in the baseband and wireless subsystem result in over an order of magnitude in IC area reduction with a simultaneous $3\times$ improvement in power efficiency over the state of the art, enabling, for the first time to our knowledge, a 64-channel recording platform that can be chronically implanted and powered well within established IEEE limits, and occupying a compact, mm-scale form factor. The system was fully verified and characterized electronically and *in vivo* through implantation in a live rodent.

The improved implant safety and longevity gives wireless ECoG excellent prospect to become the technology of choice for clinically relevant neural recording in the foreseeable future.

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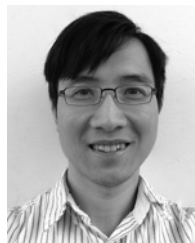
Rikky Muller (S'07–M'14) received the B.Sc. and M.Eng. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2004, and the Ph.D. degree from the University of California, Berkeley, CA, USA, all in electrical engineering.

She was an IC Designer with Analog Devices from 2004 to 2007. While with the University of California, she was a member of the Berkeley Wireless Research Center and the Center for Neural Engineering and Prosthesis. She was a McKenzie Fellow and Lecturer of Electrical and Electronic

Engineering with the University of Melbourne from 2013 to 2014. In 2013, she cofounded Cortera Neurotechnologies, Berkeley, CA, USA, where she is currently CEO. Her research interests are in low-power circuits, MEMS/sensor interfaces, implantable microsystems and neuroengineering.

Dr. Muller was the recipient of the McKenzie Postdoctoral Fellowship (2014), the MAP Entrepreneurial Fellowship (2013), the UC Berkeley EE

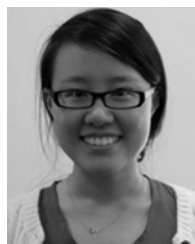
Graduate Fellowship (2007–2008), the Center for Neural Engineering and Prosthesis Graduate Fellowship (2012).



Han-Phuc Le (S'05–M'13) received the B.S. degree in electrical engineering from Hanoi University of Technology, Vietnam, in 2003, the M.S. degree from KAIST, Daejeon, Korea, in 2006, and the Ph.D. degree from the University of California, Berkeley, CA, USA, in 2013.

In 2012, he cofounded Lion Semiconductor Inc., Berkeley, CA, USA, where he is currently the Chief Technology Officer. He has held R&D and consulting positions at the Vietnam Academy of Science and Technology in Vietnam, KEC, LG and JDA

Tech in Korea, Oracle, AMD, Intel and Rambus. His interests include circuit designs for power electronics and communications applications, with emphasis on high-speed switched-mode power supply, fully integrated conversions, control methodology and mixed-signal integrated circuits.



Wen Li (S'08) received the B.Eng. degree in electrical engineering from the Chinese University of Hong Kong, Hong Kong, in 2008. She is currently working toward the Ph.D. degree at the University of California, Berkeley, CA, USA.

Her research interests include analog/mixed-signal/RF circuits and energy-efficient wireless systems for biomedical applications.



Peter Ledochowitsch (S'11–M'14) received the Dipl.-Phys. degree from the Georg August University, Göttingen, Germany, in 2008, and the Joint Ph.D. degree in bioengineering from the University of California, Berkeley, CA, USA, and the University of California, San Francisco, CA, USA, in 2013. His doctoral work, developed at the Berkeley Sensor and Actuator Center (BSAC) and supported in part by the Center for Neural Engineering and Prosthesis (CNEP), focused on the development of high-performance micro-Electrocorticography

(μ ECoG) sensors, as well as their applications to basic neuroscience, and brain–machine interfaces (BMI).

He is currently a Scientist I with Neural Coding at the Allen Institute for Brain Science, Seattle, WA, USA, and is a cofounder and CTO of Cortera Neurotechnologies Inc., Berkeley, CA, USA

Dr. Ledochowitsch was a Fellow of the German National Academic Foundation (2003–2008).



Simone Gambini (S'04–M'11) received the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA, in 2009.

In 2010, he was with Telegent Systems, where he designed RF circuits for highly integrated mobile TV tuners. From 2011 to 2012, he designed next-generation magnetic biosensors and other MEMS interfaces. During 2012–2014, he was a Lecturer with the Electrical Engineering Department, University of Melbourne, Melbourne, Australia. His research interests are in leveraging low-power

electronics to create microsystems integrating sensing, actuation, and wireless communication. He has authored/coauthored over 20 papers in the area of low-power integrated circuits and systems.

Dr. Gambini is an associate editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and a member of the Technical Program Committee of the European Solid-State Circuits Conference.



Toni Bjorninen (M'08) received the M.Sc. and Ph.D. degrees (with distinction) in electrical engineering from Tampere University of Technology, Tampere, Finland, in 2009 and 2012, respectively.

He is currently an Academy of Finland Postdoctoral Researcher with the Department of Electronics and Communications Engineering, Tampere University of Technology, Tampere, Finland, where his research is focused on implantable and wearable antennas in body-centric sensing systems. His other research interests include antenna technologies in RFID systems and computational methods in electromagnetics and microwave engineering. He has authored/coauthored 80 peer-reviewed scientific publications.



Aaron Koralek (S'13) received the A.B. degree in molecular biology from Princeton University, Princeton, NJ, USA, in 2006, and the Ph.D. degree from the Helen Wills Neuroscience Institute, University of California, Berkeley, CA, USA, in 2014.

He is currently a Postdoctoral Researcher with the Champalimaud Neuroscience Programme, Lisbon, Portugal. While at Berkeley, he did graduate work in the Brain-Machine Interface Systems Laboratory of Dr. Jose M. Carmena investigating neural correlates of learning, large-scale neuronal network dynamics, neural plasticity, and brain-machine interfaces. He is currently working in the Neurobiology of Action Laboratory of Dr. Rui M. Costa investigating dopaminergic modulation of behavioral exploration and variability in action selection.



Jose M. Carmena (SM'09) received the B.S. degree in electrical engineering from the Polytechnic University of Valencia, Valencia, Spain, in 1995, the M.S. degree in electrical engineering from the University of Valencia, Valencia, Spain, in 1997, and the M.S. degree in artificial intelligence and Ph.D. degree in robotics from the University of Edinburgh, Edinburgh, U.K., in 1998 and 2002, respectively.

From 2002 to 2005, he was a Postdoctoral Fellow with the Department of Neurobiology and the Center for Neuroengineering, Duke University, Durham, NC, USA. He is an Associate Professor of electrical engineering and neuroscience with the University of California, Berkeley, CA, USA, and Co-Director of the Center for Neural Engineering and Prostheses there and the University of California, San Francisco, CA, USA. His research program in neural engineering and systems neuroscience is aimed at understanding the neural basis of sensorimotor learning and control and at building the science and engineering base that will allow the creation of reliable neuroprosthetic systems for the severely disabled.

Dr. Carmena is a senior member of the IEEE Robotics and Automation, Systems, Man and Cybernetics, and Engineering in Medicine and Biology Societies, the Society for Neuroscience, and the Neural Control of Movement Society. He was the recipient of the Bakar Fellowship (2012), the IEEE Engineering in Medicine and Biology Society Early Career Achievement Award (2011), the Aspen Brain Forum Prize in Neurotechnology (2010), the National Science Foundation CAREER Award (2010), the Alfred P. Sloan Research Fellowship (2009), the Okawa Foundation Research Grant Award (2007), the UC Berkeley Hellman Faculty Award (2007), and the Christopher Reeve Paralysis Foundation Postdoctoral Fellowship (2003).



Michel M. Maharbiz (SM'14) received the Ph.D. degree from the University of California, Berkeley, CA, USA, under Prof. Roger T. Howe and Prof. Jay D. Keasling in 2003.

Until 2007, he was an Assistant Professor with the University of Michigan, Ann Arbor, MI, USA. He joined the faculty of the University of California, Berkeley, CA, USA, in 2008, where he is now an Associate Professor with the Department of Electrical Engineering and Computer Science. He is a cofounder of Tweedle Technologies and Cortera Neurotechnologies Inc, Berkeley, CA, USA. His current research interests include building micro/nano interfaces to cells and organisms and exploring bio-derived fabrication methods.

Dr. Maharbiz is a Bakar Fellow. He was the recipient of a 2009 National Science Foundation Career Award and received popular recognition for his work in building interfaces to living organisms (MIT TR10, Time Magazine's Top 50 Inventions of 2009).



Elad Alon (SM'12) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2001, 2002, and 2006, respectively.

In January 2007, he joined the University of California, Berkeley, CA, USA, where he is now an Associate Professor of electrical engineering and computer sciences as well as a Codirector of the Berkeley Wireless Research Center (BWRC). He has held consulting, visiting, or advisory positions at Lion Semiconductor, Wilocity, Cadence, Xilinx, Oracle, Intel, AMD, Rambus, Hewlett Packard, and IBM Research, where he worked on digital, analog, and mixed-signal integrated circuits for computing, test and measurement, and high-speed communications. His research focuses on energy-efficient integrated systems, including the circuit, device, communications, and optimization techniques used to design them.

Dr. Alon was the recipient of the IBM Faculty Award in 2008, the 2009 Hellman Family Faculty Fund Award as well as the 2010 UC Berkeley Electrical Engineering Outstanding Teaching Award, and has coauthored papers that received the 2010 ISSCC Jack Raper Award for Outstanding Technology Directions Paper, the 2011 Symposium on VLSI Circuits Best Student Paper Award, and the 2012 as well as 2013 Custom Integrated Circuits Conference Best Student Paper Award.



Jan Rabaey (F'95) received the Ph.D. degree in applied sciences from the Katholieke Universiteit Leuven, Leuven, Belgium.

After being connected to the University of California, Berkeley, CA, USA, as a Visiting Research Engineer, he was a Research Manager with IMEC, Leuven, Belgium. In 1987, he joined the faculty of the Electrical Engineering and Computer Science Department, University of California, Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship. He is currently the Scientific Co-director of the Berkeley Wireless Research Center (BWRC), as well as the Director of the FCRP Multiscale Systems Research Center (MuSyC). His research interests include the conception and implementation of next-generation integrated wireless systems.

Dr. Rabaey was the recipient of a wide range of awards, among which are the 2008 IEEE Circuits and Systems Society Mac Van Valkenburg Award and the 2009 European Design Automation Association (EDAA) Lifetime Achievement award. In 2010, he was awarded the prestigious Semiconductor Industry Association (SIA) University Researcher Award.