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# A Minimum Viable Mission Profile Emulator for IGBT Modules in Modular Multilevel Converters

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#### **ABSTRACT**

Various methods have been presented to emulate the electrical behavior of Modular Multilevel Converters (MMCs). To meet the demands for reliability aspect study of MMCs, this paper proposes a minimum viable setup to emulate the thermal behavior and investigates its feasibility for reliability testing. The proposed mission profile emulator has three distinctive features: 1) capable of emulating and measuring the thermal stresses of power modules; 2) capable of implementing practical switching profiles as a full-scale MMC; and 3) with significantly reduced requirement for dc power supply compared to existing setups used for electrical aspect study. Theoretical discussions and experimental measurements are presented to demonstrate the capability of the mission profile emulator.

#### I. INTRODUCTION

MMCs have become a key equipment of High Voltage Direct Current (HVDC) transmission today [1]-[3]. However, due to the massive use of IGBT power modules, its reliability study becomes essential to model based design of MMCs [4] [5]. Reliability aspect testing based on a full-scale MMC is usually not economically wise, therefore, a minimum viable setup that can emulate the key electro-thermal stresses of the IGBT modules applied in MMCs is a feasible solution. In the prior-art studies, sub-module (SM) based test setups focus mainly on the electrical behavior emulation. An equivalent test scheme in [6] utilizes two SMs to emulate the electrical features of SMs (e.g., the SM capacitor voltage and the arm current). Based on the resonant test circuit proposed in [7] and control of the MMC can be conducted. However, when it comes to the thermal and reliability emulation of the SM, these setups can no longer fulfill all specific test requirements summarized as below for the MMC: 1) Capability of providing high blocking voltage and high current for the practical power devices in the MMC [8], 2) low switching frequency mission profile (e.g., several times of the fundamental frequency [9]), 3) smooth arm current, and 4) dc bias in the arm current profile [7] [10]. For the test bench in [10], series-connected IGBTs have to be used when applying the testing to Device Under test (DUT) rated at higher than 2 kV to fulfill the highvoltage requirement. The test bench in [6] has to increase the switching frequency in order to achieve a smooth arm current, but scarifies its thermal performance of the MMC with a low switching frequency in the field. The resonant test circuit in

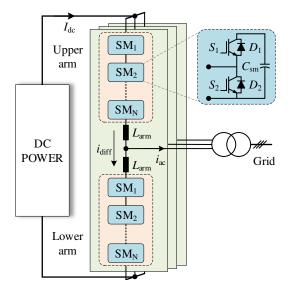


Fig. 1. Circuit configuration of a typical three-phase MMC.  $I_{\rm dc}$  is the dc-bus current,  $i_{\rm ac}$  is the output ac current,  $i_{\rm cir}$  is the circulating current,  $L_{\rm arm}$  is the arm inductor, and  $C_{\rm sm}$  is the submodule capacitor.

[7], is unable to generate dc bias in the arm current, which fails to emulate the practical operation of the MMC, and its corresponding thermal behavior. As an improvement, [11] utilizes a full bridge converter to emulate the arm current profile, and introduces an auxiliary SM connected in series with the DUT. Its test capability is improved more than five times in terms of the applicable voltage level compared with the previous one [10]. However, the power supply voltage is still coupled with the DUT, and should be carefully chosen. In this paper, a novel SM-based mission profile emulator is proposed. It is capable of emulating and measuring the thermal stresses of power modules, and implementing practical switching profile as a full-scale MMC. Moreover, the requirement for dc power supply is significantly reduced compared to existing viable setups.

# II. PROPOSED MISSION PROFILE EMULATOR AND ITS CONTROL SCHEME

In order to build a SM-based mission profile emulator of the MMC, the operation of the SM has to be identified first and then fully emulated. Thus, this section will first present the basic operation of a full-scale MMC, and then the proposed mission profile emulator.

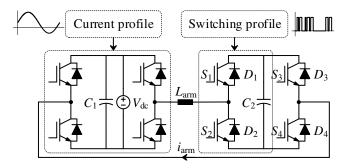


Fig. 2. Topology of the proposed mission profile emulator.

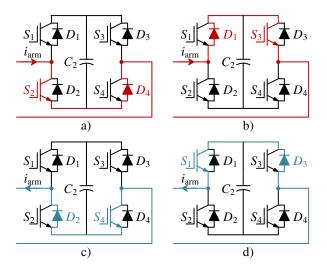


Fig. 3. Ideal paths for positive current in the DUT and two auxiliary IGBTs. (a) Bypass SM with positive arm current; (b) Insert SM with positive arm current; (c) Bypass SM with negative arm current; (d) Insert SM with negative arm current.

#### A. Basic Configuration and Operation of MMCs

The typical configuration of a three-phase MMC is shown in Fig. 1. Each phase is divided into two arms: the upper arm and the lower arm. Each arm consists of N series-connected half-bridge SMs and an arm inductor to limit the circulating current and fault current. In order to transfer the active power, besides the ac component, a dc circulating current exists in the arm current. As for the modulation methods, two commonly used ones are Phase Shifted Carrier (PSC) modulation [9], [12] and the Nearest Level Modulation (NLM) [13], [14]. PSC is suitable for MMCs with a small number of SMs per arm and the switching frequency of SMs should be high. NLM is utilized when the MMC is applied in high-voltage applications, where hundreds of SMs per arm are connected in series. In addition, the switching frequency can be as low as several times of the fundamental frequency [15].

#### B. Proposed Mission Profile Emulator

In order to emulate the mission profile of the MMC and to evaluate the thermal stresses of the power modules, a mission profile emulator composed of two full bridge converters is proposed as shown in Fig. 2. One of them together with an inductor and a low-voltage power supply serve to regulate the

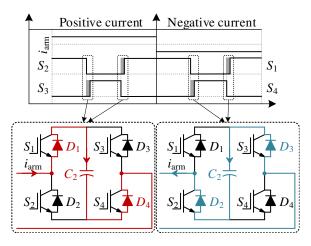


Fig. 4. Current paths to charge the capacitor  $C_2$  during the interval of gate signal delay.

inductor current. Another full bridge converter consists of the DUT, a capacitor  $C_2$ , and two auxiliary IGBTs. The DUT is controlled by the switching profile obtain from simulations, and the auxiliary IGBTs are designed to provide extra current paths without going through capacitor  $C_2$  as shown in Fig. 3.

In theory,  $S_1$  and  $S_3$  share the same gate signals, which is complementary to the devices  $S_2$  and  $S_4$ . It means that there is always a current path in the DUT, which ensures that the capacitor  $C_2$  will not be charged or discharged regardless of the switching and current profile. Thus, two main advantages can be achieved by this topology. One is that the switching profile is decoupled with the current profile, and any practical switching profile (e.g., different switching frequency) can be tested on this setup. The other is that the voltage of power supply  $V_{\rm dc}$  is decoupled with the voltage of DUT. This can facilitate the test of a SM rated at high voltage level. Note that  $C_2$  serves only to maintain the blocking voltage of the power devices same as the average value of an actual SM in order to obtain the same switching loss. In addition, turnon delays have to be programmed for all gate signals in order to avoid short circuit failures in practice. In this case, non-ideal current paths charge the capacitor  $C_2$  during the delay interval as shown in Fig. 4. Consequently, the capacitor voltage deviate from its desired value, especially when a high frequency switching profile is applied. Thus, a capacitor voltage controller is needed for the mission profile emulator.

#### C. Capacitor Voltage Control

The gate signals of  $S_1$  and  $S_2$  are decided by the switching profile allowing no interference from external controllers. The two auxiliary power switches therefore serve to achieve the control objective. The control principle is to add extra switching actions to  $S_3$  and  $S_4$ , and to force the current to go through the capacitor  $C_2$ . In this case, the capacitor  $C_2$  can be charged/discharged accordingly, and its voltage is thus possible to be controlled. More specifically, the introduced low-level switching actions can charge the capacitor regardless of the

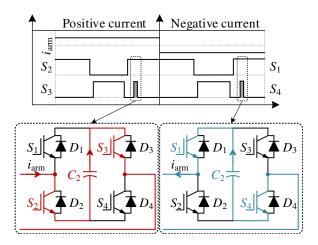


Fig. 5. Current paths to discharge the capacitor  $C_2$  during the additional high-level switching actions.

current direction, and high-level actions can discharge it as shown in Fig. 5.

For mission profiles with high switching frequency, such as the phase-shifted carrier (PSC) modulation, this control strategy can be implemented by adding an adjustment coefficient to the voltage reference for the gate signals of  $S_3$  and  $S_4$  as shown in Fig. 6. The adjustment is dynamically decided by the capacitor voltage error, the arm current and the switching profile. In detail, a positive adjustment contributes to an extra turn-on delay and turn-off lead of  $S_3$  to charge the capacitor, and a negative adjustment can add additional turn-on leads and turn-off delays to  $S_3$  to discharge the capacitor. The advantage of this method lies in the same switching frequency between the DUT and the two auxiliary IGBTs. Thus, the same power device and cooling system design can be implemented for all the power switches.

However, this aforementioned method is not effective for mission profiles with low switching frequency, such as the nearest level modulation (NLM), where a limited number of switching actions can be used to regulate the capacitor voltage. One alternative way is, as shown in Fig. 7, to generate additional high frequency switching actions, and combine it with the low switching frequency profile in order to get the final gate signals for  $S_3$  and  $S_4$ . The duty cycle of the additional high frequency switching actions is decided by the amplitude of the arm current to limit the introduced current ripple. Note that the capacitor voltage control is only enabled when its voltage goes out of the upper and lower limitations.

#### D. Control Parameter Selection

The parameter in both capacitor voltage controls is  $k_{\rm p}$ . It determines the time interval of introduced switching actions, and further affects the current ripple, which should be limited within a certain range. Within the short interval, the voltage of  $C_2$  is assumed to be constant, and the current ripple is

$$\frac{V_{\rm C2}}{L_{\rm arm}}T_{\rm intro} = k_{\rm ripple} |i_{\rm arm}|, \qquad (1)$$

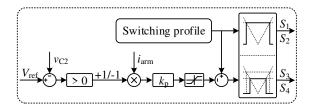


Fig. 6. Current paths to discharge the capacitor  $C_2$  during the additional high-level switching actions. (ref is the arm voltage reference.)

| Item  | Value   |
|---|---------|
| Dc power supply voltage $V_{ m dc}$                     | 35 V    |
| Capacitor voltage $V_{ m C2}$                           | 300.0 V |
| Capacitor $C_2$   | 2.9 mF  |
| Inductor $L_{arm}$                                      | 2.0 mH  |
| Carrier frequency of the current source $f_{ m sw\_cs}$ | 6.0 kHz |
| Carrier frequency of the DUT $f_{\mathrm{sw\_DUT}}$     | 1.5 kHz |
| Current frequency $f_{ m current}$                      | 50 Hz   |
| Dc current amplitude $I_0$                              | 7.13 A  |
| Fundamental current amplitude $I_1$                     | 17.85 A |
| Ambient temperature $T_{\rm a}$                         | 20 °C   |

where  $V_{\rm C2}$  is the average voltage of capacitor  $C_2$ ,  $L_{\rm arm}$  is the coupling inductor,  $T_{\rm intro}$  is the time interval of the introduced switching actions,  $i_{\rm arm}$  is the arm current,  $k_{\rm ripple}$  is current ripple ratio. Furthermore, the duty ratio of introduced pulses is

$$k_{\rm p} |i_{\rm arm}| = T_{\rm intro} f_{\rm a} = \frac{k_{\rm ripple} |i_{\rm arm}| L_{\rm arm} f_{\rm a}}{V_{\rm C2}},$$
 (2)

where  $f_{\rm a}$  is the introduced high frequency carrier frequency. Thus,  $k_{\scriptscriptstyle \rm D}$  can be calculated as

$$k_{\rm p} = \frac{k_{\rm ripple} L_{\rm arm} f_{\rm a}}{V_{\rm C2}}.$$
 (3)

By using (3), the current error caused by the capacitor voltage control can be limited within  $k_{\rm a} \times 100\%$  of the actual current.

#### III. MISSION PROFILE EMULATOR DEMONSTRATION

In order to validate the effectiveness of the proposed mission profile emulator and its control, an experimental setup is built as shown in Fig. 8. Three full-bridge IGBT modules F4\_50R12KS4 [16] are used. One full-bridge module functions to track the current profile as a current source. Another one is used as the DUT operating as a half-bridge, which aims to exclude the impact of thermal coupling from the two auxiliary power devices implemented by a third half-bridge module. For safe operation, a 2 us turn-on delay is added to all gate signals. The junction temperatures are measured by a thermal camera [].

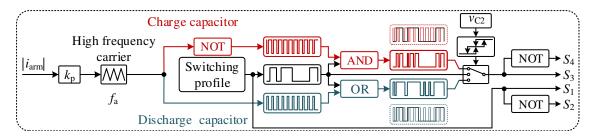


Fig. 7. Capacitor voltage control for mission profiles with low switching frequency.

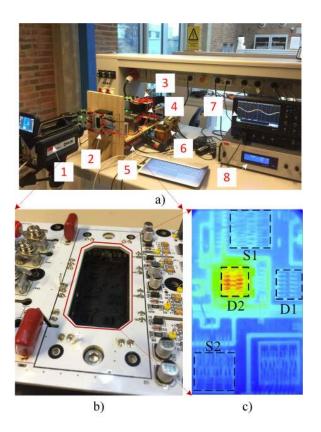


Fig. 8. Experimental setup of the proposed mission profile emulator. a) Photo of the setup, b) Photo of the SM, and c) Thermal distribution of the DUT. (1: thermal Camera, 2: Device Under Test, 3: IGBT module for current control and auxiliary module, 4: inductor, 5: power Supply.)

### A. Electrical Behavior Verification

Fig. 9 and Fig. 10 show the experimental waveforms of the capacitor voltage control used in mission profiles with high switching frequency and low switching frequency respectively. It can be seen that the capacitor voltage is controlled to increase gradually from zero to the desired voltage of 300 V in the start-up process, taking about 1.1 s for the PSC and 2 s for the NLM in total. Afterwards, the capacitor voltage stabilizes, and the mission profile test starts. It can be seen that the current waveform is well regulated to be a dc bias plus a sinusoidal component, which is the exact operation of MMCs. In addition, the characteristics of two modulation strategies can be clearly seen from the zoom-in figure of the gate signals. For the NLM as shown in Fig. 10, high frequency additional

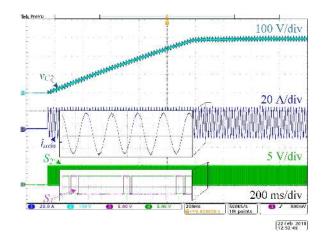


Fig. 9. Experimental results of the capacitor voltage, arm current and gate signals with PSC.

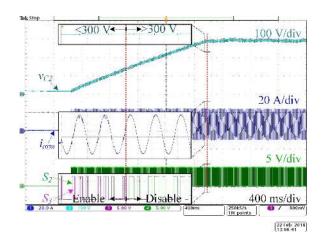


Fig. 10. Experimental results of the capacitor voltage, arm current and gate signals with NLM.

switching pulses can be observed in  $S_3$  when the capacitor voltage control is enabled, and  $S_3$  becomes the same with  $S_2$  when the capacitor voltage keeps stable at 300 V. For the PSC shown in Fig. 9, extra turn-on delays and turn-off leads can be seen for  $S_3$  compared with the gate signal of  $S_2$  for the capacitor voltage control. The above experiments validate the functionality of the proposed mission profile emulator in terms of its electrical behavior.

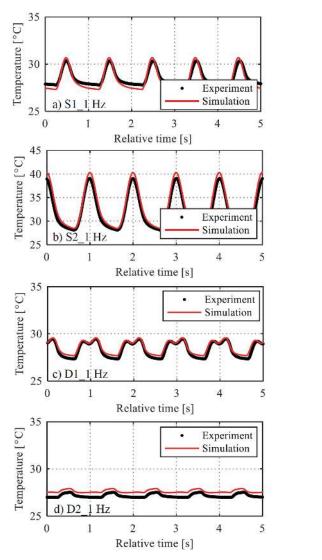


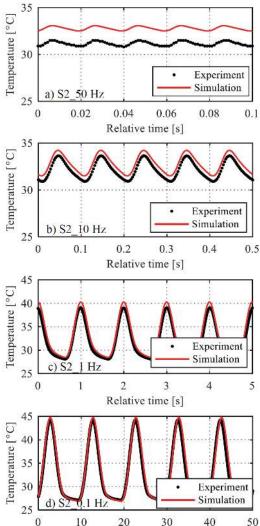
Fig. 11. Experimental and simulated waveforms of the junction temperatures with the frequency being 1 Hz. a)  $S_1$ , b)  $S_2$ , c)  $D_1$ , and d)  $D_2$ .

# 25 0 10 20 30 40 50 Relative time [s] Fig. 12. Experimental and simulated waveforms of the junction temperatures respectively. By contrast, they are 1 °C and 27 °C for the least stressed component $D_2$ respectively. Conversely, $D_2$ is the most stressed component when the active power is transferred conversely from the ac side to the dc side. Thus, thermal management or thermal balancing control within each SM deserves to be studied to fulfill the lifetime matching of all four devices. Moreover, comparing the simulations and the experiments, a temperature difference up to 1°C can be observed for the average temperature of the four devices.

Fig. 12 shows the junction temperature of the most stressed device  $S_2$  with different cycle periods ranging from 50 Hz to 0.1 Hz. It can be seen that the simulated temperature swings agree well with the experiments with the highest error of 0.88 °C when the frequency is 1 Hz. As for the average temperature, the temperature error goes down from 1.5 °C to 0.2 °C with the decrease of frequency from 50 Hz to 0.1 Hz.

# B. Thermal Behavior Verification

The dc bias in the arm current contributes to an unbalanced thermal stress distribution inside each SM for the MMC. Thus, in order to evaluate the thermal behavior of each power devices, both simulation and experiment are conducted. Prior to the experiment, the on-state characteristics and the switching energies per pulse of the IGBT and diode are measured for the simulation purpose. In addition, a thermal coupling model including the four devices of interest is established through a complete thermal path from the junction to the ambient. Main operating parameters are listed in Table I. Fig. 11 shows the simulated and experimental results of the junction temperatures of the four devices under the switching mission profile of the PSC. It can be seen that, when the active power is transferred from the dc side to the ac side,  $S_2$  is most stressed with the junction temperature variation and the mean junction temperature being 11 °C and 34 °C



with different current frequency. a) 50 Hz, b) 10 Hz, c) 1Hz, and d) 0.1 Hz.

#### IV. CONCLUSION

A mission profile emulator is proposed to assess the thermal behavior and the reliability of the power modules in the MMC. The use of two auxiliary IGBTs decouples the power supply voltage with the DUT as well as the switching profile with the current profile. The voltage requirement for dc power supply is greatly reduced, and any practical switching profile can be tested. Moreover, two capacitor voltage control strategies applicable to mission profiles with different switching frequencies are proposed. The experimental results demonstrate the effectiveness of the proposed mission profile emulator.

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