A Modeling Approach for Σ–Δ Fractional-N Frequency Synthesizers Allowing Straightforward Noise Analysis

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***Abstract*—A general model of phase-locked loops (PLLs) is derived which incorporates the influence of divide value variations. The proposed model allows straightforward noise and dynamic analyses of Σ–Δ fractional-N frequency synthesizers and other PLL applications in which the divide value is varied in time. Based on the derived model, a general parameterization is presented that further simplifies noise calculations. The framework is used to analyze the noise performance of a custom Σ–Δ synthesizer implemented in a 0.6-μm CMOS process, and accurately predicts the measured phase noise to within 3 dB over the entire frequency offset range spanning 25 kHz to 10 MHz.**

***Index Terms*—Delta, dithering, divider, fractional-N, frequency, modeling, noise, phase-locked loop, PLL, quantization noise, sigma, synthesizer.**

I. Introduction

THE USE OF wireless products has been rapidly increasing in the last decade, and there has been worldwide development of new systems to meet the needs of this growing market. As a result, new radio architectures and circuit techniques are being actively sought that achieve high levels of integration and low-power operation while still meeting the stringent performance requirements of today's radio systems. One such technique is the use of Σ–Δ modulation to achieve high-resolution frequency synthesizers that have relatively fast settling times, as described by Riley *et al*. in [1], Copeland in [2], and Miller and Conley in [3], [4]. This method has now been used in a variety of applications ranging from accurate frequency generation [1], [5]–[7] to direct frequency modulation for transmitter applications [8]–[12].

However, despite its increasing use, a general model of Σ–Δ fractional-N synthesizers to encompass dynamic and noise performance has not previously been presented. The primary obstacle to deriving such a model is that, in contrast to classical phase-locked loop (PLL) systems, a Σ–Δ synthesizer dynamically varies the divide value in the PLL according to the output of a Σ–Δ modulator. Traditional methods of PLL analysis assume a static divide value, and the step toward allowing for dynamic variations is not straightforward. As a result, the impact of the divide value variations is often treated in isolation of other influences on the PLL [1], such as noise in the phase detector and voltage-controlled oscillator (VCO), and overall analysis of the synthesizer becomes cumbersome.

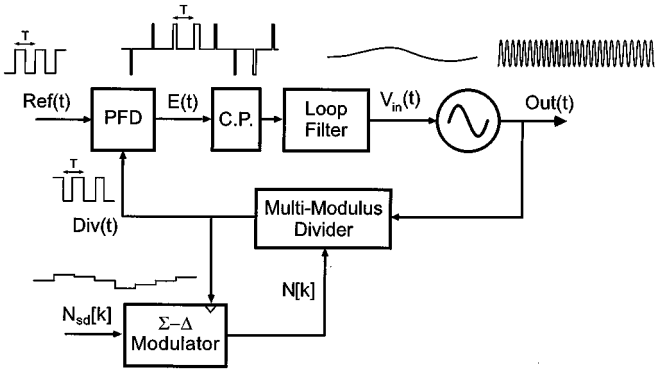

Fig. 1. Block diagram of a Σ–Δ frequency synthesizer.

In this paper, we develop a simple model for the Σ–Δ synthesizer that allows straightforward analysis of its dynamic and noise performance. The predictions of the model compare extremely well to simulated and experimental results of implemented Σ–Δ synthesizers [9], [10], [13]. In addition, we present a PLL parameterization that simplifies calculation of the PLL dynamics and assessment of the synthesizer noise performance.

To develop the Σ–Δ synthesizer model, we first derive a general model of the PLL that incorporates the influence of divide value variations. The derivation is done in the time domain and then converted to a frequency-domain block diagram. We parameterize the resulting PLL model in terms of a single function $G(f)$ and illustrate its usefulness in determining the noise performance of the PLL. The Σ–Δ modulator is then included in the generalized PLL model and its impact on the PLL is analyzed. Finally, the modeling approach is used to calculate the noise performance of a custom Σ–Δ synthesizer integrated in a 0.6-μm CMOS process and then compared to measured results.

II. Background

Fig. 1 displays a block diagram of a Σ–Δ frequency synthesizer, along with a snapshot of the signals associated with various nodes in this system. A PLL in essence, the synthesizer achieves accurate setting of its output frequency by locking to a reference frequency. This locking action is accomplished through feedback by dividing down the VCO output frequency and comparing its phase to the phase of the reference source

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to produce an error signal. The phase comparison operation is done through the use of a phase/frequency detector (PFD) which also acts as a frequency discriminator when the PLL is out of lock. The loop filter attenuates high-frequency components in the PFD output so that a smoothed error signal is sent to the VCO input. It consists of an active or passive network, and is typically fed by a charge pump which converts the error signal to a current waveform. The charge pump is not necessary, but provides a convenient means of setting the gain of the loop filter and simplifies implementation of an integrator when required.

As illustrated in the figure, a key characteristic of Σ–Δ synthesizers is that the divide value is dynamically changed in time according to the output of a Σ–Δ modulator. By doing so, much higher frequency resolution can be achieved for a given PLL bandwidth setting than possible with classical integer-N frequency synthesizers [1].

III. Time-Domain PLL Model

We now derive time-domain models for each individual PLL block shown in Fig. 1. The primary focus of our effort is on obtaining a divider model incorporating dynamic changes to its value. However, the derivation of this model requires careful attention to the way we model the PFD. In particular, we will parameterize signals associated with a tristate PFD with sequences that can be directly related to the divider operation. This approach is extended to an XOR-based PFD by relating its output to that of a tristate PFD. Following a brief derivation of the VCO model, we then obtain the divider model by relating its operation to the VCO model and the PFD sequences discussed above. Finally, the charge pump and loop filter models are described, and the overall PLL model constructed.

A. Tristate PFD

The tristate PFD and its associated signals are shown in Fig. 2. The output of the detector, $E(t)$, is characterized as a series of pulses whose widths are a function of the relative phase difference between rising edges of $\mathrm{Ref}(t)$ and $\mathrm{Div}(t)$. We parameterize the phase difference between $\mathrm{Ref}(t)$ and $\mathrm{Div}(t)$ with the discrete-time sequences $\Phi_{\mathrm{ref}}[k]$ and $\Phi_{\mathrm{div}}[k]$, respectively. $\Phi_{\mathrm{ref}}[k]$ is nominally zero, and $\Phi_{\mathrm{div}}[k]$ is defined in (1). The series of pulses that form $E(t)$ are parameterized by the following discrete-time sequences.

- t_k: time instants at which the rising edges of the reference clock occur.
- $t_k + \Delta t_k$: time instants at which the rising edges of the divider output occur.
- Δt_k: time difference between rising edges of $\mathrm{Ref}(t)$ and $\mathrm{Div}(t)$.

Assuming a constant reference frequency, consecutive values for t_k are related for all k as

$$t_k - t_{k-1} = T$$

where T is the reference period. We will make use of the Δt_k parameterization in deriving the PFD model; the other sequences will be used when deriving the divider model.

Since phase detection is a memoryless operation, its influence on the PLL dynamics is sufficiently modeled by its gain. However, the pulsed behavior of the PFD output adds some complexity in deriving the value of that gain, so our derivation will consist of two steps. The first step relates the input phase difference to the Δt_k sequence. The second step relates the Δt_k sequence to an impulse approximation of the $E(t)$ waveform.

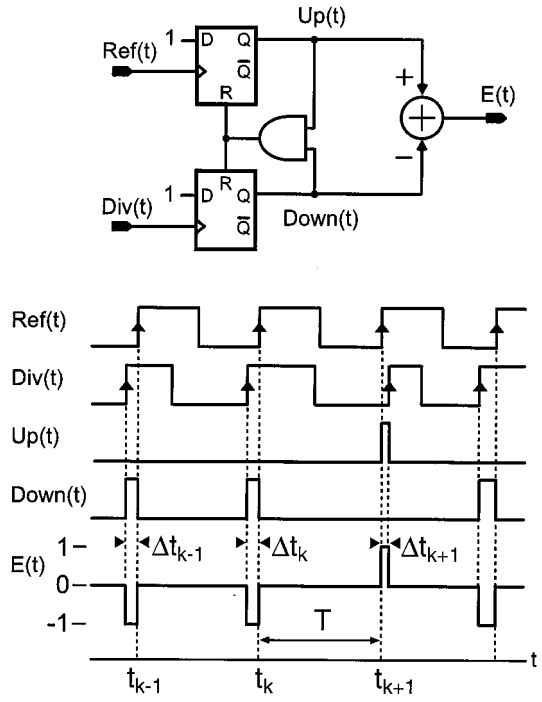

Fig. 2. Tristate phase-frequency detector and associated signals.

The relationship of Δt_k to the phase difference, $\Phi_{\mathrm{ref}}[k] - \Phi_{\mathrm{div}}[k]$, is defined as

$$\Delta t_k = \frac{T}{2\pi}(\Phi_{\mathrm{ref}}[k] - \Phi_{\mathrm{div}}[k]). \tag{1}$$

To verify the above definition, one observes from Fig. 2 that a phase error of π causes Δt_k to be $T/2$.

The impact of the Δt_k sequence on the PLL dynamics is cumbersome to model analytically since the pulse-width modulated PFD output has a *nonlinear* influence on the PLL dynamics. However, a simple approximation greatly eases our efforts—we simply represent the PFD output as an impulse sequence rather than a modulated pulse sequence. Fig. 3 illustrates this approximation; pulses in $E(t)$ are represented as impulses with area equal to their corresponding pulse, as described by

$$E(t) \approx \sum_{k=-\infty}^{\infty} \Delta t_k \delta(t - kT). \tag{2}$$

We discuss the significance of the above expression when we derive the frequency-domain model of the PLL in Section IV.

Our justification for the impulse approximation is heuristic—each PFD output pulse has much smaller width than the loop filter impulse response, and therefore acts like an impulse when the two are convolved together. Obviously, the accuracy of this approximation depends on how much smaller the PFD output pulse widths are compared to the dominant time constant of the loop filter. Since the PFD pulses must be smaller than a reference period, high accuracy is achieved

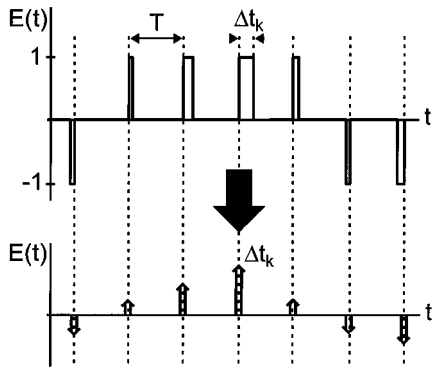

Fig. 3. Impulse sequence approximation of PFD output.

when the reference frequency is much higher than the loop filter (PLL) bandwidth. Fortunately, this condition is satisfied when dealing with Σ–Δ synthesizers since a high reference frequency to PLL bandwidth ratio is required to adequately suppress the Σ–Δ quantization noise. For additional discussion on this issue, see [13].

B. XOR-Based PFD

An XOR-based PFD is shown in Fig. 4 [13]–[15], along with associated signals that will be discussed later. Assuming the PFD is not performing frequency acquisition, the signal $C(t)$ is simply passed to the output, $E(t)$, so that the detector operates as an XOR phase detector. As such, the detector outputs an average error of zero when $\mathrm{Ref}(t)$ and $\mathrm{Div}(t)$ are in quadrature, and $E(t)$ is nominally a two-level square wave rather than the trilevel short-pulse waveform obtained with the tristate design. The combination of having wide pulses and only two output levels allows the XOR-based PFD to achieve high linearity, which is desirable for Σ–Δ synthesizer applications to avoid folding down Σ–Δ quantization noise [13].

To model the XOR-based PFD, we simply relate its associated signals to the tristate detector so that the previous results can be readily applied. Fig. 4 displays the signals associated with this PFD, and reveals that the output $E(t)$ can be decomposed into the sum of a square wave, $E_{\mathrm{spur}}(t)$, and a trilevel pulse waveform, $\hat{E}(t)$. The first component is independent of the input phase difference to the detector and presents a spurious noise signal to the PLL; its influence can be made negligible with proper design. The second component, $\hat{E}(t)$, captures the impact of the input phase difference, $\Phi_{\mathrm{div}}(t) - \Phi_{\mathrm{ref}}(t)$, on the PFD output, and can be parameterized according to the width of its pulses, where

$$\Delta t_k = \frac{T}{2\pi}(\Phi_{\mathrm{ref}}[k] - \Phi_{\mathrm{div}}[k] - \pi).$$

As with the tristate detector, the impulse approximation can be applied to obtain

$$E(t) \approx \sum_{k=-\infty}^{\infty} 2\Delta t_k \delta(t - kT) + E_{\mathrm{spur}}(t)$$

which, if we ignore $E_{\mathrm{spur}}(t)$, is the tristate expression multiplied by a factor of 2. Thus, if we ignore the phase offset of π and the square wave $E_{\mathrm{spur}}(t)$, the XOR-based PFD has an identical model to that of the tristate topology except that its gain is increased by a factor of 2.

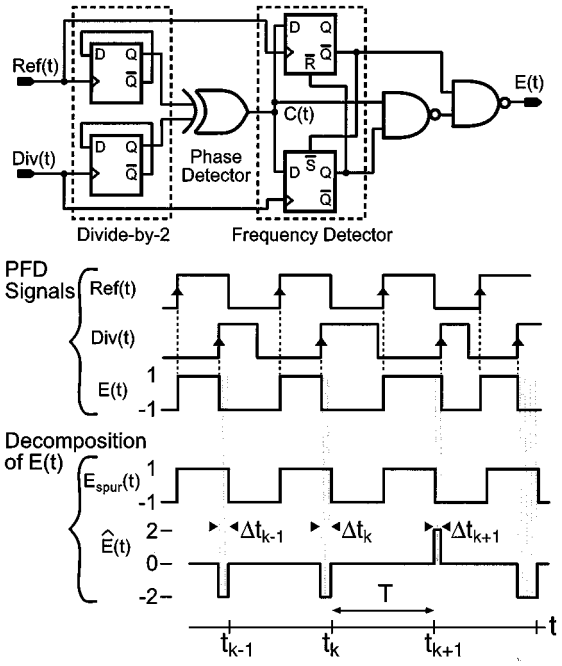

Fig. 4. XOR-based PFD, associated signals, and $E(t)$ decomposition.

C. Voltage-Controlled Oscillator

For our purposes, only two equations are needed to model the VCO. The first relates *deviations* in the VCO phase, defined as $\Phi_{\mathrm{out}}(t)$, to changes in the VCO input voltage, $V_{\mathrm{in}}(t)$. Since VCO phase is the integral of VCO frequency, and deviations in VCO frequency are calculated as $K_v V_{\mathrm{in}}(t)$, where K_v is in units of hertz per volt, we have

$$\Phi_{\mathrm{out}}(t) = \int 2\pi K_v V_{\mathrm{in}}(t) dt. \tag{3}$$

The second equation relates the *absolute* VCO phase, defined as $\Phi_{\mathrm{vco}}(t)$, to deviations in the VCO phase and the nominal VCO frequency f_{nom}:

$$\Phi_{\mathrm{vco}}(t) = 2\pi f_{\mathrm{nom}} t + \Phi_{\mathrm{out}}(t). \tag{4}$$

Our modeling efforts will be primarily focused on deviations in the VCO phase, so that (3) is of the most interest. However, (4) is required in the divider derivation that follows.

D. Divider

Modeling of the divider will be accomplished by first relating the PFD pulse widths, Δt_k, to the VCO phase deviations, $\Phi_{\mathrm{out}}(t)$, and the divide value sequence, $N[k]$. Given this relationship, the divider model is "backed out" using the PFD gain expression in (1).

We begin by noting that the divider output edges occur whenever the absolute VCO phase, $\Phi_{\mathrm{vco}}(t)$, completes $2\pi N[k]$ radian increments of phase. As stated in (4), $\Phi_{\mathrm{vco}}(t)$ is composed of a ramp in time, $2\pi f_{\mathrm{nom}} t$, and phase variations, $\Phi_{\mathrm{out}}(t)$. These statements are collectively illustrated in Fig. 5. Note that changes in $N[k]$ occur at the rising edges of the divider.

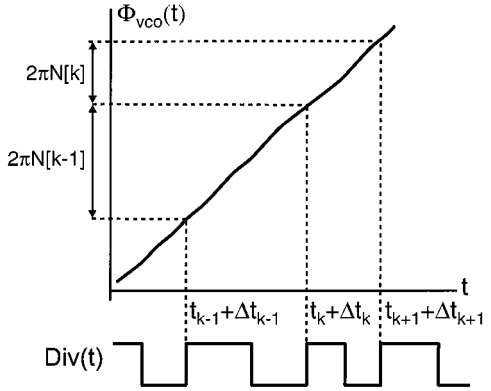

Fig. 5. Relationship of divider edges to instantaneous VCO phase, $\Phi_{\rm vco}(t)$.

Now, we can relate Δt_k to the VCO phase signal and divider sequence using (4) and Fig. 5. The first of two key equations is derived from Fig. 5 as

$$\Phi_{\rm vco}(t_k+\Delta t_k)-\Phi_{\rm vco}(t_{k-1}+\Delta t_{k-1})=2\pi N[k-1]. \quad (5)$$

The second key equation is obtained by evaluating (4) at time instants $t_k+\Delta t_k$ and $t_{k-1}+\Delta t_{k-1}$ and subtracting the resulting expressions:

$$\begin{aligned}&\Phi_{\rm vco}(t_k+\Delta t_k)-\Phi_{\rm vco}(t_{k-1}+\Delta t_{k-1})\\&\quad=2\pi f_{\rm nom}(t_k+\Delta t_k-t_{k-1}-\Delta t_{k-1})\\&\qquad+\Phi_{\rm out}(t_k+\Delta t_k)-\Phi_{\rm out}(t_{k-1}+\Delta t_{k-1})\end{aligned}$$

which, since $t_k-t_{k-1}=T$ and $f_{\rm nom}T=N_{\rm nom}$, is equivalently written as

$$\begin{aligned}&\Phi_{\rm vco}(t_k+\Delta t_k)-\Phi_{\rm vco}(t_{k-1}+\Delta t_{k-1})\\&\quad=2\pi N_{\rm nom}+2\pi f_{\rm nom}(\Delta t_k-\Delta t_{k-1})\\&\qquad+\Phi_{\rm out}(t_k+\Delta t_k)-\Phi_{\rm out}(t_{k-1}+\Delta t_{k-1}). \quad (6)\end{aligned}$$

We combine the two key equations into one formulation by substitution of (6) into (5):

$$\begin{aligned}&2\pi N_{\rm nom}+2\pi f_{\rm nom}(\Delta t_k-\Delta t_{k-1})\\&\qquad+\Phi_{\rm out}(t_k+\Delta t_k)-\Phi_{\rm out}(t_{k-1}+\Delta t_{k-1})\\&\quad=2\pi N[k-1].\end{aligned}$$

Rearrangement of this last expression then produces

$$\begin{aligned}&2\pi f_{\rm nom}(\Delta t_k-\Delta t_{k-1})\\&\quad=2\pi(N[k-1]-N_{\rm nom})-(\Phi_{\rm out}(t_k+\Delta t_k)\\&\qquad-\Phi_{\rm out}(t_{k-1}+\Delta t_{k-1})). \quad (7)\end{aligned}$$

Equation (7) is a difference equation relating all variables of interest; to remove the differences we sum the formulation over all positive time samples up to sample k:

$$\begin{aligned}&\sum_{m=1}^{k}(2\pi f_{\rm nom}(\Delta t_m-\Delta t_{m-1})\\&\quad=\sum_{m=1}^{k}(2\pi(N[m-1]-N_{\rm nom})\\&\qquad-(\Phi_{\rm out}(t_m+\Delta t_m)-\Phi_{\rm out}(t_{m-1}+\Delta t_{m-1}))).\end{aligned}$$

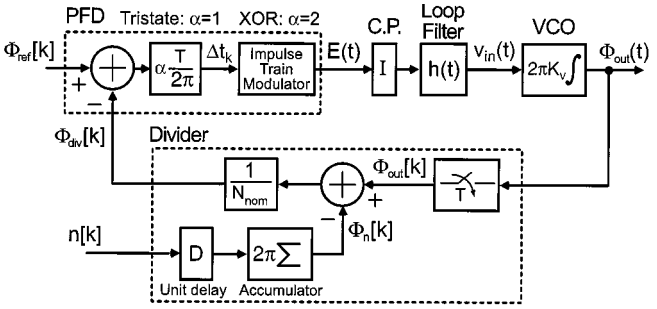

Fig. 6. Time-domain model of PLL.

Carrying out the summation operation, we obtain

$$\begin{aligned}2\pi f_{\rm nom}(\Delta t_k-\Delta t_0)=&\sum_{m=1}^{k}2\pi(N[m-1]-N_{\rm nom})\\&-(\Phi_{\rm out}(t_k+\Delta t_k)-\Phi_{\rm out}(t_0+\Delta t_0)).\end{aligned}$$

Assuming initial conditions are zero, this last expression becomes

$$\begin{aligned}&2\pi f_{\rm nom}\Delta t_k\\&\quad=\sum_{m=1}^{k}2\pi(N[m-1]-N_{\rm nom})-\Phi_{\rm out}(t_k+\Delta t_k). \quad (8)\end{aligned}$$

The final form of the desired equation is obtained by modifying (8) according to the following statements:

- Define $n[k]=N[k]-N_{\rm nom}$, $\Phi_{\rm out}[k]=\Phi_{\rm out}(t_k)$, $f_{\rm nom}=N_{\rm nom}(1/T)$.
- Approximate $\Phi_{\rm out}(t_k+\Delta t_k)\approx\Phi_{\rm out}(t_k)$.

As such, we obtain

$$\Delta t_k=\left(\frac{T}{2\pi}\right)\left(\frac{1}{N_{\rm nom}}\right)\left(2\pi\sum_{m=1}^{k}n[m-1]-\Phi_{\rm out}[k]\right). \quad (9)$$

We obtain the desired divider model by replacing Δt_k with the PFD gain expression in (1) and assuming $\Phi_{\rm ref}[k]$ is zero.

$$\Phi_{\rm div}[k]=\frac{1}{N_{\rm nom}}\left(-2\pi\sum_{m=1}^{k}n[m-1]+\Phi_{\rm out}[k]\right). \quad (10)$$

It is important to note that the only approximation made in deriving (10) is that $\Phi_{\rm out}(t_k+\Delta t_k)\approx\Phi_{\rm out}(t_k)$. Essentially, we are ignoring the nonuniform time sampling of the VCO phase deviations. As discussed in [13] and verified by actual implementations [9], [10], this approximation is quite accurate in practice even when the PLL is modulated.

E. Charge Pump and Loop Filter

The charge pump and loop filter relate the PFD output $E(t)$ to the VCO input $V_{\rm in}(t)$. We model the charge pump as a simple scaling operation on $E(t)$ of value I. The time domain model of the loop filter is characterized by its impulse response, $h(t)$.

F. Overall Model

We now combine the results of Section III-A–E to obtain the overall time-domain PLL model shown in Fig. 6. The PFD model is obtained from (1) and (2), the divider model from (10), and the VCO model from (3). As discussed earlier, the

XOR-based PFD has a factor of two larger gain than the tristate design, which is captured by the α factor in the PFD model. For convenience in analysis to follow, we also define an abstract signal, $\Phi_n[k]$, as the output of the divider accumulation action.

Some observations are in order. First, the divider effectively samples the continuous-time output phase deviation of the VCO, $\Phi_{\rm out}(t)$, and then divides its value by $N_{\rm nom}$. The output phase of the divider, $\Phi_{\rm div}[k]$, is influenced by the *integration* of deviations in the divider value, $n[k]$. The integration of $n[k]$ is a consequence of the fact that the divider output is a *phase* signal, whereas $n[k]$ causes an incremental change in the *frequency* of the divider output. Second, the PFD, charge pump, and loop filter translate the discrete-time error signal formed by $\Phi_{\rm ref}[k]$ and $\Phi_{\rm div}[k]$ to the continuous-time input of the VCO, $V_{\rm in}(t)$. These elements, along with the divider, also act as a D/A converter for mapping changes in $n[k]$ to $V_{\rm in}(t)$.

IV. Frequency-Domain PLL Model

Derivation of a frequency-domain model of the PLL is complicated by the sampling operation and impulse train modulator shown in Fig. 6. We discuss a simple approximation for the sampling operation and impulse train modulator that results in a linear time-invariant PLL model. This method, known as pseudocontinuous analysis [16], takes advantage of the fact that the impulsive output of the PFD is low-pass filtered in continuous time by the loop filter.

A. Pseudocontinuous Approximation

Consider a signal $x(t)$ that is sampled with period T and then converted to an impulse sequence $\hat{x}(t)$, as described by

$$\hat{x}(t) = \sum_{k=-\infty}^{\infty} x[k]\delta(t-kT)$$

where $x[k] = x(kT)$. The frequency-domain relationship between $\hat{x}(t)$ and $x(t)$ is found by taking the Fourier transform of the above expression, which leads to

$$\hat{X}(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X\left(f-\frac{k}{T}\right).$$

This expression reveals that the Fourier transform of $\hat{x}(t)$, $\hat{X}(f)$, is composed of multiple copies of the Fourier transform of $x(t)$, $X(f)$, that are scaled in magnitude by $1/T$ and shifted in frequency from one another with spacing $1/T$. We assume that the frequency content of $X(f)$ is confined to frequencies between $-1/(2T)$ and $1/(2T)$, so that negligible aliasing occurs between the copies of $X(f)$ within $\hat{X}(f)$.

Developing a frequency-domain model relating $\hat{X}(f)$ to $X(f)$ is complicated by the many copies of $X(f)$ in $\hat{X}(f)$ that occur due to the sampling operation. However, if we assume that $\hat{x}(t)$ is fed into a continuous-time low-pass filter with sufficiently low bandwidth, we can obtain a simple approximation of the relationship between $\hat{X}(f)$ and $X(f)$. Fig. 7 graphically illustrates a frequency-domain view of the sampling operation and the impact of following it with a continuous-time low-pass filter of bandwidth less than $1/(2T)$. The low-pass filter significantly attenuates all of the replicated copies of $X(f)$ within $\hat{X}(f)$ except for the baseband copy, which allows us to approximate the relationship between $\hat{x}(t)$ and $x(t)$ in the frequency domain as a simple scaling operation of $1/T$. In so doing, we ignore aliasing effects that will occur if there is frequency content in $X(f)$ at frequencies beyond the range of $-1/(2T)$ to $1/(2T)$. However, our analysis will be reasonably accurate when performing closed-loop analysis for most frequencies of interest in our application. The double outline of the box in the figure is meant to serve as a reminder that a sampling operation is taking place.

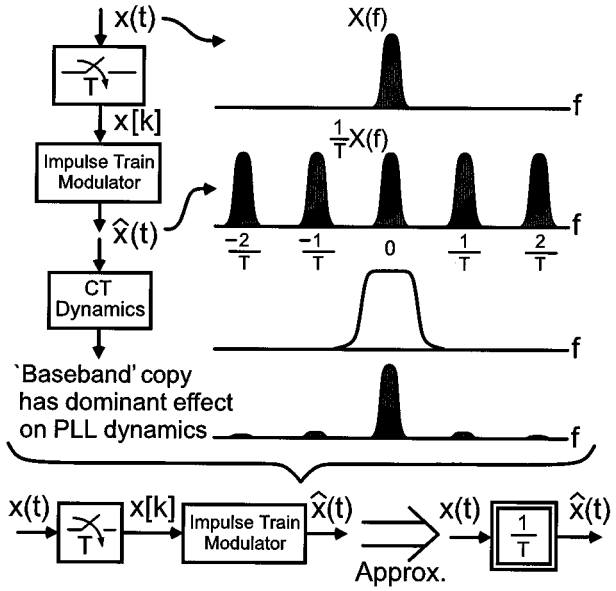

Fig. 7. Pseudocontinuous method of modeling a sampling operation in the frequency domain.

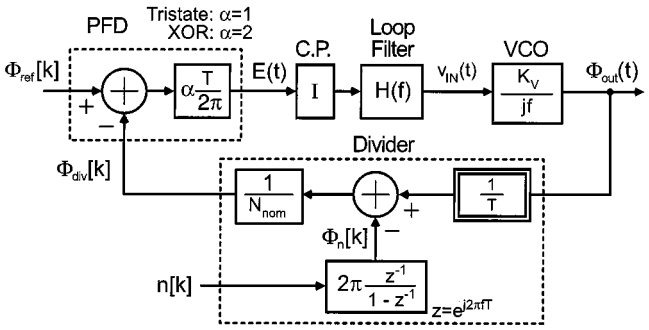

Fig. 8. Frequency-domain model of PLL.

B. Resulting Model

The time-domain block diagram in Fig. 6 is now readily converted to the frequency domain by taking the Z-transform of the discrete-time blocks, the Fourier transform of the continuous-time blocks, and by applying the approximation of the sampling operation discussed above. Fig. 8 displays the resulting model. Note that all blocks are parameterized by the common variable f, which denotes frequency in hertz, under the assumption that all discrete-time sequences interact with the continuous-time blocks as modulated impulse trains of period T. Also note that all the *signals* in the PLL are still denoted in the time domain even though they interact

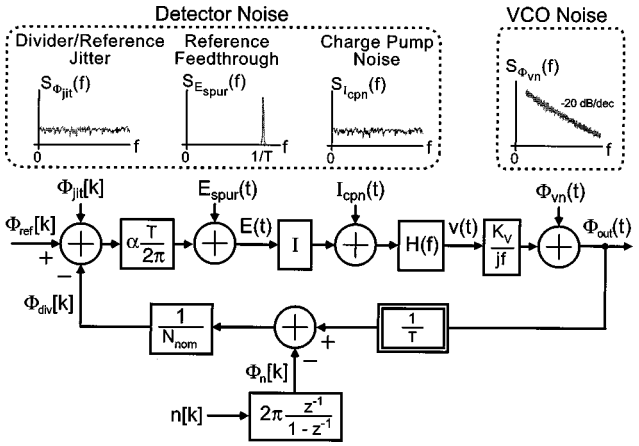

Fig. 9. Detailed view of PLL noise sources and examples of their respective spectral densities.

through frequency-domain blocks. The reason for this notation convention is that, in practice, these signals are stochastic and do not have defined Fourier transforms, but rather are described by their power spectral densities.

V. Parameterization of PLL

We now parameterize the PLL dynamics depicted in Fig. 8 in terms of a single function which we will call $G(f)$. Using this parameterization, we then develop a general noise model for frequency synthesizers in which all the relevant transfer functions are described in terms of $G(f)$.

A. Derivation

To parameterize the PLL dynamics, it is convenient to define a base function that provides a simple description of all the PLL transfer functions of interest. It turns out that the following definition works well for this purpose.

$$G(f) = \frac{A(f)}{1 + A(f)} \tag{11}$$

where $A(f)$ is the open-loop transfer function of the PLL:

$$A(f) = \left(\frac{\alpha}{2\pi}\right) IH(f) \left(\frac{K_v}{jf}\right) \left(\frac{1}{N_{\text{nom}}}\right). \tag{12}$$

Since $A(f)$ is low pass in nature with infinite gain at dc, $G(f)$ has the following properties:

$$\begin{aligned} G(f) &\longrightarrow 1 \text{ as } f \longrightarrow 0 \\ G(f) &\longrightarrow 0 \text{ as } f \longrightarrow \infty \end{aligned} \tag{13}$$

implying that $G(f)$ is a low-pass filter with a low frequency gain of one.

One may try to tie an intrinsic meaning to $G(f)$ in terms of PLL behavior. However, it is meant only as a convenient vehicle for compactly describing the PLL transfer functions of interest, as will be shown later in this section.

B. Application to Noise Analysis

The derived parameterization allows straightforward calculation of the noise performance of a synthesizer as a function of various noise sources in the PLL, which are shown in Fig. 9.

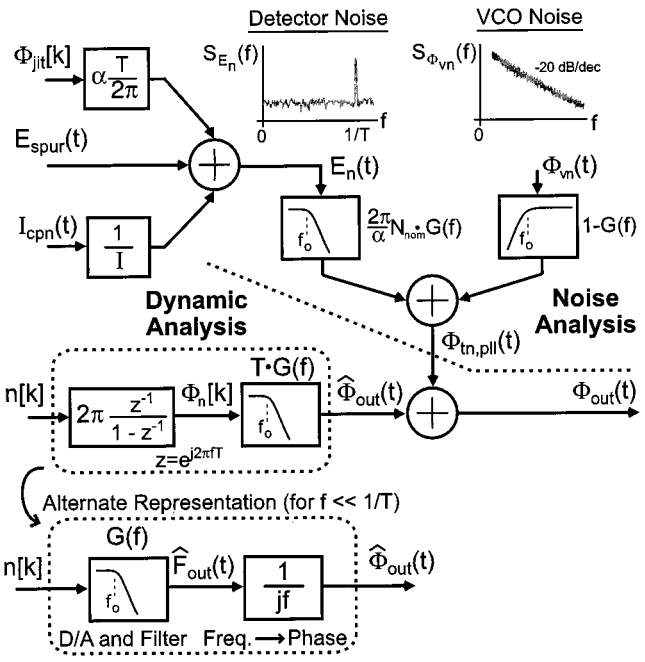

Fig. 10. Parameterized model of PLL for dynamic response and noise calculations.

Divider/reference jitter, $\Phi_{\text{jit}}[k]$, corresponds to noise-induced variations in the transition times of the Reference or Divider output waveforms. A periodic reference spur $E_{\text{spur}}(t)$ is caused by use of the XOR-based PFD, or by the tristate PFD when its output duty cycle is nonzero. Charge-pump noise is caused by noise produced in the transistors that compose the charge-pump circuit. Finally, VCO noise includes the intrinsic noise of the VCO and voltage noise at the output of the loop filter. For convenience in later discussion, we have lumped these noise sources into two categories, VCO noise and detector noise, as shown in Fig. 9.

Fig. 10 displays the transfer function relationships from each of the above noise sources to the synthesizer output. The derivation of these transfer functions is straightforward based on Fig. 9 and the $G(f)$ parameterization derived earlier. Note that two different parameterizations are shown to describe the impact of divide value variations on the PLL output phase. The alternate model relates changes in the divide value, $n[k]$, more directly to the PLL output frequency. Its derivation follows by noting that the order of linear time-invariant blocks can be switched, and that

$$\begin{aligned} \frac{z^{-1}}{1 - z^{-1}} &= \frac{e^{-j2\pi fT}}{1 - e^{-j2\pi fT}} \\ &\approx \frac{1 - j2\pi fT}{1 - (1 - j2\pi fT)} \\ &\approx \frac{1}{j2\pi fT}, \qquad \text{for } f \ll \frac{1}{T}. \end{aligned}$$

Note that the validity of the dynamic model, and its alternate, presented in Fig. 10, has been verified in previous work discussed in [9], [13]. The validity of the noise model will be verified in Section VII.

Calculation of spectral noise densities using Fig. 10 is complicated by the fact that both discrete-time (DT) and

continuous-time (CT) signals are present. Three cases are of significance, and their respective spectral noise calculations are as follows [17]:

Case 1) CT input $x(t)$ fed into CT filter $H(f)$ to produce a CT output $y(t)$:

$$S_y(f) = |H(f)|^2 S_x(f). \tag{14}$$

Case 2) DT input $x[k]$ fed into DT filter $H(e^{j2\pi fT})$ to produce a DT output $y[k]$:

$$S_y(e^{j2\pi fT}) = |H(e^{j2\pi fT})|^2 S_x(e^{j2\pi fT}). \tag{15}$$

Case 3) DT input $x[k]$ fed into CT filter $H(f)$ to produce a CT output $y(t)$:

$$S_y(f) = \frac{1}{T}|H(f)|^2 S_x(e^{j2\pi fT}). \tag{16}$$

In Case (3), we assume that the DT input interacts with the CT filter as a modulated impulse train of period T.

The above spectral density calculations and Fig. 10 allow us to accurately calculate the influence of the various noise sources on the PLL output. A few qualitative observations are also in order. Detector noise is low-pass filtered by the PLL dynamics, while VCO noise is high-pass filtered by the PLL dynamics. The overall noise power in the PLL output, whose integral over frequency corresponds to the time-domain jitter of the PLL output, is a function of the PLL bandwidth. If the PLL bandwidth is very low, VCO noise will dominate over a wide frequency range due to the abundant suppression of detector noise. Likewise, a high PLL bandwidth will suppress VCO noise over a wide frequency range at the expense of allowing more detector noise through.

VI. Σ–Δ Synthesizer Model

We are now ready to incorporate the Σ–Δ modulator into the general PLL model. We do so by first providing a brief description of Σ–Δ modulator fundamentals, and then provide intuition to the means by which they increase the frequency resolution of a synthesizer compared to a classical implementation in which the divider value is held constant. Finally, we present a frequency-domain model of the Σ–Δ synthesizer and use it to calculate the impact of the Σ–Δ quantization noise on the PLL output phase.

A. Σ–Δ Modulator

A Σ–Δ modulator achieves a high-resolution signal using only a few output levels. To do this, the modulator dithers its output at a high rate such that the "average" value of the dithered sequence corresponds to a high-resolution input signal whose energy is confined to low frequencies. Appropriate filtering of the output sequence removes quantization noise produced by the dithering, which yields a high-resolution signal closely matching that of the input.

In Σ–Δ synthesizer applications, it is important to note that the Σ–Δ modulator is *purely digital* in its implementation. Thus, Σ–Δ structures that are difficult to implement in the analog world due to high matching requirements, such as the MASH (or cascaded) architecture [18], [19], are trivial to implement in this application due to the precise matching offered by digital circuits.

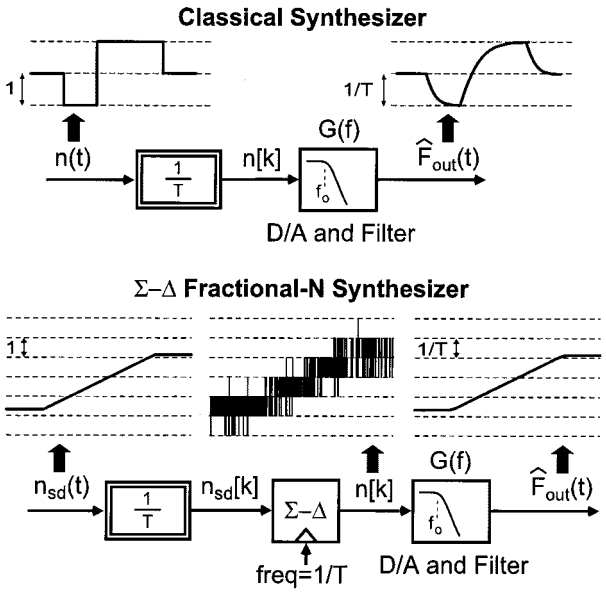

Fig. 11. Illustration of dithering action of Σ–Δ modulator.

In general, modeling of a Σ–Δ modulator is accomplished by assuming its quantization noise is independent of its input [19]. This leads to a linear time-invariant model that is parameterized by transfer functions from the input and quantization noise to the output. For instance, a MASH Σ–Δ modulator structure [19] of order m, input $x[k]$, and output $y[k]$ is described by

$$y(z) = x(z) - (1 - z^{-1})^m r(z). \tag{17}$$

Thus, the modulator passes its input to the output along with quantization noise, $r[k]$, that is *shaped* by the filter $(1-z^{-1})^m$. Ideally, $r[k]$ is white and uniformly distributed between 0 and 1 so that its spectrum is flat and of magnitude $1/12$ [20], [21].

It is convenient to parameterize the Σ–Δ modulator in terms of two transfer functions. The signal transfer function (STF) of the Σ–Δ modulator is defined from the input $x[k]$ to output $y[k]$, while the noise transfer function (NTF) is defined from the base quantization noise $r[k]$ to the output. Inspection of (17) reveals that a MASH structure of order m is parameterized as

$$\text{STF:} \quad H_s(z) = 1$$
$$\text{NTF:} \quad H_n(z) = (1 - z^{-1})^m|_{z=e^{-j2\pi fT}}.$$

B. Application to PLL

To understand the impact of using a Σ–Δ modulator to control the divide value in a frequency synthesizer, Fig. 11 contrasts the way the divide value is varied in classical versus Σ–Δ fractional-N frequency synthesizers based on the alternate model in Fig. 10. Note that the divide value variations are cast as continuous-time signals to get the proper scale factor such that a unit change in divide value yields an output frequency change of $1/T$ Hz. In the classical case, the divide value is static except when the output frequency is changed, and the PLL output frequency responds to the change according to the low-pass nature of the PLL dynamics $G(f)$. In contrast, a Σ–Δ fractional-N

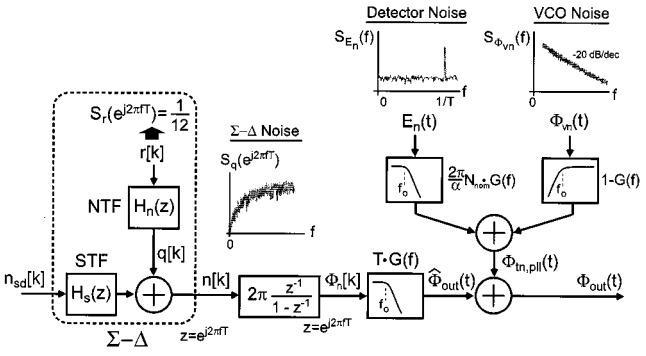

Fig. 12. Parameterized model of a Σ–Δ synthesizer.

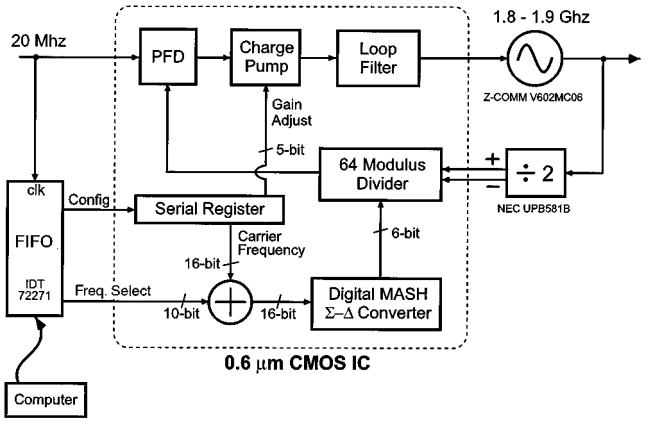

Fig. 13. Block diagram of prototype system.

synthesizer constantly dithers the divide value at a high rate compared to the bandwidth of $G(f)$ such that $G(f)$ extracts out its low-frequency content. The low frequency content of the Σ–Δ output is, in turn, set by the Σ–Δ input $n_{sd}[k]$, which can have arbitrarily high resolution. Thus, the Σ–Δ modulator allows the PLL output frequency to be controlled to a very high resolution *independent* of the reference frequency—a high reference frequency can be used while simultaneously achieving high-frequency resolution.

C. Frequency-Domain Model

To obtain the frequency-domain model of a Σ–Δ synthesizer, we simply extend the PLL model in Fig. 10 to include the Σ–Δ modulator, as shown in Fig. 12. This figure depicts a general model of a Σ–Δ modulator which is characterized by its STF and NTF. The base quantization noise $r[k]$ is assumed ideal (i.e., white) in the illustration.

Fig. 12 offers several insights to the fundamentals of Σ–Δ frequency synthesis. First, we see that the shaped Σ–Δ quantization noise passes through a digital accumulator and then the PLL dynamics, $G(f)$, before impacting the output phase of the PLL. The digital accumulator, a consequence of the integrating nature of the divider, effectively reduces the noise-shaping order of the Σ–Δ by one. The PLL dynamics, $G(f)$, act to remove the high-frequency quantization noise produced by the Σ–Δ modulator. The Σ–Δ quantization noise adds an additional noise source to those already present in the PLL, but the relationship from each noise source to the output phase remains purely a function of $G(f)$ and the nominal divide value.

D. Quantization Noise Impact on PLL

As Fig. 12 reveals, a Σ–Δ synthesizer's noise performance is impacted by the Σ–Δ quantization noise in addition to the intrinsic detector and VCO noise sources found in the classical PLL. Calculation of this impact is straightforward using the presented modeling approach. For example, given the NTF of an mth order MASH structure is $(1-z^{-1})^m$, we calculate the impact of its quantization noise on the PLL output using Fig. 12 and (16) as

$$S_{\Phi_{\text{out}}}(f) = \frac{1}{T}\left|T\cdot G(f)\right|^2 \left|2\pi\frac{e^{-j2\pi fT}}{1-e^{-j2\pi fT}}\right|^2 \times \left|(1-e^{-j2\pi fT})^m\right|^2 S_r(f)$$

which is also expressed as

$$S_{\Phi_{\text{out}}}(f) = \frac{1}{T}\left|T\cdot G(f)\right|^2 \left((2\pi)^2(2\sin(\pi fT))^{2(m-1)}\right) S_r(f). \tag{18}$$

If the quantization noise spectra of $r[k]$ is white, then

$$S_r(f) = \frac{1}{12}$$

as previously discussed. In many cases, $r[k]$ is not white and must be computed numerically by simulating the Σ–Δ modulator at a given value of $n_{sd}[k]$.

Equation (18) shows that the Σ–Δ quantization noise is reduced in order by one due to the integrating action of the divider. Assuming $r[k]$ is white, the shaped noise rises at $(m-1)20$ dB/decade for frequencies $\ll 1/T$. Therefore, if the order of $G(f)$ is chosen to be the same as the order of the Σ–Δ, the quantization noise seen at the PLL output will roll off at −20 dB/decade outside the PLL bandwidth. This rolloff characteristic matches that of the VCO noise.

VII. Results

The above methodology is now used to analyze the noise performance of a prototype system described in [9], [13]. Fig. 13 displays a block diagram of the prototype, which consists of a custom CMOS fractional-N synthesizer IC that includes an XOR-based PFD, an on-chip loop filter that uses switched capacitors to set its time constant, a second-order digital MASH Σ–Δ modulator, and an asynchronous 64-modulus divider that supports any divide value between 32 and 63.5 in half-cycle increments. An external divide-by-2 prescaler is used so that the CMOS divider input operates at half the VCO frequency, which modifies the range of divide values to include all integers between 64 and 127. A computer interface is used to set the digital frequency value that is fed into the input of the Σ–Δ modulator.

A. Modeling

A linearized frequency-domain model of the prototype system is shown in Fig. 14. The open-loop transfer function of the system consists of two integrators, a pole at f_p and a zero at f_z. Additional poles and zeros occur in the system due to the effects of finite opamp bandwidth and other nonidealities,

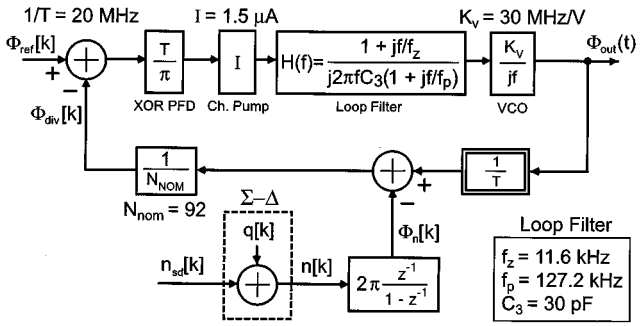

Fig. 14. Linearized frequency-domain model of prototype system.

but are not significant for the analysis to follow. The $G(f)$ parameterization is calculated from Fig. 14 and (11) as

$$G(f) = \frac{1 + \dfrac{jf}{f_z}}{1 + \dfrac{jf}{f_{\rm cp}}} \left(\frac{1}{1 + \dfrac{jf}{(f_o Q)} + \left(\dfrac{jf}{f_o}\right)^2} \right). \tag{19}$$

The parameters of the system were set such that the PLL had a bandwidth of 84 kHz:

$$\begin{aligned} f_o &= 84.3 \text{ kHz} \\ f_z &= 11.6 \text{ kHz} \\ f_{\rm cp} &= 14.2 \text{ kHz} \\ Q &= 0.75. \end{aligned} \tag{20}$$

Fig. 15 expands the block diagram of the prototype to indicate the circuits of relevance and their respective noise contributions. A few comments are in order. First, a reference frequency $1/T$ of 20 MHz was chosen to achieve an acceptably low impact of Σ–Δ quantization noise while still allowing low-power implementation of the digital logic. This choice of reference frequency, in turn, required that $N_{\rm nom} = 92$ to achieve an output carrier frequency of 1.84 GHz. The value of K_v was set to 30 MHz/V by the external VCO. The value of C_3 was chosen as large as practical in order to obtain good noise performance; it was constrained to 30 pF due to area constraints on the die of the custom IC.

B. Noise Analysis

Table I displays the value of each noise source shown in Fig. 15. Many of these values were obtained through ac simulation of the relevant circuits in HSPICE. Note that all noise sources other than $q[k]$ are assumed to be white, so that the values of their variance suffice for their description. This assumption holds for the input-referred VCO noise, $v_{\rm vco,in}(t)$, provided that the output phase noise of the VCO rolls off at -20 dB/dec [22], [23]; the -20 dB/dec rolloff is achieved in the model since $v_{\rm vco,in}(t)$, which has a flat spectral density, passes through the integrating action of the VCO. The actual VCO deviates from the -20 dB/dec rolloff at low frequencies due to $1/f$ noise, and at high frequencies due to a finite noise floor. However, the assumption of -20 dB/dec rolloff suffices for the frequency offsets of interest.

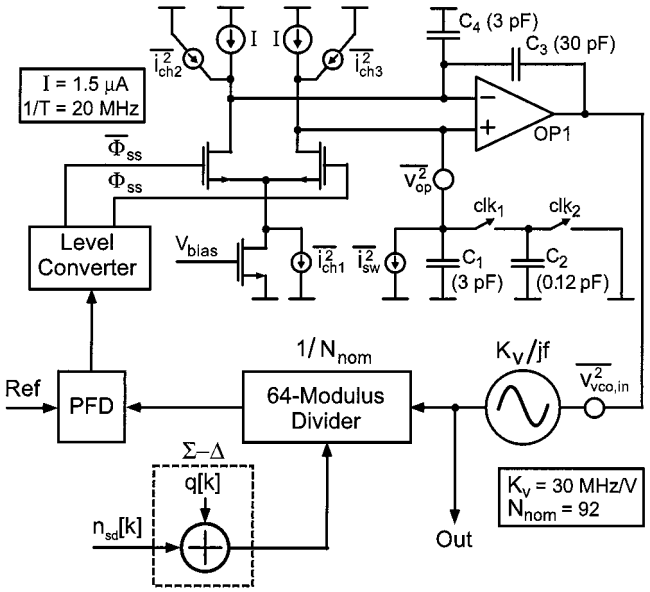

Fig. 15. Expanded view of PLL System.

TABLE I
VALUES OF NOISE SOURCES WITHIN PLL

Noise Source	Origin	Nature	Calculation	Value
$\overline{i^2_{ch1}}$	Ch. Pump, OP1	CT	HSPICE	1.2E-24 A^2/Hz
$\overline{i^2_{ch2}}$, $\overline{i^2_{ch3}}$	Ch. Pump	CT	HSPICE	1.8E-25 A^2/Hz
$\overline{i^2_{sw}}$	Switched Cap	DT	Equation 22	1.0E-26 A^2/Hz
$\overline{v^2_{op}}$	OP1	CT	HSPICE	1.85E-16 V^2/Hz
$\overline{v^2_{vco,in}}$	VCO	CT	Equation 21	1.4E-16 V^2/Hz
$q[k]$	Σ-Δ	DT	Equation 23	—

The input-referred noise of the VCO was calculated from an open-loop VCO phase noise measurement (shown in Fig. 17) at 5-MHz frequency offset as

$$10 \log \left(\overline{v^2_{\rm vco,in}} \left| \frac{K_v}{(jf)} \right|^2 \right) = -143 \text{ dBc/Hz} \quad \text{at } f = 5 \text{ MHz} \tag{21}$$

where K_v is 30 MHz/V. The value of the kT/C noise current produced by the switched-capacitor operation $\overline{i^2_{\rm sw}}$ was calculated as

$$\overline{i^2_{\rm sw}} = \left(\frac{1}{T}\right) kT_{\rm K} C_2 \tag{22}$$

where k is Boltzmann's constant, and $T_{\rm K}$ is temperature in degrees Kelvin. Finally, the spectral density of the Σ–Δ quantization noise was calculated as

$$S_q(f) = \frac{1}{12} \left(2 \sin(\pi f T)\right)^{2m} \tag{23}$$

where $m = 2$ is the order of the Σ–Δ modulator.

The noise sources in Table I can be classified as either charge-pump noise, VCO noise, or Σ–Δ quantization noise, which we denote as $i_{\rm cp}(t)$, $v_{\rm vco}(t)$, and $q[k]$, respectively. For convenience, we will assume that $v_{\rm vco}(t)$ is referred to the input of the VCO, so that it passes through the transfer function $K_v/(jf)$ before influencing the VCO output phase. Given the

values of these sources, the overall noise spectral density at the synthesizer output $S_{\Phi_{\rm tn}}(f)$ is described as

$$S_{\Phi_{\rm tn}}(f) = S_{\Phi_{\rm cp}}(f) + S_{\Phi_{\rm vco}}(f) + S_{\Phi_q}(f) \tag{24}$$

where $S_{\Phi_{\rm cp}}(f)$, $S_{\Phi_{\rm vco}}(f)$, and $S_{\Phi_q}(f)$ are the contributions from $i_{\rm cp}(t)$, $v_{\rm vco}(t)$, and $q[k]$, respectively. $S_{\Phi_q}(f)$ is given by (18) with $m = 2$. $S_{\Phi_{\rm cp}}(f)$ and $S_{\Phi_{\rm vco}}(f)$ are calculated from Fig. 10 and (14) as

$$S_{\Phi_{\rm cp}}(f) = \overline{i_{\rm cp}^2}\left(\frac{\pi N_{\rm nom}}{I}\right)^2 |G(f)|^2$$
$$S_{\Phi_{\rm vco}}(f) = \overline{v_{\rm vco}^2}\left|\frac{K_v}{(jf)}\right|^2 |1 - G(f)|^2 . \tag{25}$$

Note that we have assumed that $i_{\rm cp}(t)$ and $v_{\rm vco}(t)$ are white, and that $\alpha = 2$ since an XOR-based PFD is used.

The task that remains is to determine the values of $i_{\rm cp}(t)$ and $v_{\rm vco}(t)$. Examination of Fig. 15 reveals that charge-pump noise is a function of the following noise sources:

$$\overline{i_{\rm cp}^2} = f_i\left(\overline{i_{\rm ch1}^2}, \overline{i_{\rm ch2}^2}, \overline{i_{\rm ch3}^2}, \overline{i_{\rm sw}^2}\right) \tag{26}$$

while VCO noise is a function of the noise sources

$$\overline{v_{\rm vco}^2} = f_v\left(\overline{v_{\rm vco,in}^2}, \overline{v_{\rm op}^2}\right). \tag{27}$$

We will quickly infer the value of the functions $f_i(\cdot)$ and $f_v(\cdot)$ in this paper; the reader is referred to [13] for more detail.

Let us first determine $f_i(\cdot)$. Examination of Table I reveals that $\overline{i_{\rm ch1}^2}$ is an order of magnitude larger than $\overline{i_{\rm ch2}^2}$, $\overline{i_{\rm ch3}^2}$, and $\overline{i_{\rm sw}^2}$. Since the $\overline{i_{\rm ch1}^2}$ noise source is switched alternately between the positive and negative terminals of OP1, its contribution to $i_{\rm cp}(t)$ will be pulsed in nature. At a nominal duty cycle of 50%, we would expect the energy of $\overline{i_{\rm ch1}^2}$ to be split equally between the positive and negative terminals of OP1. As such, $\overline{i_{\rm cp}^2}$ is then $\overline{i_{\rm ch1}^2}/2$. This intuitive argument was verified using a detailed C simulation of the PLL [24]. Note that a more accurate estimate of $\overline{i_{\rm cp}^2}$ will take into account any offset in the nominal duty cycle of the phase detector output, and the transient response of the charge pump.

Now let us determine $f_v(\cdot)$. Since Table I reveals that $\overline{v_{\rm vco}^2}$ is of the same order of $\overline{v_{\rm op}^2}$, we simply add these components to obtain $\overline{v_{\rm vco}^2} \approx \overline{v_{\rm vco}^2} + \overline{v_{\rm op}^2}$. This expression is accurate at frequencies less than the unity gain bandwidth of OP1; the $\overline{v_{\rm op}^2}$ noise source is passed to its output with a gain of approximately one in this region. At frequencies beyond OP1's bandwidth, the expression is conservatively high since $\overline{v_{\rm op}^2}$ is attenuated in this frequency range.

Based on the above information, plots of the spectra in (24) are shown in Fig. 16. For convenience, we have also overlapped measured results from Fig. 17 for easy comparison, which will be discussed shortly. As shown in Fig. 16, the influence of detector noise dominates at low frequencies, and the influence of VCO and Σ–Δ quantization noise dominate at high frequencies. Note that the calculations use $G(f)$ described by (19) with the parameter values specified in (20).

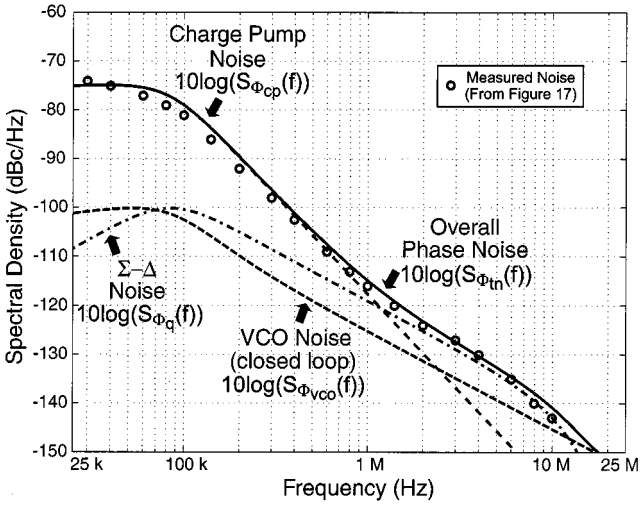

Fig. 16. Calculated noise spectra of synthesizer compared to measured results.

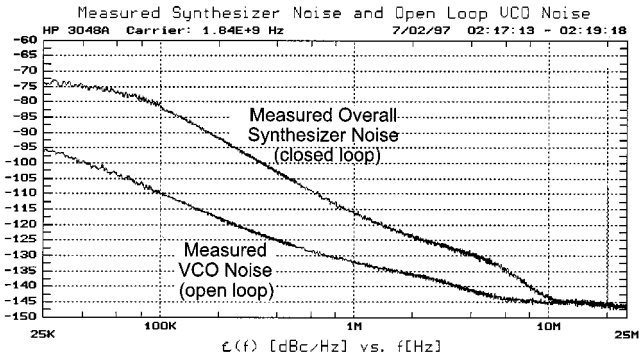

Fig. 17. Measured closed-loop synthesizer noise and open-loop VCO noise.

Fig. 17 shows measured plots of $S_{\Phi_{\rm tn}}(f)$ and the open-loop phase noise of the VCO from the synthesizer prototype; the plots were obtained from an HP 3048A phase-noise measurement system. It should be noted that the LSB of the Σ–Δ modulator was dithered to reduce spurious content, which was necessary due to the low order of the Σ–Δ modulator. The resulting spectra compare quite well with the calculated curve in Fig. 16 over the frequency offset range of 25 kHz to 10 MHz. Above 10 MHz, the phase-noise measurement was limited by the sensitivity of the measurement equipment. Note that the −60 dBc spur at 20-MHz offset is due to the 50% nominal duty cycle of the PFD; no effort was made to reduce it below this level during the design process since it was acceptable for the intended application of the prototype.

VIII. Conclusion

In this paper, we developed a general model of a PLL that incorporates the influence of divide value variations. A model for Σ–Δ fractional-N synthesizers was obtained by simply incorporating a Σ–Δ modulator model into this framework. The PLL model was parameterized by a single transfer function $G(f)$, which further simplifies noise calculations. The framework was used to calculate the noise performance of a custom Σ–Δ synthesizer, and was shown to accurately predict

measured results within 3 dB over a frequency offset range from 25 kHz to 10 MHz.

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