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Research Article

A Modified Seven-Level Inverter with Inverted Sine Wave Carrier for PWM Control

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The conventional multilevel inverter necessitates more active switching devices and high dc-link voltages. To minimalize the employment of switching devices and dc-link voltages, a novel topology has been proposed. In this paper, a novel minimum switch multilevel inverter is established using six switches and two dc-link voltages in the proportion of 1 : 2. In addition, the proposed topology is proficient in making seven-level voltages by appropriate gate signals. The PWM signals were produced using several inverted sine carriers and a single trapezoidal reference. When compared to other existing inverters, this configuration needs fewer components, as well as fewer gate drives. Furthermore, this module can generate a negative level without the use of a supplementary circuit such as an H-Bridge. As a result, overall cost and complexity are greatly reduced. The proposed minimum switch multilevel inverter operation is validated through simulations followed by experimental results of a prototype.

1. Introduction

The cascaded inverter, which is made up of a series of connected strings of a full-bridge inverter, has been presented in [1]. This structure can be functioned in both symmetric and uneven types based on the input source magnitude. Asymmetrical type inverter configuration required fewer cascaded bridges to achieve more output levels [2]. In [3], a new seven-level inverter scheme is proposed with six semiconductor switches and 3 dc capacitors. However, the voltage balancing of the capacitor is quite challenging. A new MLI topology with series connected dc voltage sources has been presented in [4]. To lower the switching losses, this structure includes a level generation and polarity generation portion. Increasing the output voltage, on the other hand, necessitates the use of more dc sources. In [5], MLI topologies with a capacitor selection circuit have been presented. However, obtaining distinct dc sources having multiple ratios necessitates the use of a front-end transformer. Transformers less switched capacitor inverter topology have been presented in [6]. However, the determination of capacitance value is quite complex. A 7-level configuration with a dc supply with and series of capacitors, diodes, and power semiconductor switches have been presented in [7]. It also uses a new switching strategy to solve voltage balancing problems in capacitors. However, the proposed configuration has a restriction on high-voltage applications. A medium-voltage hybrid seven-level cascaded inverter topology is presented in [8]. However, the circuit topology is more complicated because it requires a high number of switching devices. A packed U cell inverter configuration is presented in [9, 10] with a lower number of power semiconductor switches to high-voltage applications. However, exploiting power semiconductor switches with

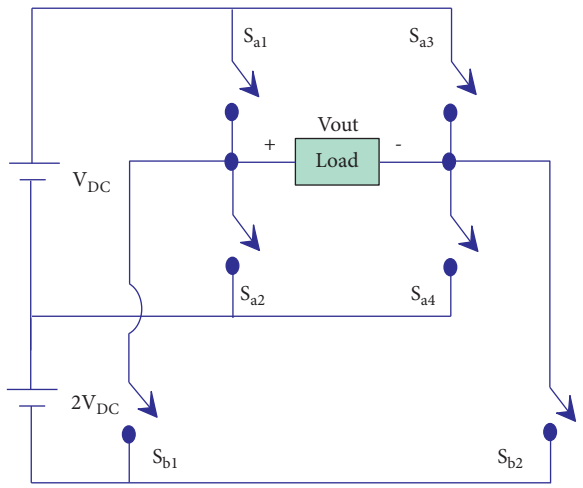


Figure 1: Proposed 7-level inverter configuration.

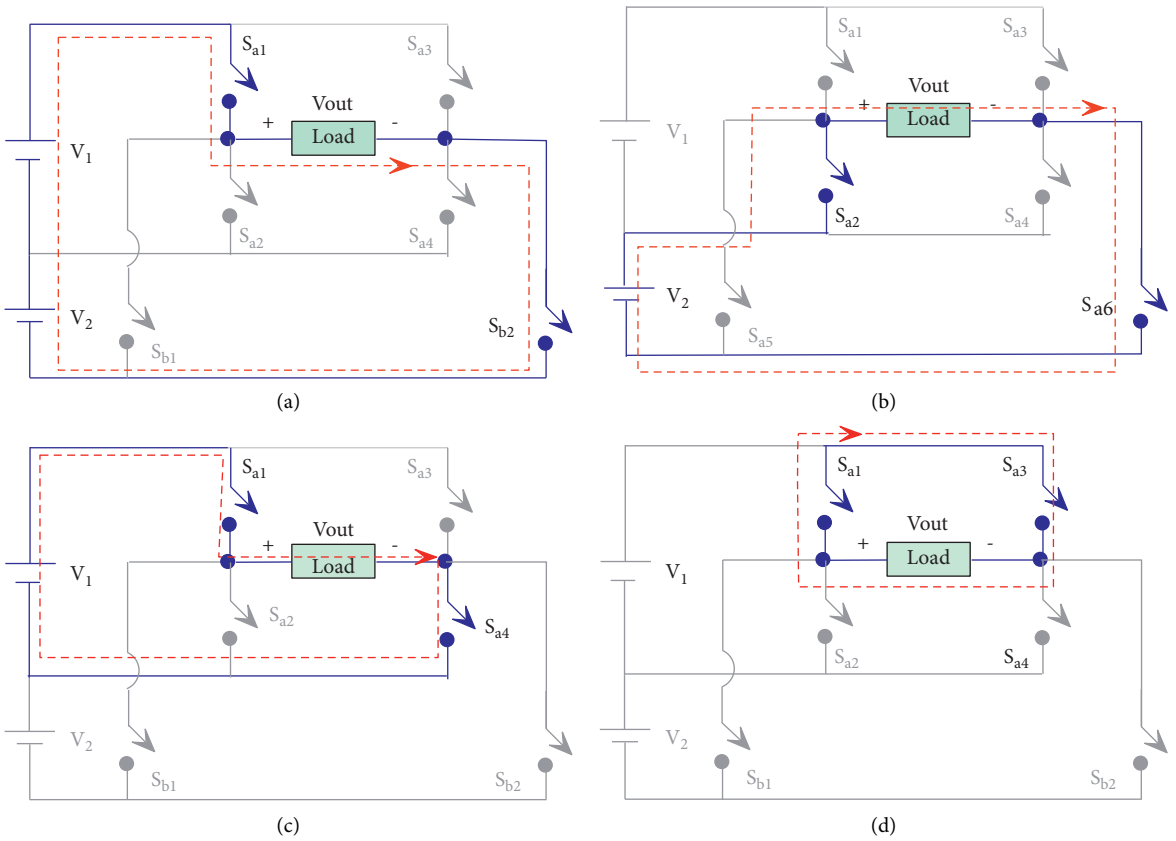
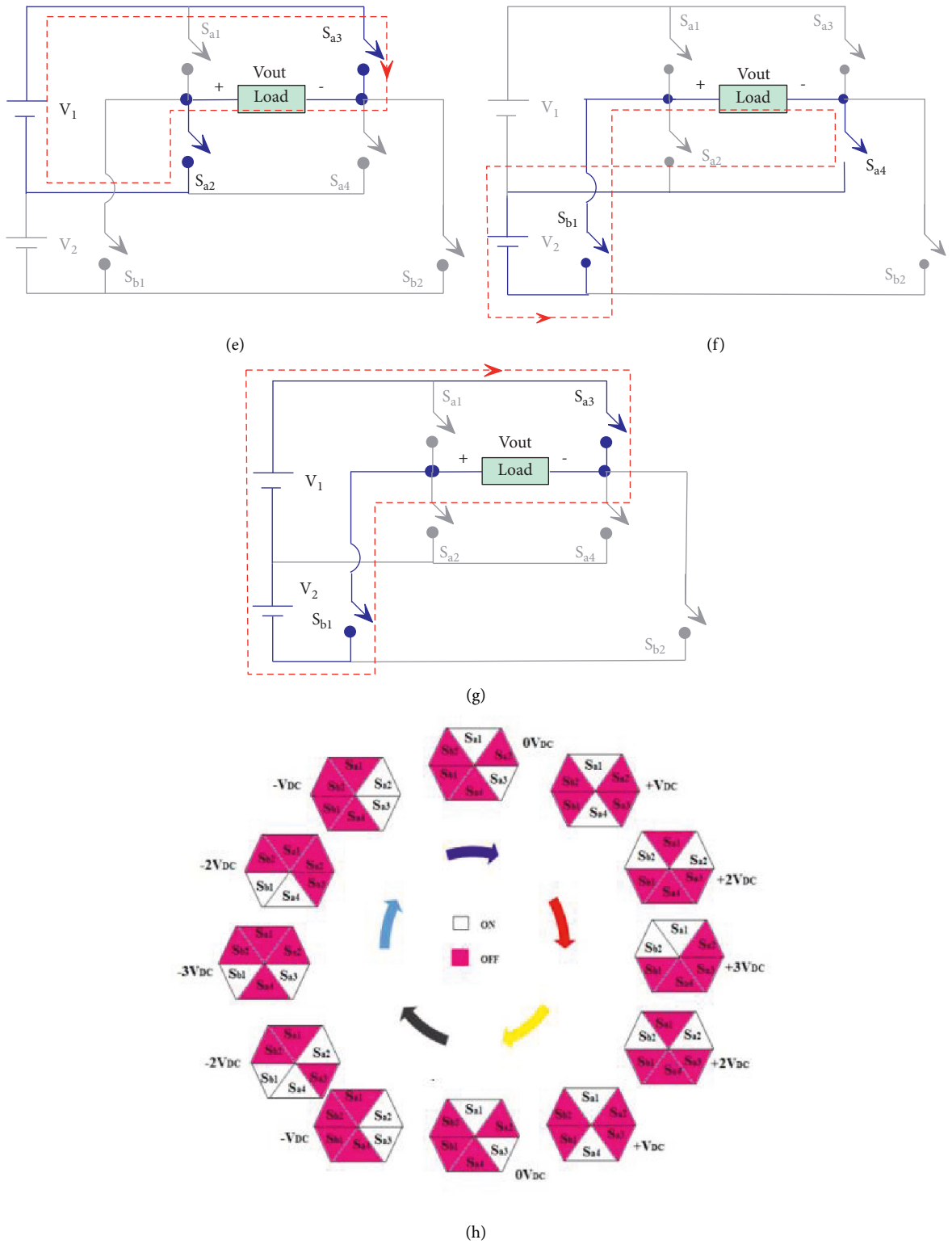


Figure 2: Continued.



(h)

FIGURE 2: (a) Current path and switching plan for making $+3V_{DC}$ at load. (b) Current path and switching plan for making $+2V_{DC}$ at load. (c) Current path and switching plan for making $+V_{DC}$ at load. (d) Current path and switching plan for making $0V_{DC}$ at load. (e) Current path and switching plan for making $-V_{DC}$ at load. (f) Current path and switching plan for making $-2V_{DC}$ at load. (g) Current path and switching plan for making $-3V_{DC}$ at load. (h) Cyclic switching sequence of chosen MLI.

Table 1: Voltage stress on switches.

Switch	Voltage stress
S_{a1}	$3V_{DC}$
S_{a2}	$2V_{DC}$
S_{a3}	$3V_{DC}$
S_{a4}	$2V_{DC}$
S_{b1}	$3V_{DC}$
S_{b2}	$3V_{DC}$

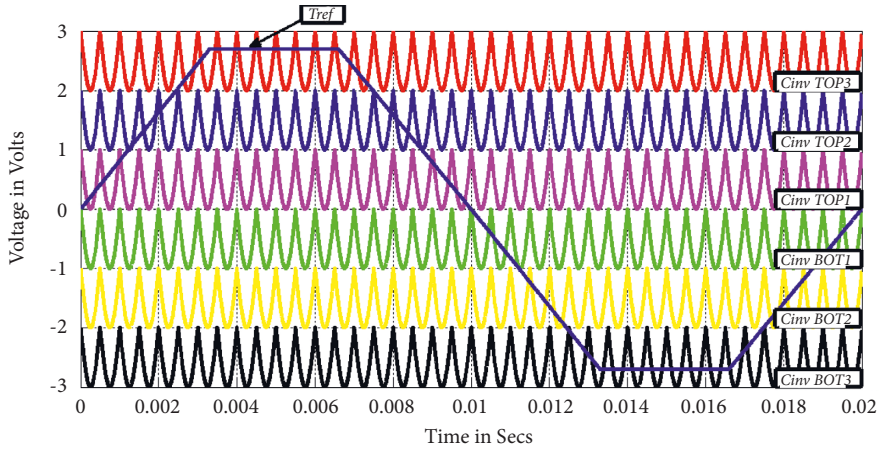


Figure 3: Graphic depiction of the PD-PWM scheme with inverted sine carrier and trapezoidal reference waveform.

Table 2: Comparison with recent past developed MLIs.

Parameter	Ref. no. [1]	Ref. no. [3]	Ref. no. [4]	Ref. no. [5]	Ref. no. [6]	Ref. no. [7]	Ref. no. [8]	Ref. no. [9]	Ref. no. [10]	Ref. no. [11]	Ref. no. [12]	Ref. no. [13]	Ref. no. [14]	Proposed
N_{Source}	1	1	3	1	1	1	2	1	2	1	1	1	4	2
$N_{capacitors}$	3	3	0	2	3	3	2	1	2	3	3	2	0	0
N_{Switch}	8	8	10	6	10	7	12	6	6	8	10	8	6	6
N_{Driver}	8	8	10	6	10	7	12	6	6	8	10	8	6	6
N_{Diode}	4	0	0	2	0	2	4	0	0	4	0	2	2	0

different ratings and frequencies is crucial. 7-level inverters designed with switched capacitors are described in [11–13]. To enhance the voltage level, however, the voltage across the dc-link capacitor should be enhanced. In addition, to minimize overall harmonic distortion, level shifted, phase shifted, and hybrid pulse width modulation (PWM) approaches are often used. The key challenges with these MLI topologies are improving efficiency by enhancing the quality of power using appropriate control and modulation techniques. Additionally, finding the exact modulation method for any kind of multilevel converter seems to be complicated [2, 14–16]. Drawing inspiration from early research, the article outlines a novel 7-level inverter based on a decreased number of parts, with a series of connected dc sources of binary sequence to achieve maximum capacity from dc sources by an appropriate organization of switches [17]. Symmetrical and asymmetrical MLI with lower switch count and dc sources are presented in [18–21]. However, these topologies need auxiliary circuits to generate negative levels.

The proposed inverter topology has the following merits over the inverter topology presented in recent past years.

(1) Simple structure with fewer semiconductor components and individual DC sources for each unit has great potential for the application of dispersed generation.

(2) It does not require any supplementary H-bridge unit to make negative polarity levels. Therefore, the redesign overcomes the restriction on high-voltage applications due to high-voltage stress on H-bridge switches [21].

(3) Reduction in blocking voltage on switches, a diversity of switches, and heat sinks.

(4) Modified PWM technique uses trapezoidal reference and inverted sine carrier waveform for the inverter, which enhances the inverter performance by maximising output voltage and reducing voltage distortion [22].

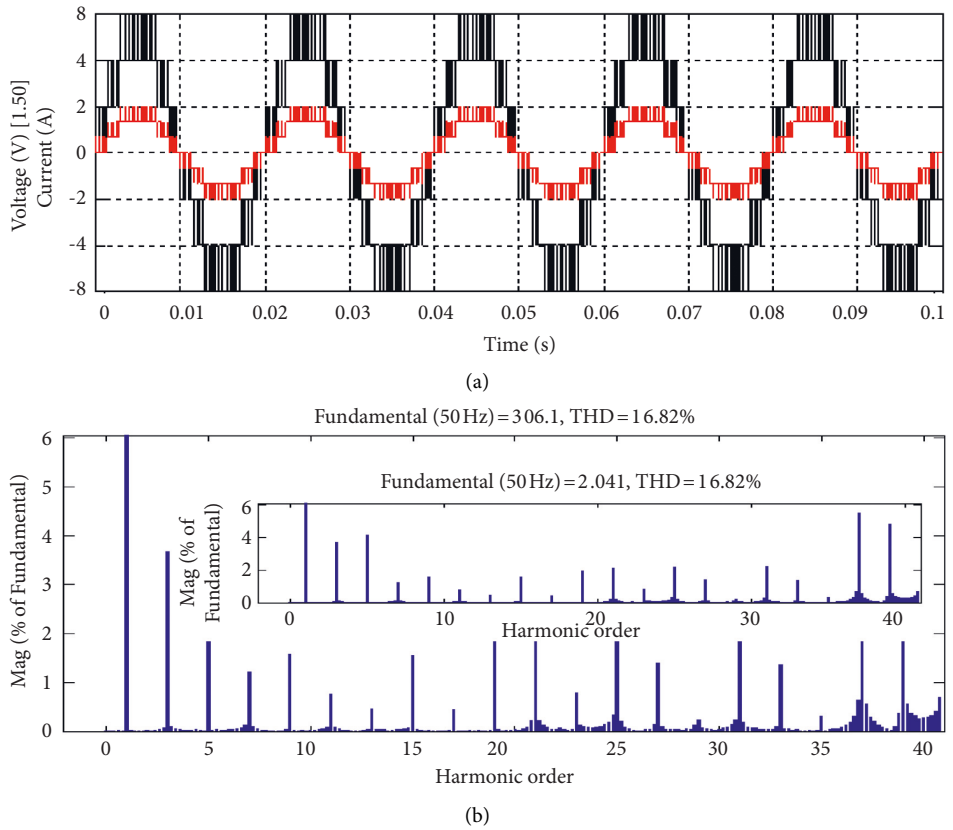


Figure 4: (a) Resultant 7-level voltage along with the current for R (100 Ω) load (simulation). (b) Harmonic spectrum.

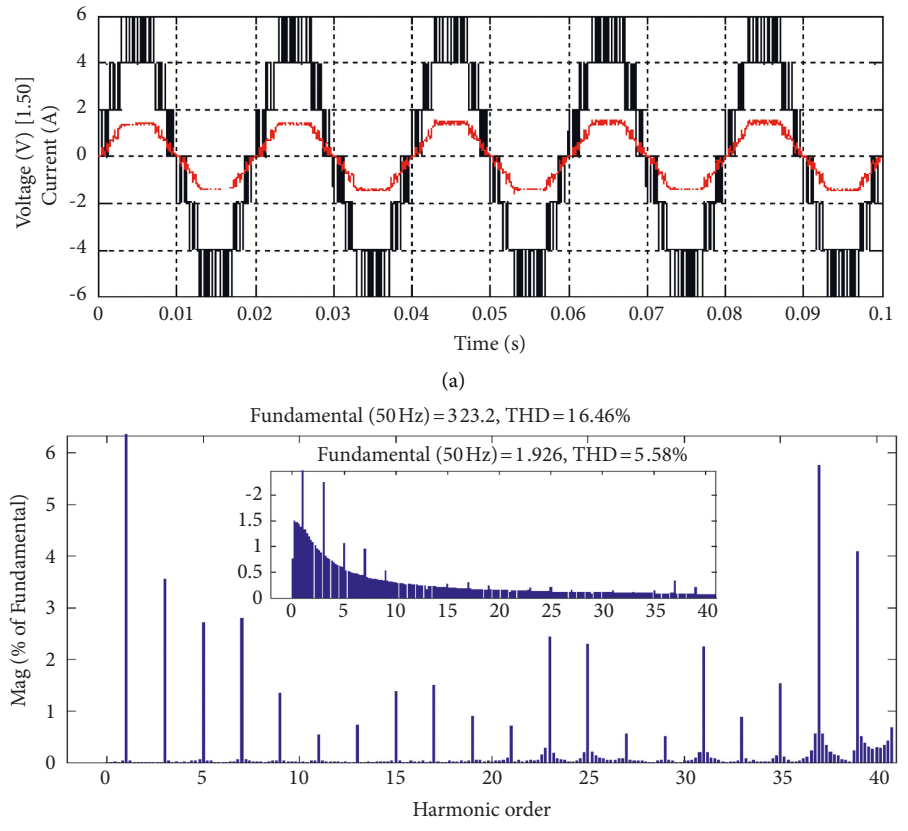


Figure 5: (a) Resultant 7-level voltage along with the current for a series RL (100 Ω and 240 mH) load (simulation). (b) Harmonic spectrum.

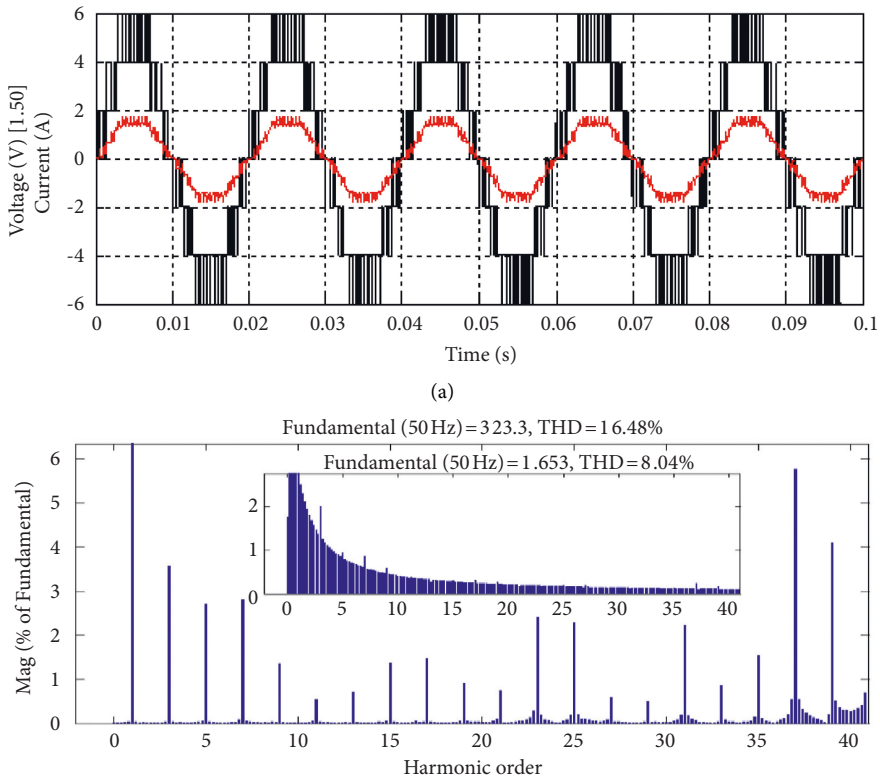


FIGURE 6: (a) Resultant 7-level voltage along with the current for a series RL (100 Ω and 400 mH) load (simulation). (b) Harmonic spectrum.

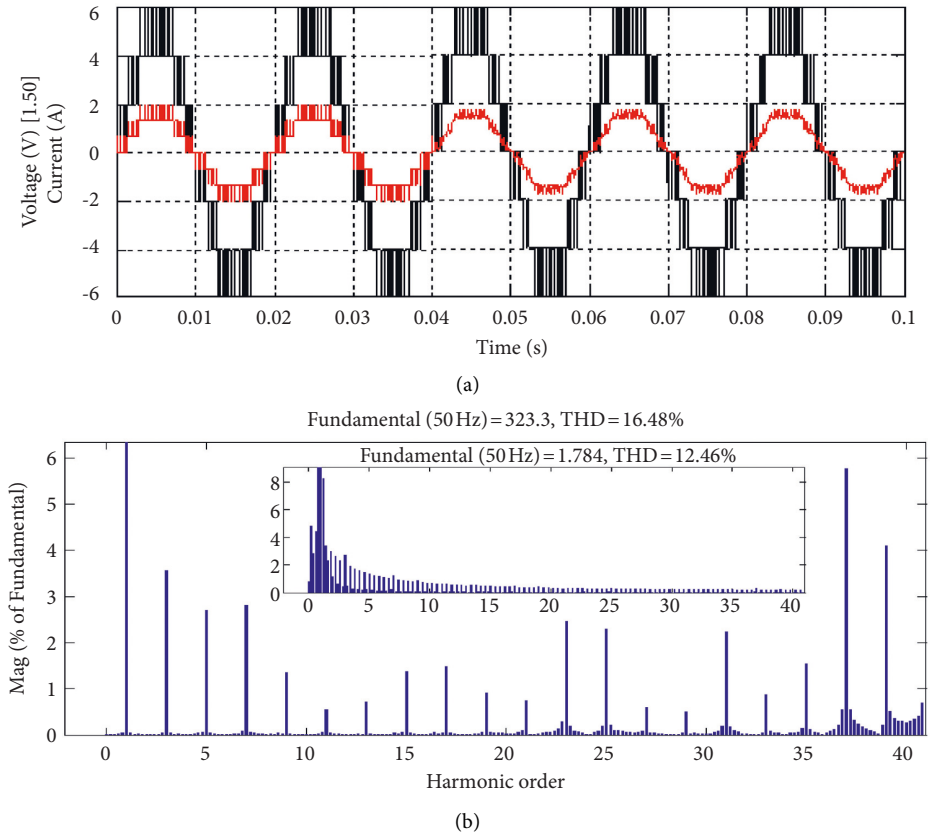


FIGURE 7: (a) Resultant 7-level voltage along with the current for sudden step change $R = 100\ \Omega$ to ($R = 100\ \Omega$, $L = 400$ mH) load (simulation results). (b) Harmonic spectrum.

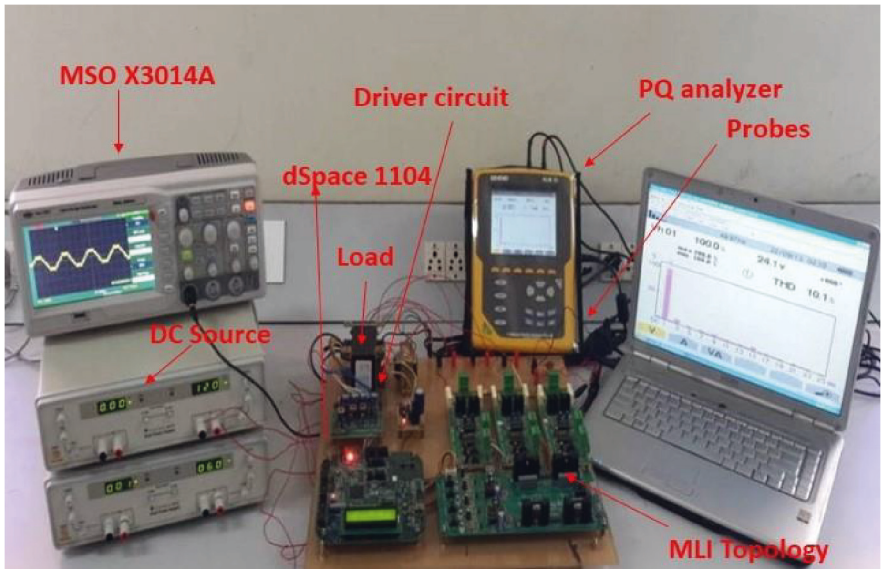
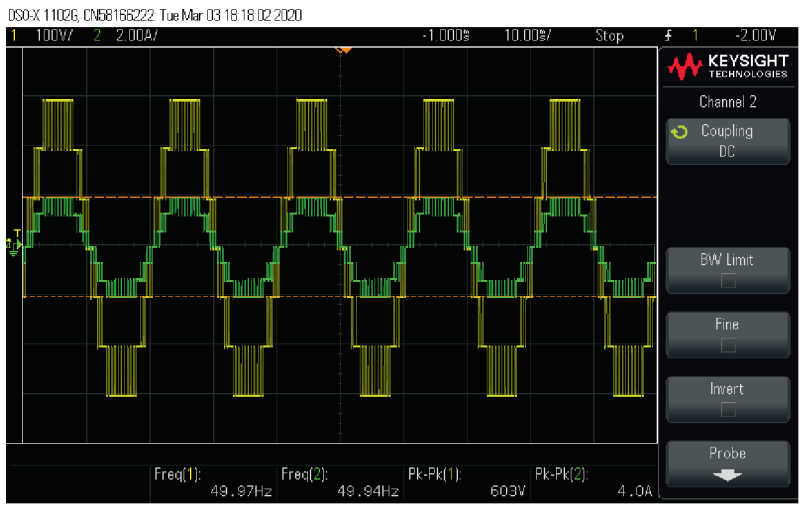
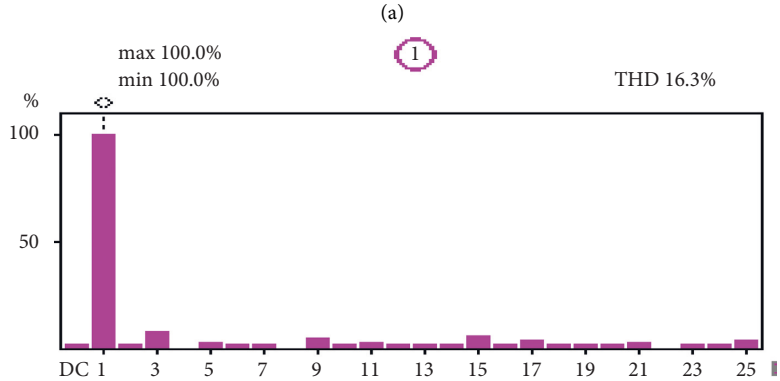


Figure 8: Experimental arrangement of proposed seven-level inverter.



(a)



(b)

Figure 9: (a) Resultant 7-level voltage along with the current for R (100 Ω) load (experiments). (b) Harmonic spectrum.

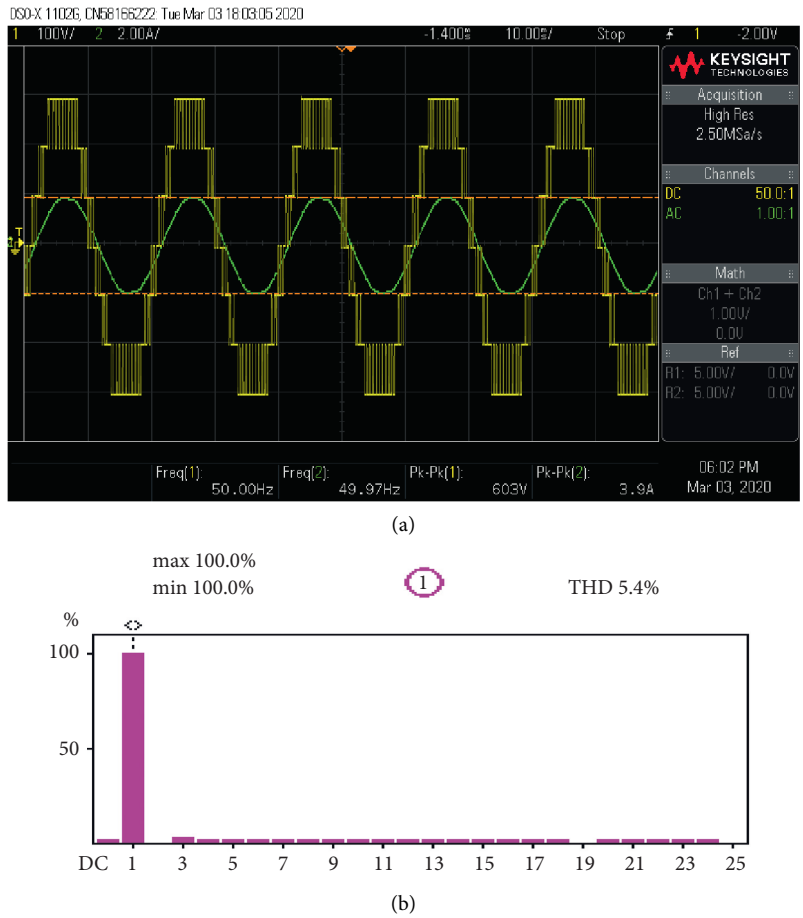


FIGURE 10: (a) Resultant 7-level voltage along with the current for a series RL-load (100 Ω and 240 mH) (experiments). (b) Current harmonic spectrum.

The following is the structure of the article: the operation of the proposed configuration and PWM technique is described in Section 2. Sections 3 and 4 discuss the comparative study and results. Conclusions are finally drawn in Section 5.

2. 7-Level Inverter Configuration and PWM Technique

2.1. Proposed Configuration of MLI. Figure 1 displays the proposed structure of a 7-level inverter with a new device arrangement. It is used to extract the seven-level output by choosing the suitable switches and sources. The configuration consists of 'two' dc sources with distinct voltage scales that have a two-fold geometric progression (V_{DC} and $2V_{DC}$), then the output voltage levels $0V_{DC}$, $\pm V_{DC}$, $\pm 2V_{DC}$, and $\pm 3V_{DC}$ can be achieved by choosing the suitable path from switches and dc sources. It consists of six semiconductor switches (Sa1 to Sa4, Sb1, and Sb2) like IGBT and two unequal dc sources of magnitude V_{DC} and $2V_{DC}$. With a proper driving pattern for six switches, it is possible to obtain voltage levels from -3 V_{DC} to 3 V_{DC}.

However, the extension of further high levels is quite complex. To avoid a short circuit, the suggested configuration switches (Sa1, Sa2), (Sa3, Sa4), (Sa1, Sb1), and (Sa3, Sb2) should never be switched on at the same period [23].

The current path for each output state and cyclic switching sequence is depicted in Figure 2(a)–2(h). Sa1, as well as Sa3, were switched ON in accordance with the operating modes for maintaining zero level. When Sa1 and Sa4 are turned ON, the output voltage becomes $+V_{DC}$, and then Sa2 and Sb2 are switched ON to produce $+2V_{DC}$ as an output voltage. Sa1 and Sb2 are turned ON to make output voltage as $+3V_{DC}$, then V_{out} becomes $-V_{DC}$ by turning ON Sa2 and Sa3. To synthesize $-2V_{DC}$ as the output voltage, Sa4 and Sb1 are turned ON. Sa3 and Sb1 are turned ON to make an output voltage $-3V_{DC}$. Table.1 shows voltage stress on each switch.

2.2. Proposed PWM Technique. The control strategy uses trapezoidal wave as a reference instead of sine wave and inverted sine waves as a carrier instead of triangular wave. The trapezoidal wave is obtained from triangular wave by limiting its magnitude, which is peak of the triangular wave. Interaction of trapezoidal reference and inverted sine carrier provide wider pulse area compared to conventional sinusoidal PWM scheme, which enhance the fundamental components. The operation of minimum switch multilevel

Figure 11: (a) Resultant 7-level voltage along with the current for a series RL-load (100 Ω and 400 mH) (experiments). (b) Current harmonic spectrum.

inverter is achieved by proper switching using carrier-based PWM technique named PD-PWM, which is depicted in Figure 3. In this case, a trapezoidal reference wave Tref and six inverted sine carrier C inv (1, 2, 3, ... , 6) are used. The half of the carrier are set above the zero reference C inv TOP (1, 2, 3, . . . , C inv/2) and remain set below the zero reference C inv BOT (1, 2, 3, . . ., C inv/2) with same frequency, phase, and amplitude are disposed. Each C inv* are compared with reference Tref, which produces command signals (Cs1, Cs2,. . .Cs3. . .). The switching signals are generated by a proper logical combination of command signals.

3. Comparative Study

Many reduced switch MLI topologies have been developed in recent past years. To prove the effectiveness of the proposed topology, several parameter (number of sources, switches, driver circuits, capacitors, and diodes) comparisons have been made between the proposed MLI topology and the recently developed topologies which are tabulated in Table 2. Table 2 shows the comparison of different parameters. From Table 1, it is evident that the proposed topology has the best features in the number of power switches, driver circuits, source capacitors, and diode. Based on the aforementioned merits, the proposed MLI requires the least cost and installation space requirement as compared to other MLI topologies.

4. Results and Discussions

4.1. Simulation Results. The Simulink-Power system block set has been used to simulate the desired asymmetrical multilevel inverter. Seven-level inverters were simulated for the modulation index value of 1 with various loads and dynamic shifts in the loads. VDC = 100V, R load value of 100 Ω, R-L load values of ($R = 100\,\Omega$, $L = 240$ mH), and ($R = 100\,\Omega$, $L = 400$ mH) are utilized. The carrier switching frequency fcarrier = 2 kHz.

Figures 4(a) and 4(b) exhibit the resultant waveform of voltage and current for the desired 7L inverter, as well as an FFT chart for the standard resistive load. The seven-level output waveform has voltage magnitudes of 0, ±100V, ±200V, and ±300V. The output voltage THD is 16.82%, and the fundamental peak voltage is 216.4 V. For the R-L load condition ($R = 100\,\Omega$, $L = 240$ mH), Figures 5(a) and 5(b) display the load voltage and currents, and also the output current FFT plot. The resultant current has a total harmonic distortion (THD) of 5.58%, as found by a Fast Fourier Transform (FFT) analysis. Furthermore, the testing has been performed using a separate set of R-L load ($R = 100$ ohms,

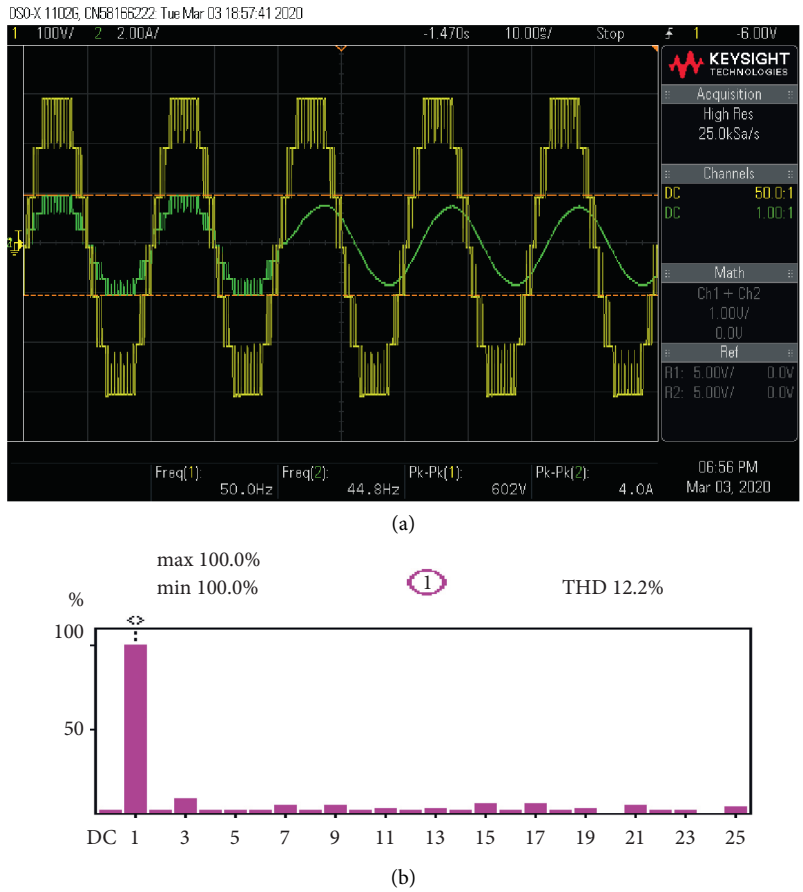


FIGURE 12: (a) Resultant 7-level voltage along with the current for sudden step change $R = 100\,\Omega$ to ($R = 100\,\Omega$, $L = 400$ mH) load (experiments). (b) Current harmonic spectrum.

$L = 400$ mH) with almost the same amplitude (100 Volts) of dc source for the same inverter configuration. Figures 6(a) and 6(b) show the resulting voltage and current for this load state, and also the resultant current FFT plot. The load current has a THD of 8.04 percent, as revealed by an FFT analysis. The developed inverter configuration has been effectively investigated for the rapid phase.

Transition loads [24]: the load voltage and current for rapid load shifts between $R = 100$ ohms to ($R = 100$ ohms, $L = 400$ mH) at $t = 0.04$ sec, as well as the current FFT plot, are displayed in Figures 7(a) and 7(b). The load voltage appears to remain steady even after a rapid transformation in load. Furthermore, the current in the load is rehabilitated from high to low value. The current harmonic distortion is found to be 12.46% using the FFT analysis.

4.2. Experimental Validation. In this study, a prototype of a seven-level inverter was examined under various loading conditions as well as dynamic variations in load values by setting the modulation index to 1. The MLI configuration consists of two DC sources (V1 = 100 V, V2 = 200 V) and six IGBT switches which produce 7-level output with the maximum value of 300 V. The other parameters are considered as follows: FGA25N120 IGBT switch, TLP350 driver circuit, R load value is 100 Ω, R-L load value of ($R = 100\,\Omega$, $L = 240$ mH), ($R = 100\,\Omega$, $L = 400$ mH), and the triggering signal for the IGBT switches is produced by the real-time controller DSpace 1104 in real time. The carrier switching frequency fcarrier = 2 kHz. Figure 8 depicts an experimental arrangement of the proposed 7L inverter. Figures 9(a) and 9(b) illustrate the resultant voltage and current waveforms for the proposed 7L inverter, as well as the FFT plot for the R load. The output waveform has a magnitude of 0, ±100V, ±200V, and ±300V. The output voltage THD is 16.30%, and the fundamental peak voltage of 213.4 V. For the R-L load ($R = 100$ ohm and $L = 240$ mH), Figures 10(a) and 10(b) show the 7-level voltage pattern and current pattern, as well as the current FFT plot. It can be seen that according to an FFT measurement of resultant current, the percentage of THD is 5.48%. The 7-level inverter arrangement were further investigate with R-L load ($R = 100$, $L = 400$ mH) and 100 V dc sources. Figures 11(a) and 11(b) exhibit the resultant voltage and current, as well as the current FFT plot. The percentage of THD in the resultant current is 8.04 percent, according to an FFT measurement. The effectiveness of the designed inverter structure has been validated for rapid phase-changing loading. The resultant voltage and current for rapid load transitions between $R = 100$ ohms and ($R = 100$ ohms, $L = 400$ mH) at $t = 0.04$ sec, as well as the current FFT chart,

are shown in Figures 12(a) and 12(b), respectively. It can be witnessed that after a quick shift in load, the resultant voltage appears to be stable. Moreover, the resultant current is reduced from a high to a low level. The percentage THD of resultant current is reported to be 12.26 using the FFT.

The aforementioned performance findings reveal that the presented topology is capable of handling a wide range of loads and is also suited for dynamic load changes.

5. Conclusion

In the work, a new multilevel inverter configuration is established using six switches. The suggested topology is a synthesized 7-level output waveform with two uneven dc inputs using trapezoidal reference and inverted sin-carrier-based PD-PWM method. The recommended multilevel inverter performance is confirmed with a variety of loading conditions. Furthermore, the proposed architecture uses merely six switches and eliminates the requirement for a distinct level generation and polarity generation arrangement. Furthermore, the proposed switching approach significantly improves the harmonic spectrum of the output waves under unequal dc links with dynamically changing load conditions. Moreover, the proposed switching method can apply to all types of multilevel inverters and it can be used in applications with higher and lower switching frequencies. The viability of recommended control technique is evaluated experimentally. The results validate the effectiveness of the recommended multilevel inverter configuration and control technique. As an outcome, we believe that the suggested multilevel inverter structure and control technique can provide improved dynamic performance while also lowering overall harmonic distortion and enhancing voltage profile.

Data Availability

The required data can be obtained from the corresponding author upon an email request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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