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ORIGINAL ARTICLE

A modular approach for testable conservative reversible multiplexer circuit for nano-electronic confine application

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Abstract

Quantum technology has an attractive application nowadays for its minimizing the energy dissipation, which is a prominent part of any system-level design. In this article, the significant module of a multiplexer, an extended to n:1 is framed with prominent application in the control unit of the processor. The proposed multiplexer modules are framed by the algorithm, which is extended perspective based. Further, quantum cost and gate count are less to ensure the efficient quantum computing framed. In addition, the QCA computing framework is an attempt to synthesize the optimal primitives in conservative reversible multiplexer in nano-electronic confine application. The developed lemmas is framed to prove the optimal parameters in the reversible circuit. Compared with existing state-of-art-works, the proposed modular multiplexer, the gate count, quantum cost and unit delay are optimal.

Keywords Quantum information science · Reversible multiplexer · Quantum-dot cellular automata · Quantum cost

Introduction

The complementary metal-oxide semiconductor (CMOS) circuit design in the nanometer scale range has primary limitations such as MOS transistor width (W), length (L) and short channel effect that cause degradation of the device performance [1]. To overcome the problems the research moved towards nanotechnology [2]. Recently quantum-dot cellular automata (QCA) general theorems promise the principle of low power, high device density, high switching speed and high operating frequency (THz) [3]. On the other hand, reversible logic has a popular field in the area of digital logic that can perform computing with almost zero power consumption [4]. Energy dissipation is a significant factor in digital logic circuits. According to Landauer, the single bit of data lost generates $KT\ln 2 = 0.017$ eV of heat energy, where K is Boltzmann's constant and $T = 300$ K is the absolute temperature [5]. Bennett proved that a zero power dissipation in a digital circuit is likely only if the circuit is designed for reversible logic gates [6]. In low power area, the reversible logic technique has an emerging area in Nano-electronics and quantum computing. In specific quantum, circuits are nanometric scale and high computation speed. Since they involve tiny size particle (known as qubits) and exist in the atomic scale level [7]. The advantage of reversible logic is that quantum computing is made of this method. Moreover, reversible logic is top-level emerging technologies, which process high-speed computing, low power, and nanometric scale [8]. Initially, the conservative based circuits are designed that emphasis on controlling the fault, which in turn increase the reliability of the circuits [9]. The second most important factor is a cost, which basic part of the quantum cost. If we focus on these two points, then the efficiency of the circuit will be enhanced. The novelty of this work is to design the circuits by combining all the above two factors.

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Among all digital integrated circuits, multiplexer circuits are the fundamental part, which is embedded in the module part of the control unit of the processor. More appropriately, the control unit of the processor consists of the multiplexer [9]. After reviewing the state-of-the-art work in this area, it can be conceived that a significant amount of research has been done in this domain besides few works targets the conservative approach, combined quantum logic circuit, and QCA framework [4, 7, 10–14]. The circuit by the authors in [7] such as 2:1 multiplexer was presented by MX-cqca gate using the conservative, but it is non-reversible. This multiplexer circuit has some constraints such as the modular approach cannot be developed for higher-order multiplexer, quantum circuit not realized because it is non-reversible. The main drawback of existing multiplexer in literature is it's not conservative reversible logic based, many researchers synthesize effort for optimizing the QCA parameters such as cell count, area and latency as [jcel1, jcel2]. The tendency to use such non-conservative QCA multiplexer is not fault tolerance and its high error rate too [15, 16]. After reviewing all the state-of-art-work, it can be analyzed that our proposed circuits have some speciality such as low-cost metric parameters (gate count, garbage outputs, and quantum cost) and conservative reversible logic based. In the more specific multiplexer, design approach extended for n-bit input using the developed algorithm. Further QCA layout implementation of proposed multiplexer has been constructed which appropriate to current Nano-electronics confine application.

Most of the above literature paper circuits discussed above not optimize, there is utilizing more quantum cost, not conservative approach and no quantum equivalent circuit of design. This means these designs are not cost-effective in terms of quantum cost and it is not conservative. However, the introduced design of multiplexer achieve optimal value of parameters and the performance is also studied by expanding the quantum equivalent circuit for the proposed design.

This work proposes low quantum cost-based conservative reversible multiplexer. The outlines of the workaround proposed circuits can be pointed out as follow.

- We design a conservative, reversible m:1 type multiplexer using existing R-CQCA gate. The presented quantum circuit shows the circuit is more cost-effective regarding quantum cost as compared to existing ones.
- We present the smaller QCA robust structure of multiplexer, and the simulation outcomes specify the correct functionality for the minimum clock cycle delay.
- We design a cost-effective, conservative reversible multiplexer based on proposed algorithm.
- We design a 2:1 multiplexer layout through QCADesigner tool, which provide the 0.25 s latency and 0.24 μm^2 area.
- We synthesize the multiplexer based on algorithm it expand to n:1 multiplexer also and it helpful for ALU, and control unit of processor design.

The rest of the paper is organized as follows: "Basic terminologies" section discusses the basic terminologies related to our work. "Proposed multiplexer based on R-CQCA gate" section discuss the proposed reversible gate R-CQCA. The utility of R-CQCA as a multiplexer is elaborated in "Existing conservative, reversible gates" section. Proposed gate cell layout is given in "Design of conservative reversible multiplexer gate in QCA" section. In "Table 4 presents the comparative analysis of multiplexer" section, the table presents the comparative analysis of multiplexer. Finally, a conclusion has been shown in section Conclusion.

Basic terminologies

This section, we have presented the basic terminology such as reversible logic, conservative, reversible logic and QCA that are related to this work. Basic terminologies have been reviewed in state-of-the-art work as per [17–20].

Definition 2.1 The reversible gate should have the equal number of inputs $I_v(A_0, A_1,\ldots A_n)$ and outputs $O_v(B_0, B_1,\ldots B_n)$ and the bijective mapping at the same time. Figure 1a drawn the reversible gate.

Definition 2.2 A conservative, reversible gate is a hamming weight of inputs and outputs is equal [8], which is shown in Fig. 1b. More appropriately, it can be drawn in Eq. (1).

$$A_1 \oplus A_2 \oplus \ldots A_n \overset{\text{bijective}}{\longleftrightarrow} B_1 \oplus B_2 \oplus \ldots B_n \tag{1}$$

Definition 2.3 The significant cost-metric parameter for reversible logic is quantum cost. Any reversible gate can be decomposed into 1×1 and 2×2 gates such as CNOT, V and V^+ gates (called quantum primitive gates). The CNOT gate is depicted in Fig. 2a and the quantum cost calculation for some basic structures are depicted in Fig. 2b–e. The cost is calculated by counting the total primitives gates [7]. The controlled V and V^+ gate are depicted in Fig. 2f. In the controlled V gate when the control input $A=1$, implies $Q=V(B)$, that V is synthesized by Eq. (2). When $A=0$, implies $Q=$B, where A and B are inputs and Q is the output. The V and V^+ gates have some basic properties that drawn in Eqs. (3) and (4).

$$V = \frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & -1 \end{pmatrix} \tag{2}$$

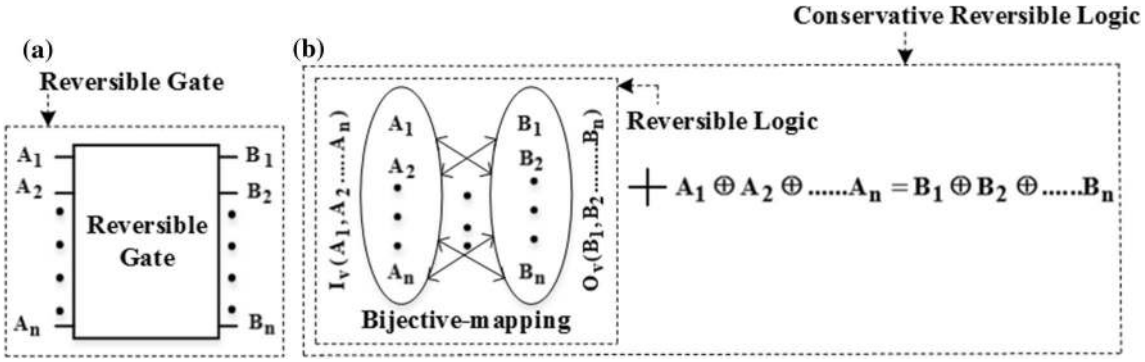
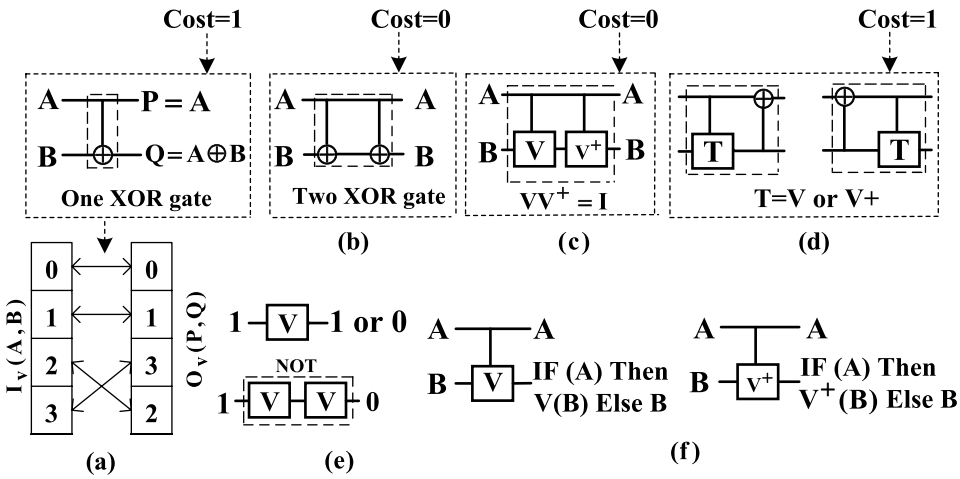


Fig. 1 An $n \times n$ architecture of reversible gate

Fig. 2 Basic of quantum cost



$$V \times V = V^{+} \times V^{+} = \text{NOT} \tag{3}$$

$$V^{+} \times V = V \times V^{+} = I \tag{4}$$

Definition 2.4 In QCA cell has a quantum dot, with a four number. The shape of quantum-dot is circular with a specified diameter of 10 nm, and each dot is situated within a neighbor radius of 20 nm. Whether two extra electrons are situated in existing two quantum dots, and the arrangement is always in a diagonal way. The formed QCA cell can be a definite polarization (Fig. 3a). The majority gate, inverter, fan-out concept, and clock are depicted in Fig. 3b–d, respectively. The binary value stored in the QCA cell can be defined by polarization. The polarization expression is drawn by Eq. (5).

$$P = \frac{(\sigma_{1} + \sigma_{3}) - (\sigma_{2} + \sigma_{4})}{\sigma_1 + \sigma_2 + \sigma_3 + \sigma_4} \tag{5}$$

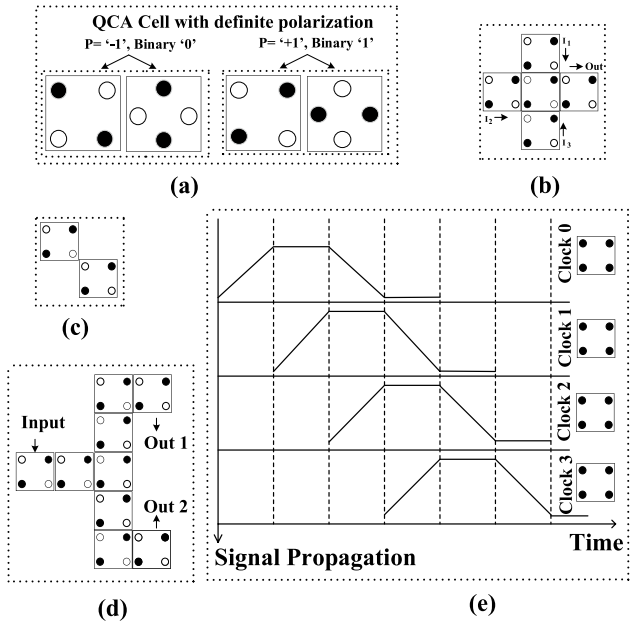


Fig. 3 QCA fundamentals **a** QCA cell, **b** majority gate, **c** smaller robust inverter, **d** fan out and **e** clocking

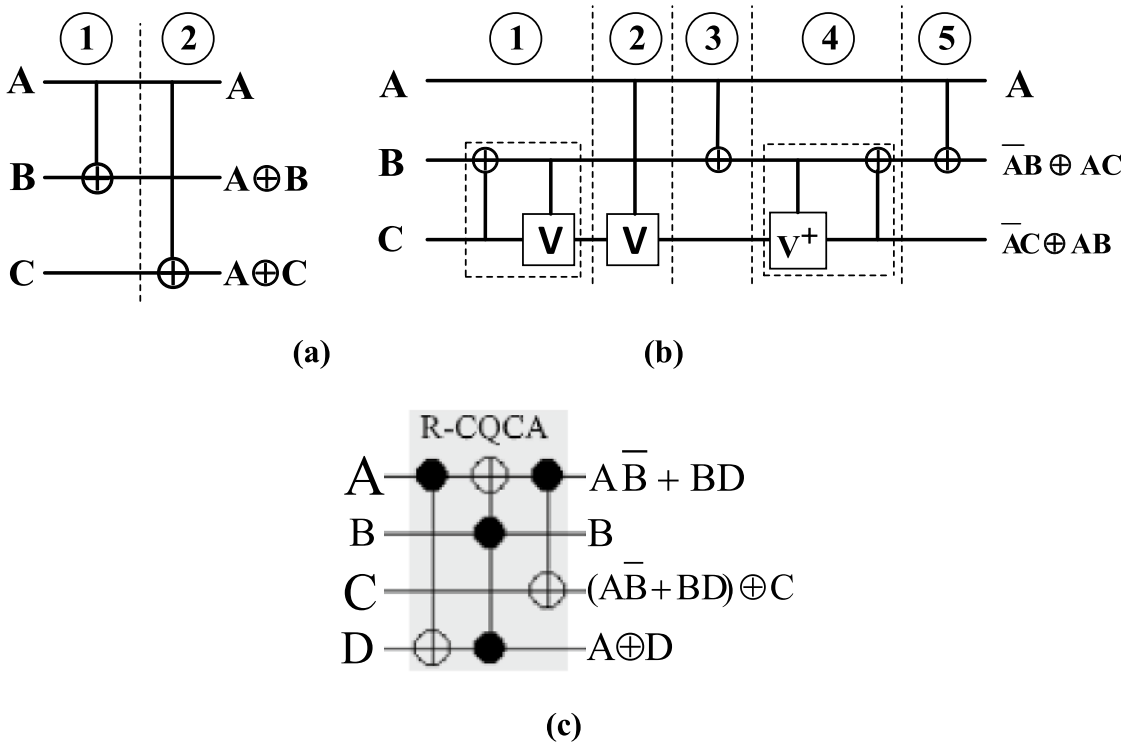


Fig. 4 Existing conservative, reversible gate quantum circuit **a** F2G, **b** FRG and **c** R-CQCA

Definition 2.5 QCA has four clock zones; the utility is to control the information flow. Four clock zones are categories by four phase (Switch, Hold, release and relax). Clock zone is shown in Fig. 3e.

Definition 2.6 The kink energy is the difference between the maximum and minimum energy. Whereas maximum energy exist when the two cells have opposite polarization and have the minimum energy when they have the same polarization. The kink energy is drawn by Eq. (6). Whereas the electrostatic energy of a circuit is formed by considering two cells (named cell a and cell b) with polarization (called P_a and P_b) side by side, is drawn by Eq. (7).

$$E_{\text{kink}} = E^{m,n}_{P_m \neq P_n} - E^{m,n}_{P_m = Pn} \tag{6}$$

$$E_{m,n} = \frac{1}{4\pi\varepsilon_0} \Sigma^4_{k=1} \Sigma^4_{l=1} \frac{q^m_k q^n_l}{|r^m_k - r^n_l|} \tag{7}$$

Proposed multiplexer based on R-CQCA gate

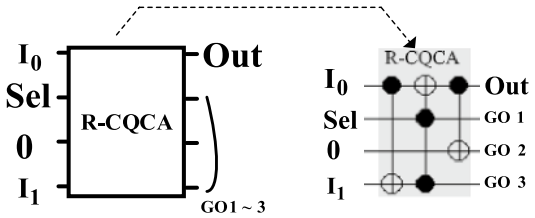
To test the circuit, the conservative logic claims to have cost-efficient application in reversible logic circuits. In fact, the conservative feature is the prominent part of testing reversible gates [21]. Hence, to achieve a low error rate and testing feature, the conservative, reversible technique would truly be remarked as the useful feature for construction digital logic integrated circuits. The conservative, reversible logic useful in QCA technique since it addresses the cost-efficient concern, such as: reducing cell complexity, reducing delay, layout area, and power [14].

In this paper, a novel multiplexer, circuit have been constructed by existing reversible gate [21]. The R-CQCA gate is utilized for the multiplexer circuit. In "Modular approaches to design a multiplexer" section, multiplexer circuits are presented.

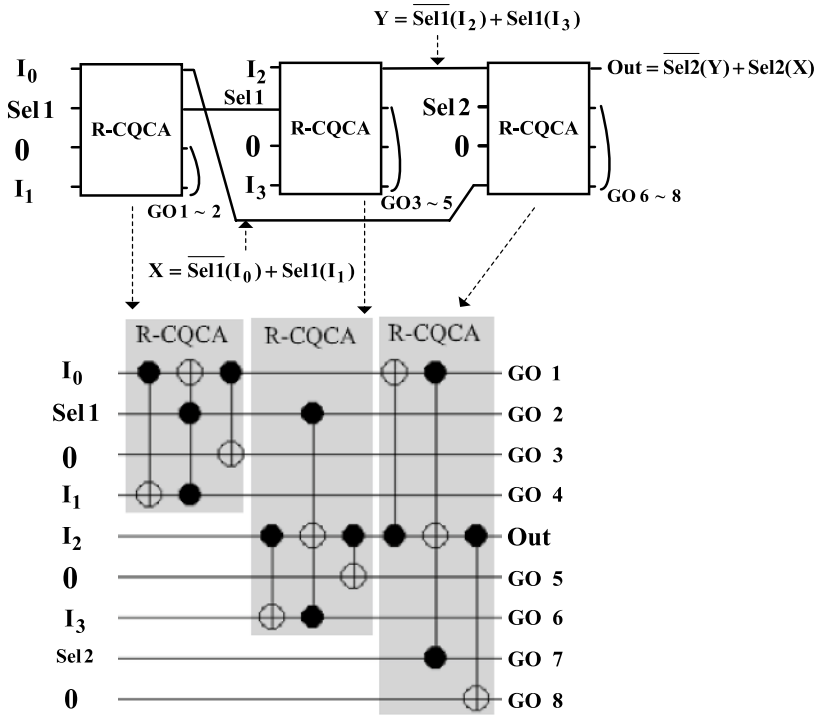
Existing conservative, reversible gates

The two popular existing conservative, reversible gate is F2G, FRG and R-CQCA. In F2G input vector is I_v the output vector O_v and they are set by $I_v(A, B, C)$ and $O_v = (A, A \oplus B, A \oplus C)$. In FRG input and output vector are set as $I_v(A, B, C)$ and $O_v = (A, \overline{A}B + AC, \overline{A}C + AB)$. The other conservative, reversible gate is R-CQCA; it is popular due to its low value of quantum cost [21]. The quantum cost of F2G, FRG, and R-CQCA are 2, 5 and 6, respectively. Conservative, reversible R-CQCA gate is used for synthesized the multiplexer in this work. The quantum equivalent circuit of F2G, FRG, and R-CQCA is depicted in Fig. 4a–c respectively.

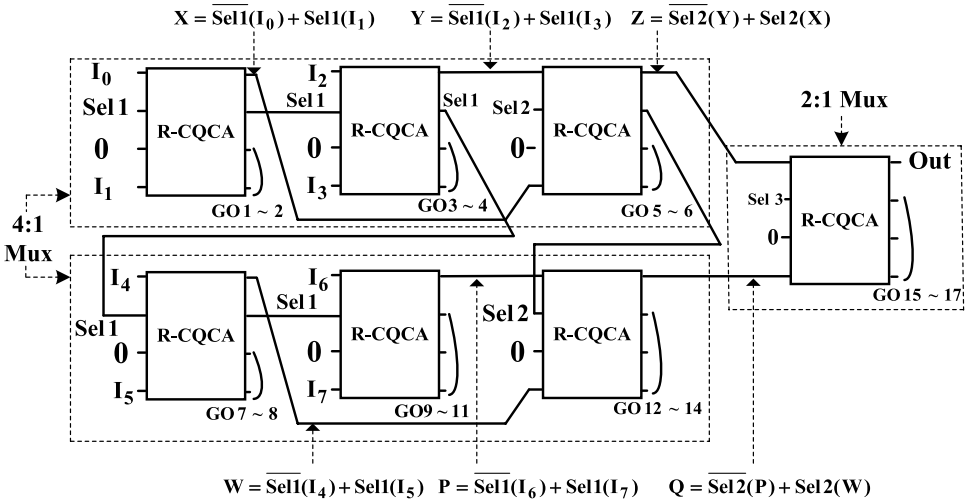
Fig. 5 Reversible multiplexer



(a) Schematic diagram and equivalent quantum presentation of 2:1 mux using R-CQCA



(b) The schematic and quantum equivalent of 4:1 mux using R-CQCA



(c) Schematic diagram of 8:1 mux using R-CQCA

Modular approaches to design a multiplexer

In the computational field, the multiplexer is used to select the particular data [9]. The 2:1 Mux design is constructed using 1 × R-CQCA, and its unit delay is 1. The schematic and quantum circuit is well furnished by the 2:1 mux as depicted in Fig. 5a. In the 2:1 mux consist of one select line (Sel), two input information (I_0, I_1) and one required output (Out). The output is synthesized by Out = $\overline{\text{Sel}}(I_0)$ + Sel(I_1). When Sel = 0 then output data line connect to I_0 and for Sel = 1 output connect to I_1.

In a modular approach, the generic unit of 2:1 mux can be employed for 4:1 Mux, a simplified three unit of 2:1 mux version is employed for the design of 4:1 mux. The corresponding schematic and quantum presentation of 4:1 mux are shown in Fig. 5b. However, based on the circuit configuration used for binary data, select inputs by select line inputs is drawn in Table 1.

Using the two units of 4:1 Mux and one unit of 2:1 mux we can accomplish the 8:1 mux, whose construction is shown in Fig. 5c. A straightforward approach for multiplexer design is adopted in m:1 mux design. Thus, the design of m:1 mux has at least two unit of $\frac{m}{2}$: 1 mux in addition one unit of 2:1 mux. A complete construction for the execution of m:1 multiplexer is depicted in Fig. 6. Thus, according to the modular approach of multiplexer, lower bound reversible parametric analysis of the number of date inputs m is given by Lemma 1. A construction algorithm of m:1 multiplexer is drawn in Algorithm 1. According to 8:1 multiplexer circuit, their computation process of data inputs is drawn in Table 2.

Lemma 1 *An m:1 multiplexer cascading link by the R-CQCA can be synthesized by (m − 1) be the minimum gate count (GC) and constant input (CI), 2(m − 1) + $\log_2 m$ be the garbage output (GO) and 4(m − 1) quantum cost (QC)*

Proof The construction of m:1 multiplexer consists of $\left(\frac{m}{2}\right)$: 1 multiplexer and single 2:1 multiplexer. Hence the minimum GC and CI for 2:1, 4:1, 8:1 and m:1 type of multiplexer is

$$(\text{GC})_{2:1\text{mux}} = (\text{CI})_{2:1\text{mux}} = 1 = 2 - 1 \tag{8}$$

Hence above equation hold for $m = 2$.

$$(\text{GC})_{4:1\text{mux}} = (\text{CI})_{2:1\text{mux}} = 3 = 4 - 1 \tag{9}$$

$$(\text{GC})_{8:1\text{mux}} = (\text{CI})_{2:1\text{mux}} = 7 = 8 - 1 \tag{10}$$

Assume that the Eq. (8), (9) and (10) supports for $m = n$. Therefore, an m:1 multiplexer can be synthesized by $(m - 1)$ gate count.

The GO rise by a 2:1, 4:1, 8:1 and m:1 type of multiplexer as drawn by Eqs. (11), (12) and (13)

$$(\text{GO})_{2:1\text{mux}} = 3 = 2(2 - 1) + \log_2 2 \tag{11}$$

Hence above equation hold for $m = 2$.

$$(\text{GO})_{4:1\text{mux}} = 8 = 2(4 - 1) + \log_2 4 \tag{12}$$

$$(\text{GO})_{8:1\text{mux}} = 17 = 2(8 - 1) + \log_2 8 \tag{13}$$

As a mathematical induction, the least $2(m - 1) + \log_2 m$ garbage output for m:1 type of multiplexer.

A 2:1, 4:1, 8:1 type of multiplexer requires 4, 12 and 28 quantum cost. The quantum cost of m:1 multiplexer synthesize by induction as below Eqs. (14), (15) and (16)

$$(\text{QC})_{2:1\text{mux}} = 4 = (2 - 1) \times 4 \tag{14}$$

Hence above equation hold for $m = 2$.

$$(\text{QC})_{4:1\text{mux}} = 12 = (4 - 1) \times 4 \tag{15}$$

$$(\text{QC})_{8:1\text{mux}} = 28 = (8 - 1) \times 4 \tag{16}$$

Therefor a m:1 multiplexer hold the $4(m - 1)$ relationship for QC.

Table 1 4:1 Multiplexer data output

Select line inputs		Intermediate outputs		Data output
Sel_1	Sel_2	X	Y	Out
0	0	I_0	I_2	I_2
0	1	I_0	I_2	I_0
1	0	I_1	I_3	I_3
1	1	I_1	I_3	I_1

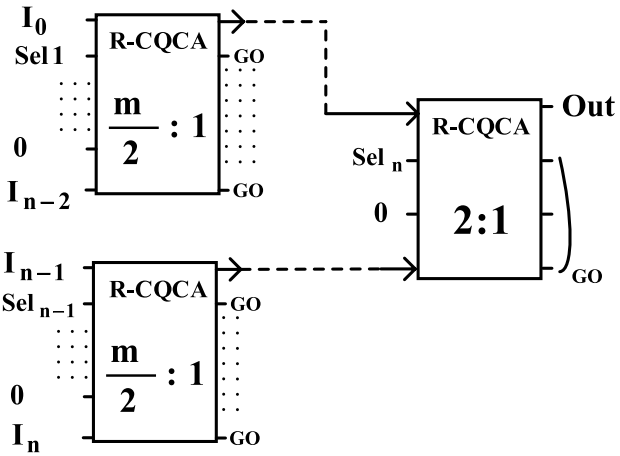


Fig. 6 Modular design of m:1 multiplexer

Algorithm 1. Modular-Design-Algorithm (m:1 multiplexer)

Input, Output: Input data set I=(I_0, I_1, I_2,……,I_{n-1}), Select line Sel=(S_0, S_1,……,S_{n-1}) and generate one output (Out) will store the outcomes.

1. Begin

Stage-1: Circuit takes 2 unit of $\left(\frac{m}{2}\right)$: 1 type multiplexer and 1 unit of 2:1 type multiplexer

2. Begin procedure (m:1 multiplexer)

3. For i=0 to m-1 **do**

4. If i=0 **then**

Utilize first $\left(\frac{m}{2}\right)$: 1 type multiplexer as an initial output of a $\left(\frac{m}{2}\right)$: 1 multiplexer

5. End if

6. If i=1 **then**

Utilize Second $\left(\frac{m}{2}\right)$: 1 type multiplexer as output of a $\left(\frac{m}{2}\right)$: 1 multiplexer

7. End if

8. If i=2 **then**

Choose the inputs of the 1 unit of 2:1 multiplexer from the cascade link from the 2 unit of $\left(\frac{m}{2}\right)$: 1 multiplexer

9. End if

10. Else

Go to line 2

11. End for

12. Return Select one desired output from 2:1 multiplexer, remaining output are consider as garbage output.

13. End

Table 2 8:1 Multiplexer data output

Select line inputs			Intermediate outputs						Data output
Sel_1	Sel_2	Sel_3	*X*	*Y*	*Z*	*W*	*P*	*Q*	Out
0	0	0	I_0	I_2	*Y*	I_4	I_6	*P*	I_2
0	0	1	I_0	I_2	*Y*	I_4	I_6	*P*	I_6
0	1	0	I_0	I_2	*X*	I_4	I_6	*W*	I_0
0	1	1	I_0	I_2	*X*	I_4	I_6	*W*	I_4
1	0	0	I_1	I_3	*Y*	I_5	I_7	*P*	I_3
1	0	1	I_1	I_3	*Y*	I_5	I_7	*P*	I_7
1	1	0	I_1	I_3	*X*	I_5	I_7	*W*	I_1
1	1	1	I_1	I_3	*X*	I_5	I_7	*W*	I_5

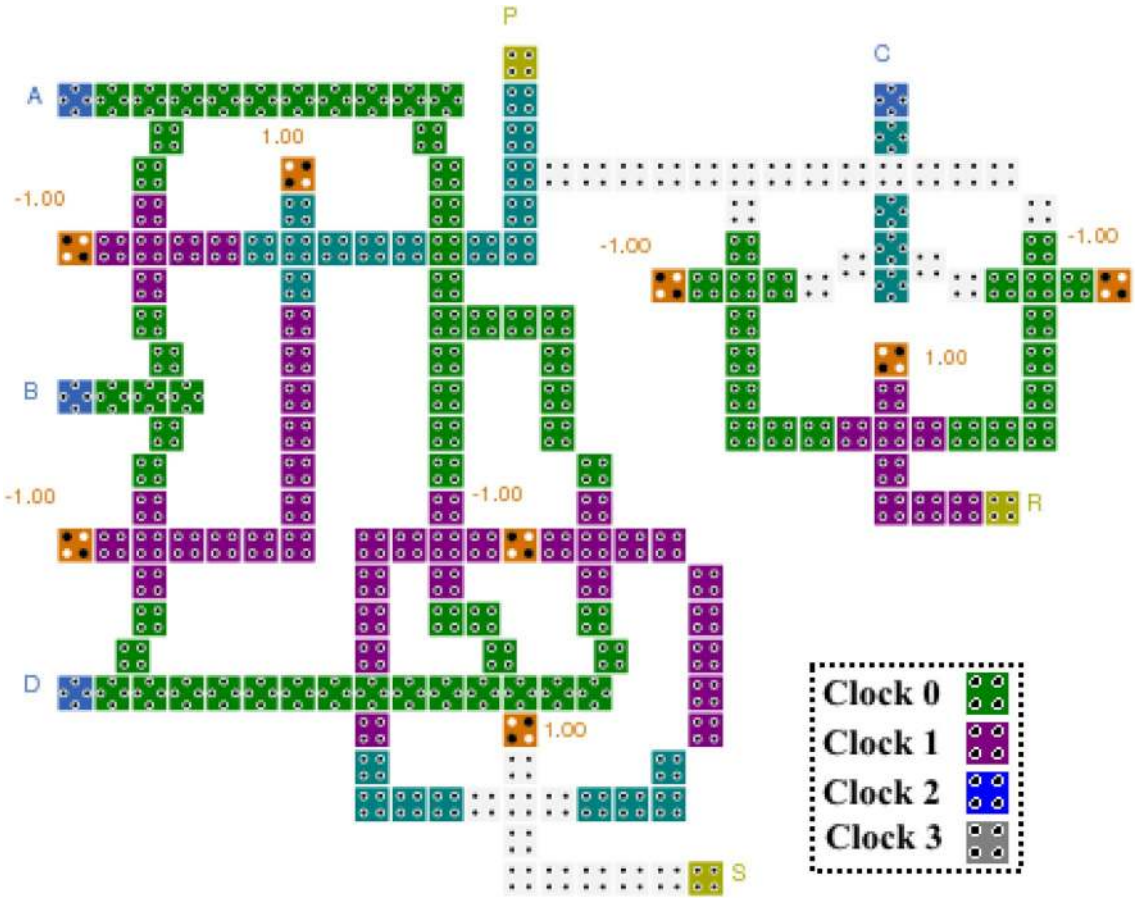


Fig. 7 Cell layout of R-CQCA

Design of conservative reversible multiplexer gate in QCA

To judge the efficiency of the proposed R-CQCA, the cell layout in QCA Designer is considered. The cell layout of R-CQCA is depicted in Fig. 7. The Bistable-approximation engine is used for outcomes verification. In Fig. 8, it visualizes the results. It depicts that the results are strong polarization value of different input combinations. The beginning output P is acquired after 0.25 clock cycle delay. The third (R) and fourth (S) outputs are acquired after 1 clock cycle delay. Using cell layout and simulation, outcomes 3 important features (complexity, speed, and area) are extracted from this proposed layout, which is shown in Lemma 2.

Lemma 2 *The maximum latency required to synthesize a 2:1 multiplexer using simulation outcomes is 0.5.*

Proof In the 2:1 multiplexer, cell layout is depicted in Fig. 7. The outcomes are verified under the bistable approximation model with default parameters in QCA Designer. The simulation outcomes elucidate that when select input $B=(0, 0)$ the outcomes $P=(0, 1)$, appear after 0.5 latency i.e. input $A=(0,1)$ is selected and sent to output node P. When to take the inputs $B=(1, 1)$ the outcomes as $P=(0, 1)$ i.e. input $D=(0,1)$ is routed to output node P. Therefore, it is observe that ancilla inputs play an important role to get the output of multiplexer. Maximum latency of 2:1 multiplexer is 0.5, as depicted in simulation result in Fig. 8. Hence, maximum 0.5 latency is utilized for projects in 2:1 multiplexer.

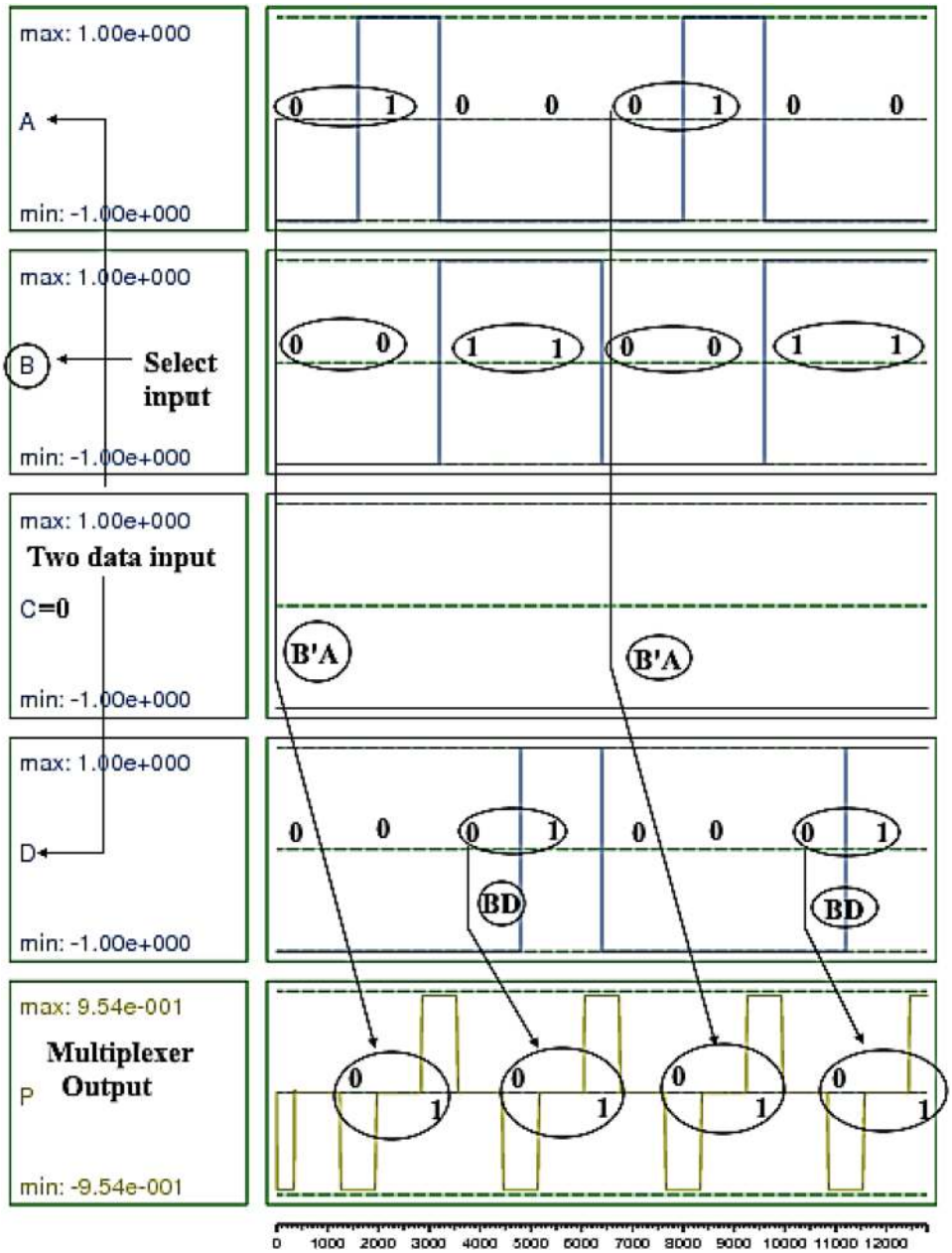


Fig. 8 Simulation result of 2:1 multiplexer using R-CQCA

Table 3 Performance metrics analysis of proposed multiplexer

Multiplexer	Metrics
2:1	1 QC (R-CQCA) = 6
	1 GO (R-CQCA) = 4
	1 CI (R-CQCA) = 1
	1 UD (R-CQCA) = 1
4:1	3 QC (R-CQCA) = 3 × 6 = 18
	3 GO (R-CQCA) = 2 + 3 + 3 = 8
	3 CI (R-CQCA) = 1 + 1 + 1 = 3
	3 UD (R-CQCA) = 3
8:1	2 QC (4:1 mux) + 1 QC (R-CQCA) = 2 × 18 + 6 = 42
	2 GO (4:1 mux) + 1 GO (R-CQCA) = (6 + 8) + 3 = 17
	2 CI (4:1 mux) + 1 CI (R-CQCA) = 2 × 3 + 1 = 7
	2 UD (R-CQCA) = 2 × 3 + 1 = 7

QC quantum cost, *GO* garbage output, *CI* ancilla input, *UD* unit delay

Table 4 presents the comparative analysis of multiplexer

Table 3 shows the proposed reversible primitives of multiplexer circuits. Table 4 presents a comprehensive comparison between the existing and proposed multiplexer circuit regarding reversible metrics such as gate count, garbage outputs, quantum cost and conservative feature. Recent existing work in [4, 7, 12, 13] have some reversible metrics, the proposed modular approach based multiplexer has the capability of optimizing all reversible metrics. The comparative analysis table depicted in Table 5.

Conclusion

This work targets the basic factor such as cost-efficient solutions for nano-electronics based confine application, which has been successfully presented in this article. The cost-efficient conservative reversible multiplexer has been discussed and introduced successfully. The synthesizer circuits discussed in this paper is new and has achieved the target results. In fact, we have explored our proposed reversible gate R-CQCA in the dissimilar type of circuits such as multiplexer. First, the modular approach for multiplexer circuits, it presents better parameters as compared to existing ones. We have proven the reliability of multiplexer by lemmas. The inevitable optimal parameters m:1 mux is $2(m-1)+\log_2 m$ garbage outputs and $4(m-1)$ quantum cost. The entire circuits work around R-CQCA and its aim is to optimize the quantum cost. The R-CQCA has only 6 quantum cost.

Table 4 Comparative analysis results of multiplexer design in QCA

Design	Reversible	Cell count	Majority gate	Inverter	Latency	Area (μm^2)
Existing [3]	No	246	11	4	1.25	0.25
Existing [10]	No	124	9	9	2	0.25
Existing [11]	No	154	3	4	1	0.15
Existing [14]	No	23	3	1	1	0.02
New	Yes	177	9	1	0.25	0.24

Table 5 Comparison between the proposed and existing multiplexer

Type		[4]	[7]	[12]	[13]	Proposed
2:1	GC	1	1	1	1	1
	GO	2	2	1	2	3
	QC	4	5	4	4	6
	Conservative	No	Yes	No	No	Yes
	Equivalent quantum circuit	No	No	No	No	Yes
4:1	GC	3	3	3	6	3
	GO	5	5	5	10	8
	QC	12	15	12	28	12
	Conservative	No	Yes	No	No	Yes
	Equivalent quantum circuit	No	No	No	No	Yes
m:1	GC	$(m-1)$	$3n$	–	–	$(m-1)$
	GO	$(m-1)+\log_2 m$	$4m+1$	–	–	$2(m-1)+\log_2 m$
	QC	$4(m-1)$	$15m$	–	–	$4(m-1)$
	Conservative	No	Yes	–	–	Yes

'–' Not mentioned

Proposed multiplexer is analyzed on QCADesigner simulator. In further analysis has been included to determine the impact of R-CQCA in QCA technology. It is found that 0.25 latency, 0.24 μm^2 area, 177 cell complexity. The proposed dissimilar type of circuit will facilitate the coverage of low reversible parameters, QCA logic computing, and classification of QCA parameters such as complexity (cell count), speed (latency) and area usages.

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