A Modular Multilevel Voltage-Boosting Marx Pulse-Waveform Generator for Electroporation Applications

Mohamed A. Elgenedy, *Member, IEEE*, Ahmed Massoud, *Senior Member, IEEE*, Shehab Ahmed, *Senior Member, IEEE*, Barry W. Williams, and Jim R. McDonald

Abstract –In order to overcome the limitations of the existing classical and solid-state Marx Pulse Generators, this paper proposes a new modular multilevel voltage-Boosting Marx Pulse Generator (BMPG). The proposed BMPG has hardware features that allow modularity, redundancy and scalability as well as operational features that alleviate the need of series connected switches and allows generation of a wide range of pulse waveforms. In the BMPG, a controllable low-voltage input boost converter supplies, via Directing/Blocking (D/B) diodes, two arms of a series modular multilevel converter Half-Bridge Sub-Modules (HB-SMs). At start up, all the arm's SM capacitors are resonantly charged in parallel from 0V, simultaneously via directing diodes, to a voltage in excess of the source voltage. After first pulse delivery, the energy of the SM capacitors decreases due to the generated pulse. Then, for continuous operation without fully discharging the SM capacitors or having a large voltage droop as in the available Marx generators, the SM-capacitors are continuously re-charged in parallel, to the desired boosted voltage level. Because all SMs are parallel connected, the boost converter duty ratio is controlled by a single voltage measurement at the output terminals of the boost converter. Due to the proposed SMs structure and the utilization of D/B diodes, each SM capacitor is effectively controlled individually without requiring a voltage sensor across each SM capacitor. Generation of the commonly used pulse waveforms in electroporation applications is possible, whilst assuring balanced capacitors, hence SM voltages. The proposed BMPG has several topological variations, such as utilizing a buck-boost converter at the input stage and replacing the HB-SM with full-bridge SMs. The proposed BMPG topology is assessed by simulation and scaled-down proof-of-concept experimentation to explore its viability for electroporation applications.

1

I. INTRODUCTION

There are two types of biological cell membrane electroporation, viz., lethal and the non-lethal [1]. Applications varying from medical, residential and industrial, benefit from the two electroporation types [2]-[4]. In both cases, the electric field E creates pores in the cell-membrane, as illustrated in Fig. 1. If these pores fail to reseal after removing the applied electric field, the cell does not survive. Drug insertion for medical treatment and biofouling prevention in factory water pipes are examples of non-lethal electroporation [1]-[5].

If the electric field level E increase across a biological cell membrane is beyond a certain critical value ($E > E_{cr}$) then lethal electroporation results, where the cell membrane is unable to reseal its pores and it dies [5]. Water disinfection, air pollution control, and food sterilization are examples of the lethal electroporation [6], where harmful microorganisms destroyed. A Pulse Generator (PG) is required to apply High-Voltage (HV) pulses across the treatment chamber. These HV pulses impose the required level of the electric field across the biological cell-membrane, as shown in Fig. 1. Recent research confirms the effectiveness of applying HV-pulses in the kilo-Volt range (1-100kV) with a pulse duration ranging from nanoseconds to milliseconds [7]. Both energy efficiency and electroporation criteria are met.
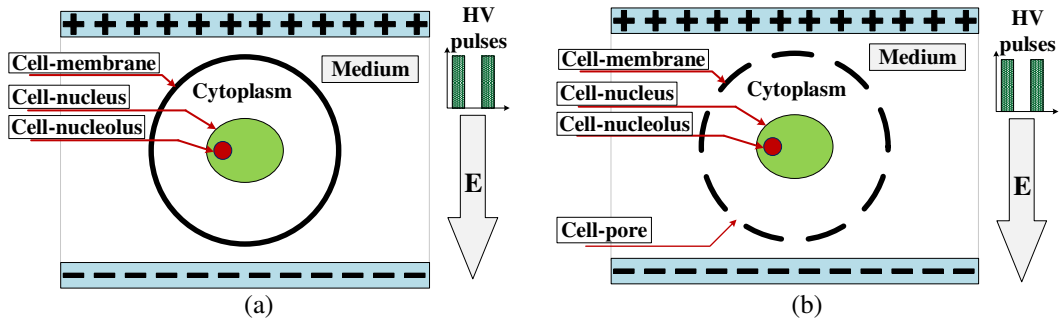

Fig. 1. Effect of electroporation on a biological cell membrane.
(a) At the beginning of electroporation. (b) After lethal electroporation.
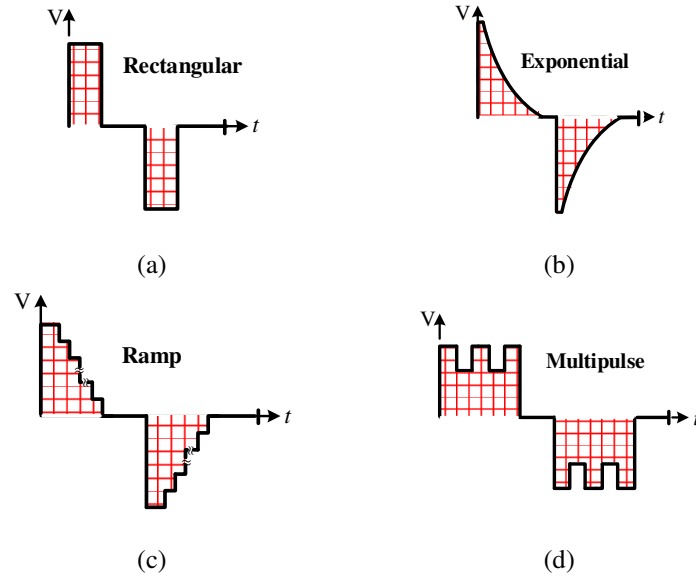
2

Fig. 2. Common pulse waveforms in PEF applications.
(a) Rectangular. (b) Exponential. (c) Ramp. (d) Multipulse.

Each application has specific HV pulse requirements, so a PG should be flexible and controllable to meet most applications requirements. Therefore, a generic pulse waveform generator should able to control the rise, plateau and tail times of the generated pulses in order to mimic a wide range of pulses [8].

As in [8]-[10], there are three main pulse waveforms; each is preferred but not limited to a specific application; these pulses can be generated from a single PG if it is able to generate a controllable multilevel waveform. The rectangular pulse waveform, shown in Fig. 2a, is the most common pulse waveform due to its effective pulse area, compared with the exponential pulse waveform, shown in Fig. 2b. Traditionally an exponential voltage waveform is created across the load due to the nature of classical PGs, which are formed of an RC network. With properly selected RC values, the exponential waveform plateau, rise and tail times, are controlled. In newer PGs, exponential waveform features can be imitated by ramped waveforms as shown in Fig. 2c [8], hence they can also be applied in insulation testing of power system components [11]. A multipulse waveform, shown in Fig. 2d, formed of wide-pulses

3

combined with a train of narrow pulses is preferred in food sterilization applications in order to minimize the generated heat without altering the food nutrition value [12].

In order to overcome the limitations (detailed in section II) of existing LV DC-fed newly-emerged power electronics-based PGs and solid-state Marx Pulse Generators (SMPGs), this paper proposes a new modular multilevel Voltage-Boosting Marx Pulse Generator (BMPG). The BMPG belongs to the hybrid Modular Multilevel Converter (MMC)-based PG family, where it is formed of two arms of series-connected MMC Half-Bridge SMs (HB-SMs) and an input boost (or buck-boost) converter. Unlike the conventional MMC-HB, the utilized SMs are configured such that their capacitors are charged directly (in parallel) via the input boost converter. Directing/Blocking (D/B) diodes are utilized to control the charging process and to block the capacitors from undesirable discharging. The diodes enable capacitor voltage balance, directing any overcharging current to achieve voltage balance, and prevent voltage drifting.

The input boost converter duty ratio δ is controlled by a single PI controller, which has a reference signal of the desired boost ratio λ_{ref}. Because of the D/B diodes, it only requires a voltage measurement of one boost converter level SM capacitor, whence a single voltage sensor is utilized for controlling all SM capacitor voltages.

In addition to presenting a new classification for available power electronics-based PG topologies (detailed in section II), the main contribution of this paper is a presentation of a robust modular, scalable generic HV PG efficiently fed from an LV DC input. The BMPG features are summarized as follows:

- Fed from an efficient LV DC input supply;

- Two-controllable gain variables; the boost converter duty ratio δ and the number of utilized series SMs N which enable topology scalability;

- One sensor per arm to measure all SM capacitor voltages;

4

- Requires two arms of MMC HB-SMs which is an established technology in terms of modularity and redundancy; and

- Can generate a flexible and controllable wide range of PEF waveforms.

Classification of available PGs is introduced in section II shedding light on power electronics-based PGs. The proposed BMPG converter features and principle of operation are detailed in sections III and IV, respectively. BMPG simulations and scaled-down proof-of-concept experimental results are presented in sections V and VI, respectively. A detailed quantitative comparison with similar Marx concept-based PGs is given in sections VII. Finally, BMPG topology variations are discussed in section VIII.

II. CLASSIFICATION OF THE EXISTING POWER ELECTRONICS BASED PGS

Several publications classify PGs based on their operation methodology [11]. With recent advances in power electronics devices and converters, several new PGs have emerged. Hence, an updated classification for the available PGs based on their topological variations is possible. There are two major PG categories as in Fig. 3, namely: classical PGs and power electronics-based PGs. The main classical PGs are Marx PG (MPG), pulse forming networks and Blumlein lines. Classical PG operation is based on storing the energy in inductors or capacitors then discharging that energy suddenly into the load [11].
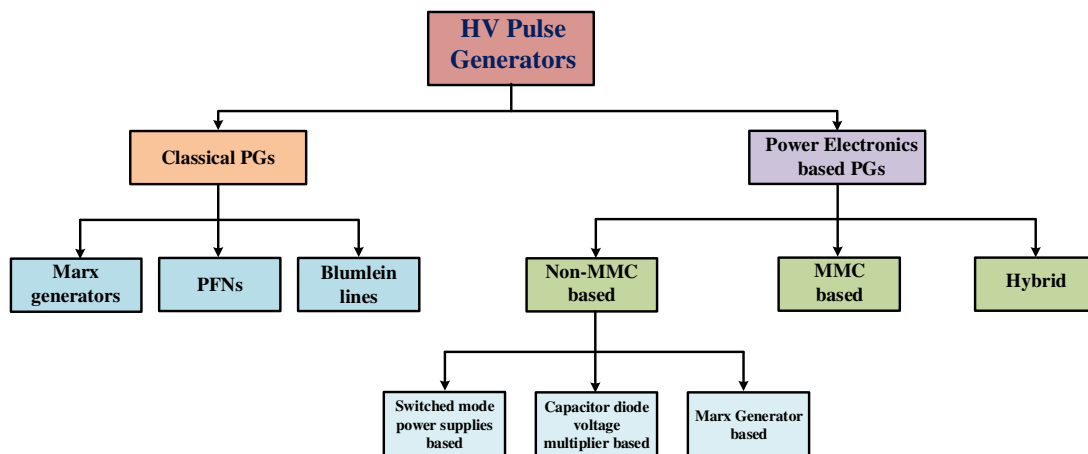

Fig. 3. Classification of HV PGs in the literature.

Among classical PGs, the MPG has been widely researched and used in electroporation applications. As illustrated in Fig. 4, the MPG comprises a group of N capacitors, C, which are inefficiently charged in parallel from the LV input supply V_s through the charging resistor r_c. The switching action takes place with the help of the spark gaps between stages, which have a break down voltage slightly higher than V_s. The HV pulse is formed when cascaded voltage break down of the spark gaps results in connecting the charged capacitors in series. For cascade break down, the first spark gap is intentionally triggered, exposing $2V_s$ voltage across the second spark gap forcing it to conduct. The breakdown process continues until all the spark gaps are shorted, hence a voltage pulse of NV_s is imposed across load R. The basic MPG generates unipolar pulses. If bipolar pulses are required, a similar stack fed from $-V_s$ is used, and the load is connected differentially between the two stack outputs [13]. The charging resistors are the control element in the MPG. If faster and shorter pulses are required, the charging resistances are reduced.
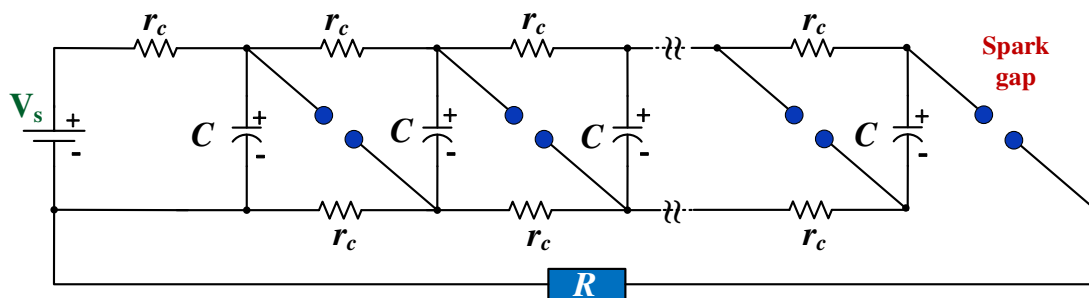

Fig. 4. Classical Marx generator.

In contrast, as shown in Fig. 3, power electronics-based PGs can be collated into three main groups, namely: Non-MMC-based, MMC-based, and hybrid topologies. MMC-based refers to topologies based on MMC phase-legs like used in HVDC transmission, adapted to HV pulse generation. The hybrid term refers to PGs that incorporate MMC SMs as a stage of pulse generation within the topology.

A. Non-MMC-based power electronics PGs

Basically, non-MMC-based PG topologies rely on utilizing power electronics to step up the voltage, thereafter, an HV switch in series with the load chops the HV. Fundamentally they can be divided into three sub-groups namely: Switch-Mode Power Supply (SMPS), Capacitor-Diode Voltage Multiplier (CDVM), and solid-state Marx Generators (SMPGs).

SMPS circuits are utilized in HV pulse generation topologies with attention to boost, buck-boost and the isolated buck-boost SMPS circuits due to their voltage step-up capabilities. In [14], the flyback converter is modified by removing the output filter capacitor and adding an RCD circuit across the transformer primary side, as shown in Fig. 5a. While the switch Q is ON, the transformer primary is exposed to V_s, and the input RCD capacitor is charged to $\delta V_s / (1 - \delta)$. When Q is OFF a negative unipolar HV pulse is generated across load R, with further voltage step up due to the transformer turns ratio. In [15], an input buck-boost converter feeds a stack of LV switch–capacitor units at the output stage, as shown in Fig. 5b. With control of the series switches Q, an HV pulse is impressed across the load with controllable dv/dt. But a complicated control algorithm is required and only unipolar pulses are generated. In [16], two boost converters are connected front-to-front while the load is connected differentially between the two outputs as shown in Fig. 5c. The topology can generate bipolar pulses, but its operation is dependent on the utilized passive elements. In [17], the boost converter-based circuit in Fig. 5d operates in a discontinuous conduction mode. The load is differentially connected between the input and output. The topology generates unipolar pulses, and no HV switch is required to create the HV pulses. The basic CDVM module, shown in Fig. 5e, has been incorporated in PG topologies [18]-[21]. The LV DC input voltage is used to charge the CDVM modules to generate HV DC then an HV switch is employed to chop the HV DC into unipolar rectangular pulses of the desired rate and width. For bipolar pulses, an H-bridge can be utilized at the output stage.
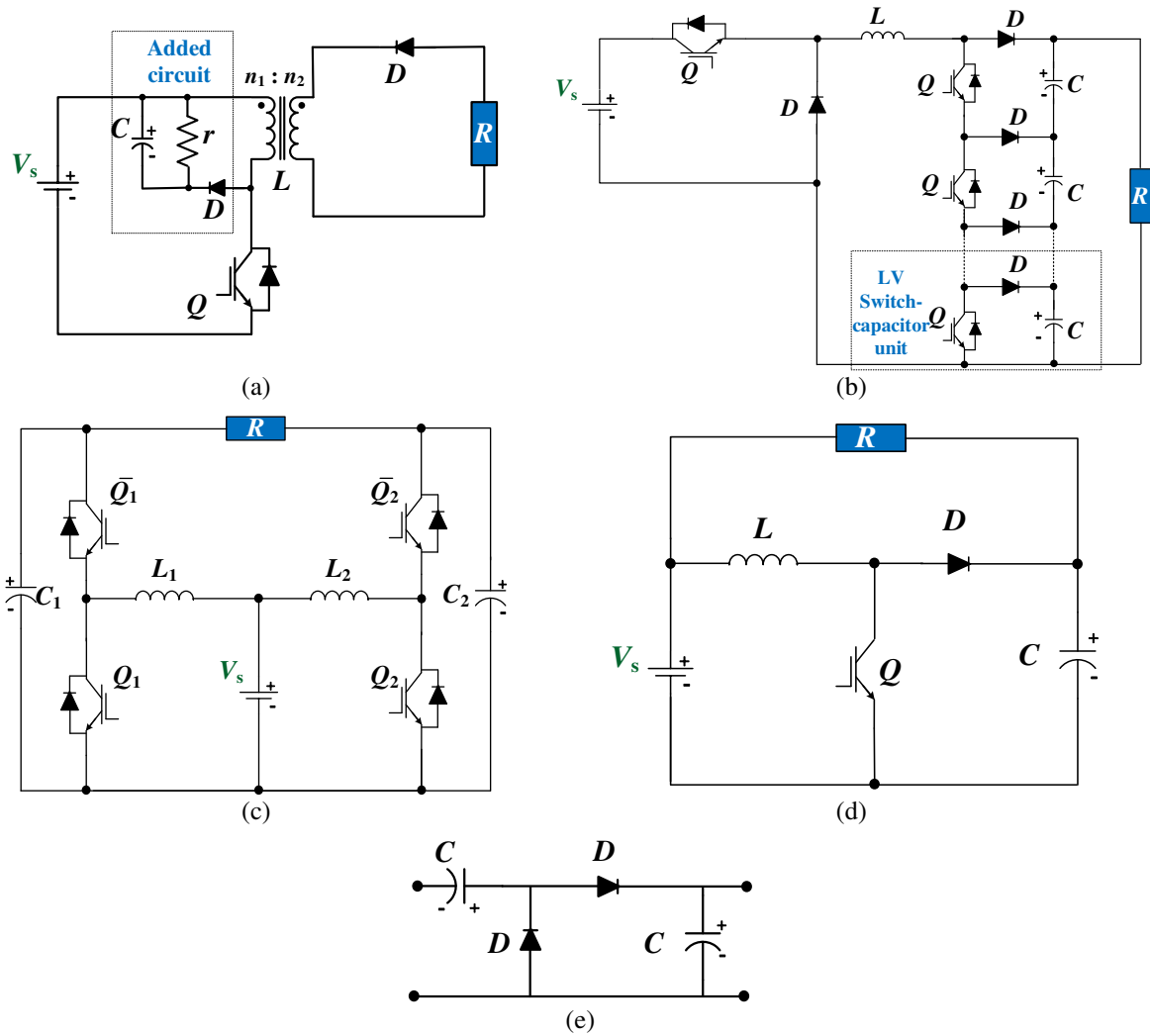
7

Fig. 5. Examples of non-MMC based PGs topologies. (a) Flyback based HV-PG. (b) buck-boost converter-based PG. (c) Front to front boost converter PG. (d) Boost converter based PG. (e) Basic CDVM module.

Mimicking the classical MPG, the SMPG has been studied [22]-[26]. The core idea is to charge a group of capacitors in parallel from a relatively LV DC supply and connect the charged capacitors in series for HV pulse generation. The spark gaps in MPG are replaced with power electronic switches in the SMPG. While sharing a similar operating principle, there are several topological variations of SMPGs, each with pros and cons. Generally, SMPG topologies can be divided into three sub-groups based on the component utilized in the repeated capacitor modules, control complexity, and ability to generate bipolar/unipolar pulses.
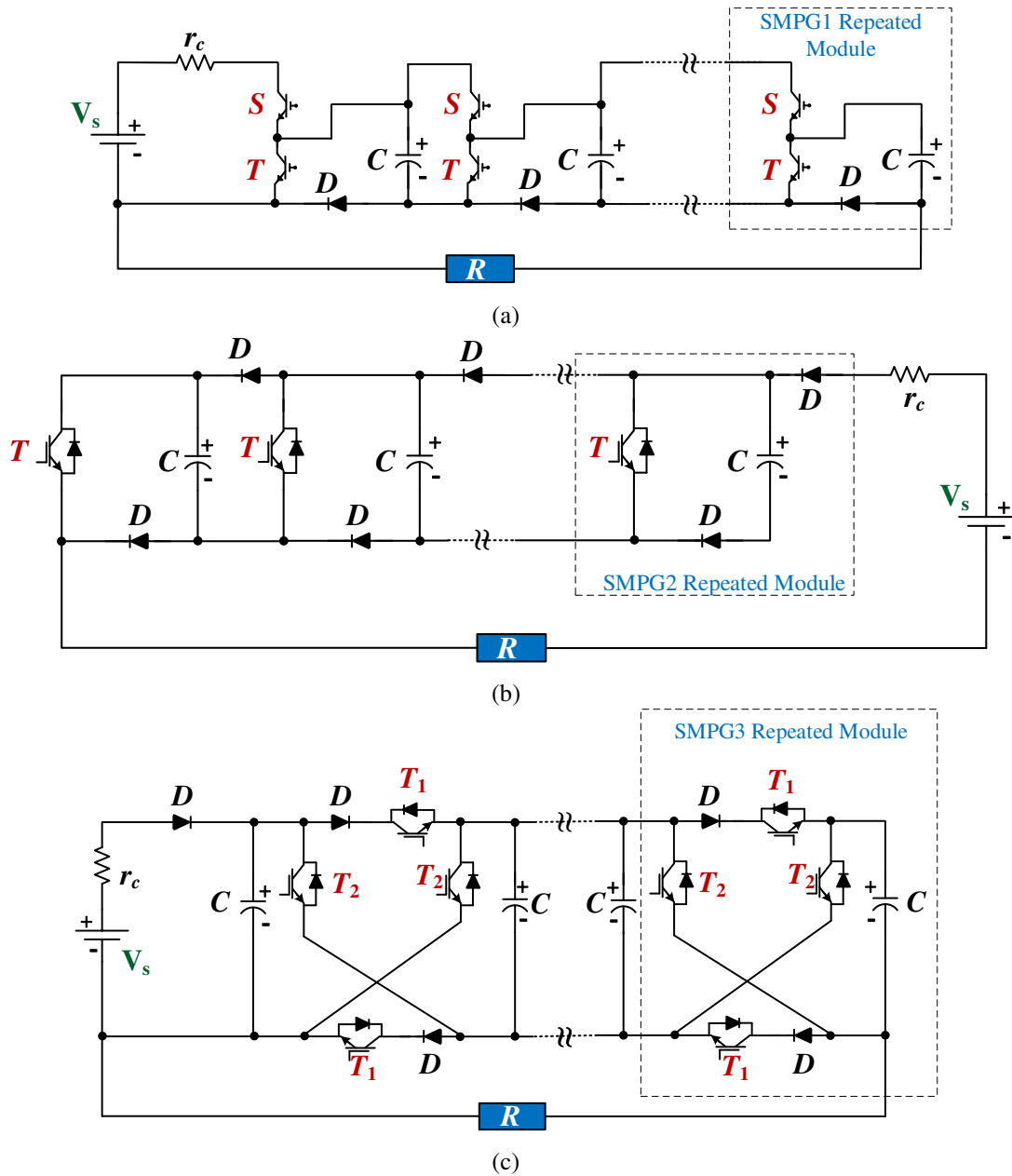
Fig. 6. Examples of SMPG topologies. (a) SMPG1. (b) SMPG2. (c) SMPG3

Fig. 6 shows three examples of the main available SMPGs:

- SMPG1 [22] (shown in Fig. 6a), has a simple structure, with a controllable capacitor charging/discharging mechanism, such that switches S facilitate charging of the capacitors while switches T allow pulse generation across the load. But IGBT ratings are not identical as the current stresses of S switches closer to V_s are higher due to parallel capacitor charging.

- With the reduced number of IGBTs than in SMPG1, SMPG2 [23] (shown in Fig. 6b) can provide unipolar pulses by simultaneous turn ON of all T switches for the required pulse time. Charging current control is needed in order to properly isolate the input supply during pulse generation, otherwise, a large charging input resistance will be required.

- SMPG1 and SMPG2 focused on improving the classical structure of an MPG with fewer power electronics switches and more control. They require two similar stacks for bipolar pulse generation. SMPG3 [24] (shown in Fig. 6c) addresses this issue, where T_1 IGBTs are used to charge the capacitors in parallel when turned ON, while T_2 switches are controlled to generated bipolar pulses across the load. However, in SMPG3 the voltage stresses on T_2 switches is twice the voltage stresses on T_1, and it needs one extra charged capacitor to allow the transition between pulse polarities.

Unlike the classical MPG, SMPG does not necessarily fully discharge their capacitors (switch voltage is safely clamped to the capacitor voltage). Yet, they suffer from large voltage droop which sometimes requires control action or additional passive components for mitigation [27], which is beyond the scope of this paper.

B. MMC based power electronics PGs

The phase-leg MMC-based PG topology in Fig. 7 is fed from HV DC input, V_s. Changing the modulating reference waveform, which is responsible for SMs insertion/bypass, allows mimicking of the modulating signal across the load. The default generated pulses are bipolar with a peak voltage of half the HV DC input. Voltage sensors are required for capacitor voltage balancing.
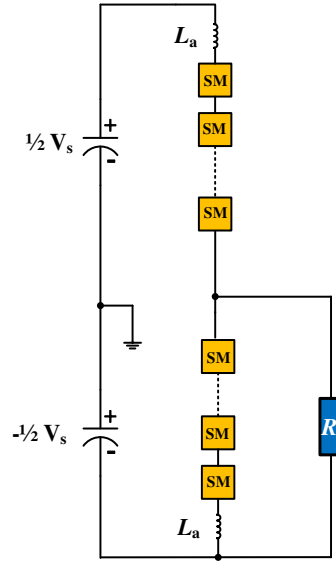
Fig. 7. Phase-leg MMC-based PG topology structure.

Sensorless SM capacitor voltage balancing in MMC based PG topologies is presented in [28]-[31] using HB-SMs. In [28]-[29], the SM-capacitor voltages are balanced by adding a diode between adjacent HB-SMs when employing a specific ON/OFF switching sequence on MMC HB-SM switches. For converter cost reduction, a conventional phase-leg of MMC HB-SMs is operated in a sensorless mode using the phase disposition PWM technique [30]. For each reference pulse waveform, the SM ON/OFF switching sequence is such that the SMs are inserted based on the same loading conditions resulting in balanced capacitor voltages. MMC phase-leg sensorless operation is attractive in terms of reducing hardware costs and complexity. But control complexity is increased as the number of the SMs is increased, and operation is adversely affected under SM failure.

C. Hybrid power electronics PGs

MMC-based PG topologies alleviate the need for HV switches and avoid the series connection of non-MMC-based PG topologies. The main limitation is the need for an HV DC input, and the MMC phase-leg can only generate bipolar pulses with a peak voltage of half the input HV DC. A solution to these limitations involves hybrid PG topologies, in which an LV

11

DC is the input stage followed by a voltage boosting mechanism. MMC SMs can be either incorporated at the voltage boosting stage or at the HV pulse creation stage or both. MMC SMs are employed to store energy in their capacitors, from the input supply, then transfer it to the load during HV pulse generation. HV pulses are created across the load without semiconductor device series connection while gaining MMC features such as modularity, scalability, and redundancy.

A boost converter fed from an LV DC source followed by a CDVM stage is proposed in [32] such that HV DC is obtained. The generated HV DC is then applied to the terminals of an MMC phase-leg. MMC SMs are employed to create the HV pulses across the load. In [33]-[34], a specific number of MMC-SMs (according to the required pulse peak voltage) are charged sequentially from an LV DC input then discharged in series across the load to generate HV rectangular pulses. Consequently, the capacitor charging time is elongated, which limits the pulse generation repetition rate and/or the number of utilized SMs.

Table I: General Features of Power Electronics-based Pulse Generator Groups

Attribute	Non-MMC-based	MMC-based	Hybrid
Examples	[14]-[26]	[8]-[9], [28]-[31]	[32]-[36]
Features	* No voltage sensors[1] * Simple control * Small footprint[2] * LV DC supply fed	* Scalable, modular, and redundant * Reduced semiconductor devices ratings * Generate different pulse waveforms	* MMC modules are connected across the load to form the pulses * No HV switches for HV DC chopping * Moderate footprint * LV DC supply fed
Limitations	* Parameter change sensitivity * Lacks modularity *HV switches * Generated pulses are mainly rectangular * Inflexible pulse characterizations	* HV DC supply fed * Essential SM capacitor voltage balancing *Large footprint * Possibly complicated control with sensorless operation	* Different pulse waveforms if SM capacitors are charged independently, otherwise drift in HV levels *Sensors to avoid capacitor voltage drift
	[1]Under open loop conditions.	[2]In comparison with MMC-based PGs.	

12

A comparison between the main features and limitations of the three voltage generator groups is presented in Table I. Generally, MMC-based topologies are fed from an HV DC input whereas the hybrid and the non-MMC-based types are fed from an LV DC input.

III. PROPOSED BMPG TOPOLOGY

This paper proposes a power electronics-based PG, which belongs to the hybrid group while adopting the Marx generator charging concept. Thus, it can be fed from an LV DC supply while keeping the features gained from utilizing MMC modules.

A. BMPG Topology Description

The proposed BMPG is shown in Fig. 8 and is formed of three main parts, namely: LV input boost converter module with its controller, upper arm (Arm1), and lower arm (Arm2). The boost converter module has input inductor L_i, two identical IGBTs Q_1 and Q_2, and four D/B diodes. The boost module has three terminals: B – a common, and A and C are connected to the positive terminal of the first SM capacitor C_{SM} in SM_{p1} in Arm1 and capacitor C_{SM} in SM_{n1} in Arm2, respectively. Arm1 generates positive polarity HV pulses across the load while Arm2 is responsible for generating the negative HV polarity pulse across the load. Each arm is formed of series-connected HB-SMs. The SMs of Arm1 are denoted as SM_{pj}, and the SMs of Arm2 are denoted as SM_{nj}, where p and n denote positive and negative pulses, respectively, and $j \in \{1, 2, ..., N\}$ where N is the number of SMs per arm.

Unlike in the conventional MMC, the SM capacitor positive terminals are sequentially connected to each other via external D/B diodes. These diodes allow the input boost converter to charge the required capacitor while blocking this current from flowing to capacitors adjacent to the boost converter. Each HB-SM is formed of two complementary (in an arm, both are never ON simultaneously, but may be OFF simultaneously) operated IGBT switches, T_m and

13

T_x. Control of these two switches, means the SM terminals can either support zero voltage, (SM *bypassed*, when T_m is ON and T_x is OFF) or the capacitor voltage, (SM *inserted*, when T_m is OFF and T_x is ON). In conventional HB-SM based topologies, SM capacitor charging is attained via the antiparallel diode of switch T_x. However, the charging mechanism of the proposed BMPG is different than the conventional MMC based PG. Rather each SM capacitor is charged directly from the input boost converter via the D/B diodes.
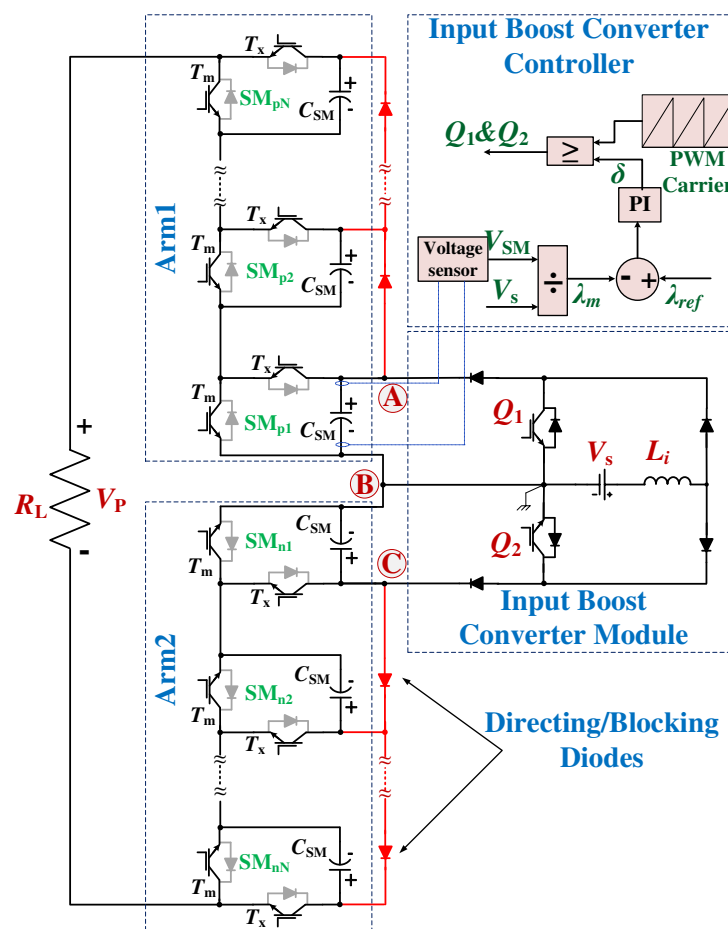

Fig. 8. The proposed BMPG topology.

In order to obtain HV pulses from an LV input supply, MMC sequential charging was used in [36] instead of charging the capacitors in parallel as in Marx generator. This allows reduced rated IGBTs. But, sequentially charged SMs result in a relatively low pulse repetition rate, as each SM capacitor has to be sequentially re-charged after contributing to the HV pulse.

Reference [36] presents an improvement by charging two SM capacitors (one from the upper arm and one from the lower arm) simultaneously. Adding a boost converter in the input stage with sequential charging, as in [37], deteriorates the repetition time as the charging time of the SM capacitors is divided into two parts. First, the boost converter inductor is energized, and then the capacitor is charged. The topology in [36]-[37] is constrained to rectangular pulses and requires switches with reverse blocking capabilities [38]-[39].

In the proposed BMPG, at start (black start), all the arms SM capacitors are resonantly charged in parallel from 0V, simultaneously via the D/B diodes. After first pulse delivery, the energy of the SM capacitors decreases due to the generated pulse. Then, for continuous operation without a large capacitor voltage droop, the SM-capacitors are re-charged in parallel, after each pulse delivery, to the desired voltage level. Thus, the BMPG acts as a Marx generator during continuous pulse generation allowing a high HV pulse repetition rate from an LV DC input. But the main differences are that the capacitors are not recharged from 0V after each pulse delivery as in MPG and no droop compensation control is needed as in an SMPG. Additionally, the BMPG can replicate all PEF pulse waveform shapes.

B. Addressing the Main SMPG Limitations

The proposed BMPG adopts the same charging mechanism as existing MPGs as well as SMPGs topologies. However, the main limitations in these topologies can be summarized as follows:

- Lack of modularity. For example, in SMPG1 (Fig. 6a), the IGBT switch current ratings are not identical. In SMPG3 (Fig. 6c), the SM switches T_2 have a different voltage rating to T_1.

- Lack of flexibility and degrees of freedom. During the charging process of the generator capacitors, a small charging/limiting resistor is used. If the input voltage is increased,

15

and to avoid paralleling IGBTs, the limiting resistor is increased. As a result, the pulse repetition rate of the generated pulses decreases.

- Lack of generic pulse waveform operation.Unipolar pulse polarities are generated. If bipolar pulses are required, two identical SMPGs are used while the load is connected differentially between them [40]. Four SMPGs are required for bipolar multipulse waveform generation.

- A classical MPG relies on fully discharging the capacitors after pulse generation. After each pulse delivery, the capacitors are charged from near zero voltage to the rated voltage. This is to avoid uncontrolled inrush current into higher level stages. But, this also limits the pulse waveform generation to exponential waveforms. Also, SMPG topologies require capacitor voltage droop mitigation.

- The maximum charging voltage of each capacitor is not greater than the input LV DC supply. If higher voltage pulses are required from the same input supply, the only solution is to increase the number of capacitor stages. Voltage boosting is not possible.

The main contributions of the proposed BMPG, addressing the limitations of the MPG and SMPGs, are:

- Utilizing MMC SMs, which offer inherently modular and redundant well-established technology. The D/B diode current ratings progressively decrease towards the outer SMs.

- The SM capacitors charge to the desired voltage level, with one voltage sensor (per pulse polarity) at the LV boost converter voltage level.

- Increased degree of freedom by utilizing an input inductor (as opposed to resistance) for capacitor charging without affecting the desired pulse repetition time.

- The charging input inductor is incorporated to form a boost converter (offering a control degree of freedom), which allows charging the SM capacitors to voltages

16

higher than the input LV DC supply. The input circuit can be modified to act as a buck-boost converter.

- The BMPG pulse voltage-peak has three control variables, the LV input voltage V_s, the boosting ratio λ, and the number of the utilized capacitors N (SMs). Specifically, for a fixed supply voltage V_s and a number of SM capacitors N, the voltage-peak can be controlled by the boost converter duty ratio λ.

- Flexible and controllable SM capacitors charging process. The charging process of the SM capacitors can be divided into two sequences: the first sequence is black start charging, while the second sequence is the continuous charging to keep the SM capacitors charged (topped up) and balanced.

- By maintaining SM capacitor voltage balance, via the D/B diodes, every SM capacitor can be seen as an isolated dc source. As a result, SM insertion can be controlled separately to form all electroporation pulse waveform shapes – forming a generic pulse waveform generator.

- The insertion/bypass of the SM-capacitors is software controlled to mimic all electroporation pulse-waveforms without changing the hardware topology.

IV. PROPOSED BMPG PULSE GENERATION OPERATION

A. *SM capacitor charging and discharging sequence*

The input boost converter is controlled by a PI controller, which generates the required duty ratio δ. This in turn controls Q_1 and Q_2 switch ON/OFF, creating the desired voltage magnitude λV_s (where $\lambda = 1/(1 - \delta)$) across the boost converter terminals AB and CB.

i. Black start

Before generating the first HV pulse, all SM capacitors (which retain zero charge) are connected across the boost converter terminals by turning on all SM switches T_m. Resonance occurs between the V_s, L_i and $2N$ parallel capacitors (through the directing/blocking D/B diodes), which for a high circuit quality-factor (efficient circuit), results in a final voltage $2V_s$ across all SM capacitors. The D/B diodes block reverse resonant current so that the each capacitor retains a boosted voltage $2V_s$. The peak resonate current $\hat{I}_r$ at ½t_r from the LV DC source is

$$\hat{I}_r = \frac{V_s}{\sqrt{L_i/2NC_{SM}}} \tag{1}$$

where the resonant current pulse period t_r is defined as (half the full natural resonant period)

$$t_r = \pi\sqrt{2L_iNC_{SM}} \tag{2}$$

Unlike the Marx equivalent, the SMs here are voltage boosted above the LV DC source voltage V_s at both start up and during normal operation. If the designed SM operating voltage is higher than $2V_s$, the boost converter is used to charge the SMs in parallel to the desired voltage, before generating the first output pulse. If the resonant energy is in excess of the LV DC source rating, a buck-boost converter (which operates in a current limiting control mode) can be used, giving slower controlled SM capacitor charging from zero to a voltage less than or higher than V_s.

Although a single switch in the input boost (or buck-boost) converter is sufficient (see Fig. 18), two switches operating simultaneously means a lower switch current rating or faster charging.
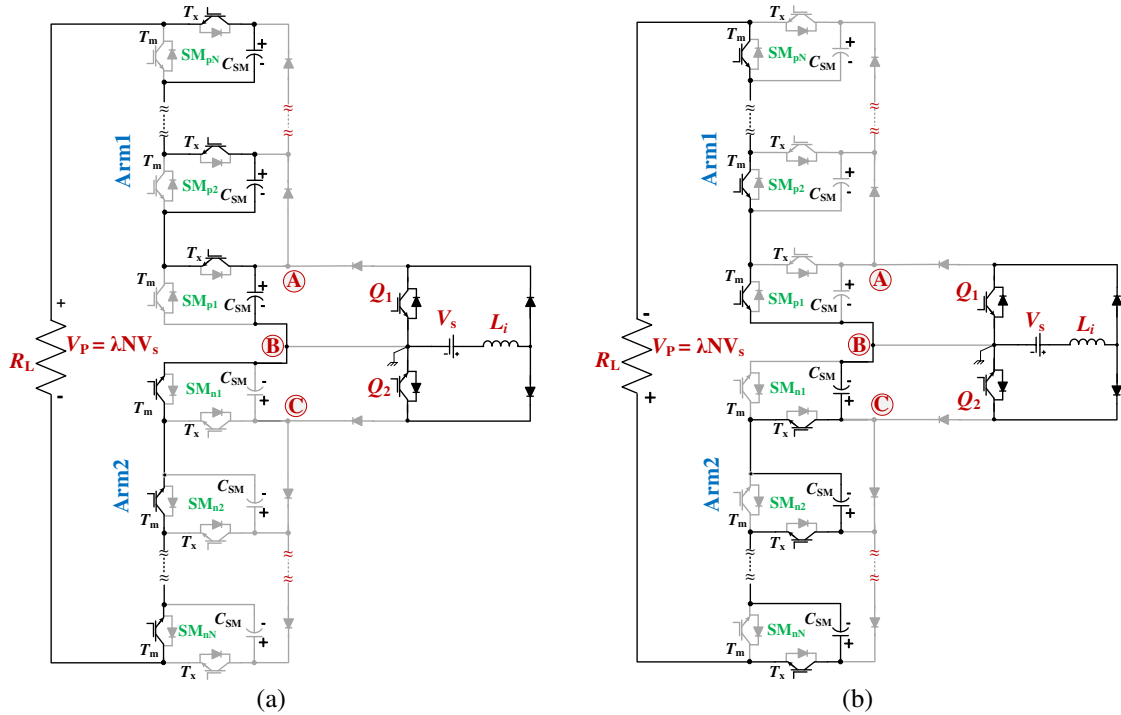
Fig. 9. Bipolar rectangular pulse generation. (a) Positive pulse. (b) Negative pulse

ii. Pulse generation

After charging (or having topped up) all the SM capacitors, HV bipolar pulse generation

across the load is initiated by allowing Arm1 SM capacitors to partially discharge into the load

(by switching ON T_x of Arm1 and switching ON T_m of Arm2 simultaneously, see Fig. 9a).

That is, for positive pulses, SMs in Arm1 are inserted, and bypassed in Arm2. For negative

pulses, the states are: bypass Arm2 SMs and insert Arm1 SMs, see Fig. 9b. SM switch operation

is always complementary. After the pulse is delivered to the load, the remaining voltage in each

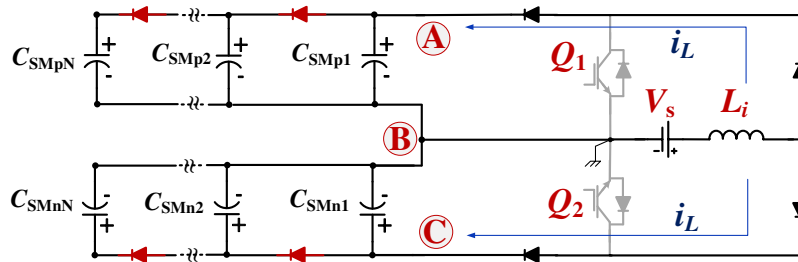SM capacitor is $\beta\lambda V_s$ (not falling below V_s with a boost converter, that is $\beta\lambda \geq 1$).

Fig. 10. Continuous charging for the SM-capacitors.

19

iii. Capacitor topping up (recharging)

After the first HV pulse delivery, involving certain provisions to be specified, re-charging during continuous boost converter operation can occur with all the MMC-SMs bypassed (T_m ON) as shown in the equivalent circuit in Fig. 10. All the SM capacitors are connected in parallel as in classical Marx generator. But, the capacitor recharging is not from 0V, rather in excess of V_s. The capacitors incur a voltage droop $(1 - \beta)$ pu due to transferring some of their energy to the load. This droop can be specified by SM capacitance selection (increase capacitance to decrease droop). Voltage sharing across SMs is inherent in the charging (all SM capacitors charge in parallel to a maximum of λV_s) and series connection discharging mechanisms (SMs either remain unchanged or discharge below λV_s).

SM-capacitors insertion and bypassing for different pulse waveforms generation should comply with either or both of:

- An inner capacitor is always *inserted* before an outer capacitor.

- An outer capacitor is always *bypassed* before an inner capacitor.

This means an outer capacitor will always retain a high voltage than an inner capacitor, after pulse generation. That is $V_{SMN} > V_{SMN-1} > \cdots > V_{SM1}$, in Fig. 10, otherwise uncontrolled current flows through the directing diodes in the direction toward the Nth SM when charging the capacitors in parallel. These two constraints are not considered a limitation, if a steep leading edge is the prime pulse requirement since all SMs can be inserted simultaneously. But SM bypassing during the pulse trailing edge should comply with the second constraint. Both SM capacitor charging and pulse generation do not involve an antiparallel diode across switches T_x and T_m. Both SM capacitor charging and pulse generation do not involve an antiparallel diode across switches T_x and T_m. But the diode in antiparallel with T_m is necessary to clamp switch T_x to the capacitor voltage at pulse turn-off.

B. BMPG Parameters Estimation

The inductance is selected to control the current ripple of the charging current of the parallel connected SM capacitors. Hence low rated semiconductor devices can be utilized, and the converter efficiency is improved (no resistor losses). Thus the inductance (assuming continuous inductor current) can be estimated from

$$L_i = \frac{V_s \delta T_Q}{\Delta I_L} \tag{3}$$

where ΔI_L is the inductor current ripple and $T_Q = 1/f_{PWM}$ is the boost converter repetition time. SM footprint/volume is dominated by capacitance/voltage size. An estimation of SM capacitance is given in [30]:

$$C_{SM} = \frac{2N t_{pl}}{(1 - \beta^2)R} \tag{4}$$

where t_{pl} is the widest pulse polarity of the generated bipolar pulses across the load R, and β is the per unit capacitorremaining voltage after pulse delivery. The capacitor recharging energy is delivered to the load during the previously generated pulse. The generated pulse repetition rate is restricted by the allowable maximum average current I_i from the LV DC source, given by:

$$E_{dc} = V_s I_i T_Q \tag{5}$$

where E_{dc} is the supplied LV DC energy per PWM cycle. The pulse energy to be replaced for N SMs (a unipolar pulse) is

$$E_{pl} = N[\tfrac{1}{2}C_{SM}(\lambda V_s)^2 - \tfrac{1}{2}C_{SM}(\beta\lambda V_s)^2] = \tfrac{1}{2}NC_{SM}(\lambda V_s)^2(1 - \beta^2) \tag{6}$$

If the energy from the LV DC source is delivered over n PWM carrier cycles ($n \geq 1$) to control the average LV DC current, then the minimum pulse repetition period is

$$T_s = t_P + t_N + (n - \tfrac{1}{2})T_Q \tag{7}$$

where t_P and t_N are the positive and negative pulse durations respectively. Unlike conventional sequential charging MMC topologies [36], the repetition rate is increased

21

significantly with the BMPG charging approach, where the $2N$ SMs are charged (topped up) progressively simultaneously. For proper operation, the carrier PWM frequency for the input boost converter should be higher than the generated pulse repetition rate, so that a number of PWM cycles ($n > 1$) occur for recharging control.

Table II: Simulation and Experimentation Specifications of the BMPG

Parameter		Simulation	Experimental
LV DC input voltage	V_s	500V	50V
Peak-Peak pulse voltage	V_{PP}	10kV	600V
Number of SMs per Arm	N	5	3
Load resistance	R	500Ω	500Ω
SM capacitance	C_{SM}	5μF	5 μF
Input inductance	L_i	1mH	3.5mH
PWM carrier repetition time	T_Q	25μs	40μs
Pulse duration for both polarities	t_{pl}	25μs	50μs
Percent remaining voltage (pu)	β	0.95	

V.   BMPG SIMULATION VERIFICATION

The proposed BMPG, in Fig. 8, with five SMs per each arm, is Matlab/Simulink simulated with the specifications in Table II. With a voltage-boost ratio of $\lambda = 2$, ($\delta = \frac{1}{2}$), a bipolar rectangular pulse waveform of $T_s = 175$μs and symmetrical pulse durations of $t_P = t_N = 25$μs is shown in Fig. 11a. Each SM capacitor is charged to 1kV as shown in Fig. 11b, thus with five SMs per arm, the peak voltage of the generated rectangular pulse is 5kV, as shown in Fig. 11a. The current and the voltage of the input boost converter inductor are shown in Fig. 11c. The controller generated duty ratio δ and the PWM carrier are shown in Fig. 11d.

The topology can generate commonly used pulse waveforms, such as a ramp and multipulse. With a voltage-boost ratio of $\lambda = 2$, Fig. 12a shows a symmetrical bipolar ramp pulse waveform with $T_s = 190$μs. The SM capacitors are inserted simultaneously, hence, a peak voltage of 5kV appears across the load for the required plateau time; Fig. 12a, 20μs, then the SM capacitors are bypassed progressively (an outer SM before an inner SM, $j = 5, 4, 3, 2, 1$) every 5μs until all are bypassed. In Fig. 12b, with a voltage-boost ratio of $\lambda = 2$, a symmetrical

bipolar multipulse waveform of $T_s = 375\mu$s is shown. Two superimposed pulses of wider and narrow duration is created by inserting all the arm SM capacitors simultaneously, then bypassing some (outer SMs) simultaneously. The process is repeated based on the desired narrow pulse repetition time. In Fig. 12b, the wider pulse repetition time is 375μs, while the narrower pulse repetition time is 50μs, with two SMs bypassed.
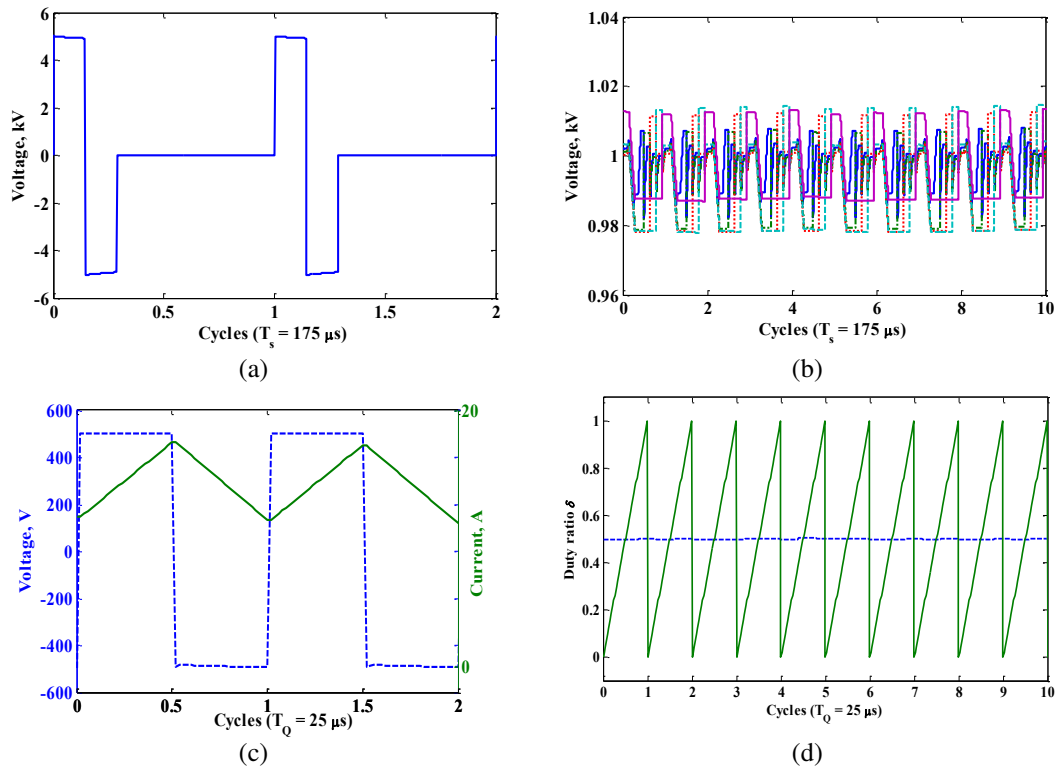

Fig. 11. Simulation results for BMPG generated bipolar rectangular waveform ($\lambda = 2$).
(a) Generated pulses. (b) Arm2 capacitor-voltages. (c) Input inductor voltage and current.
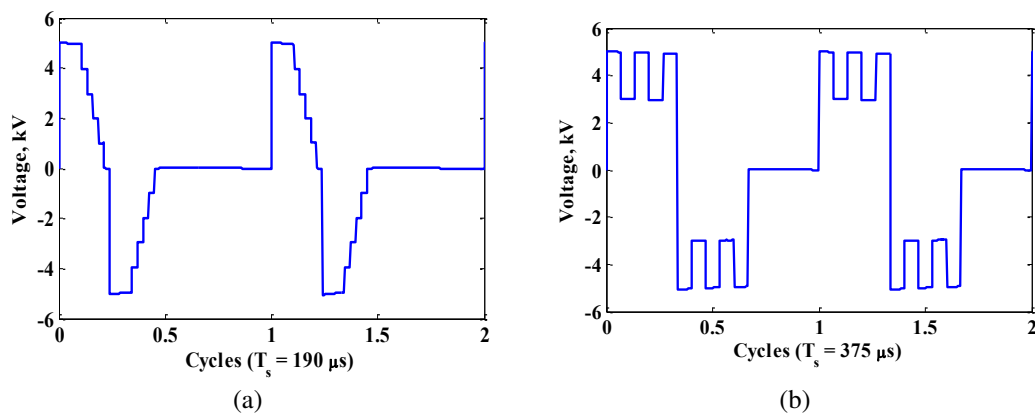(d) Input boost converter duty ratio.

Fig. 12. Simulation results for BMPG commonly used PEF bipolar pulse waveforms ($\lambda = 2$).
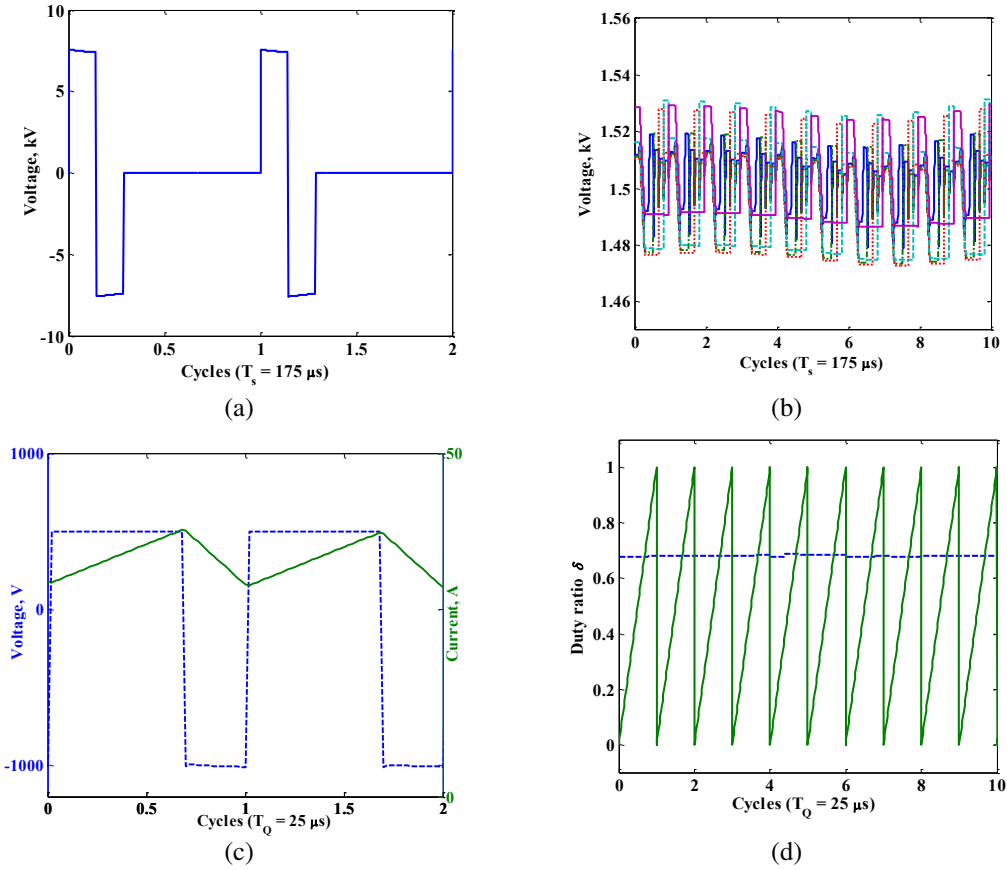(a) Ramp. (b) Multipulse.

Fig. 13. Simulation results for BMPG generated bipolar rectangular waveform ($\lambda = 3$).
(a) Generated pulses. (b) Arm2 capacitor-voltages. (c) Input inductor voltage and current.
(d) Input boost converter duty ratio.

Applying closed loop current control to the input boost converter allows voltage boost control, and the controller automatically assigns the correct inductor energizing time, such that the SM capacitors are charged at maximum current to the desired voltage λV_S. Fig. 13a shows a bipolar rectangular pulse waveform of 7.5kV peak, $T_s = 175\,\mu$s and symmetrical pulse durations of $t_P = t_N = 25\mu$s when $\lambda = 3$. The SM capacitors charge to 1.5kV as shown in Fig. 13b, while the input inductor voltage and current, and the controller generated duty ratio are in Fig. 13c and Fig. 13d, respectively. Generation of bipolar ramp pulses and multipulse waveforms are shown in Fig. 14a and Fig. 14b, respectively.
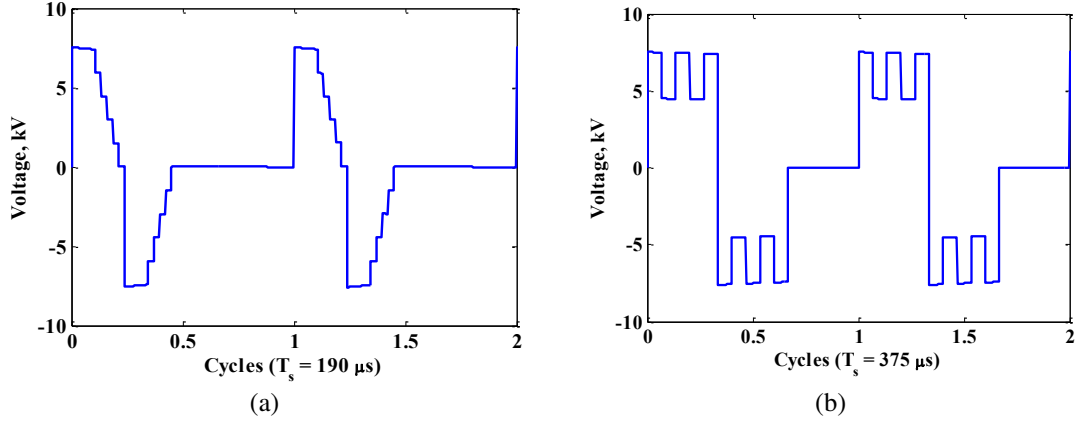
Fig. 14. Simulation results for BMPG commonly used PEF bipolar pulse waveforms ($\lambda = 3$).
(a) Ramp. (b) Multipulse.

VI.   BMPG EXPERIMENTAL VERIFICATION

The proof of concept scaled-down experimental set-up shown in Fig. 15 uses IGBT switches STGW30NC60WD in Arm1, Arm2, and the input boost converter, with IXYS DSEI30-10A directing/blocking power diodes. Each arm is comprised of three SMs.

With a boost factor of $\lambda = 2$, $V_s = 50V$ and the specification listed in Table II, three trains of conventional PEF pulse waveforms are generated. A zoomed view of the three pulse waveforms is depicted in Fig. 16, along with Arm2 SM capacitor voltages. Two cycles for the rectangular ($T_s = 200\mu s$), ramp ($T_s = 360\mu s$) and the multipulse ($T_s = 520\mu s$) waveforms are shown in Fig. 16a, Fig. 16b and Fig. 16c, respectively. The rectangular pulses with $t_P = t_N = 40\mu s$ are given in Fig. 16a. Fig. 16b shows ramp pulses with a step-voltage of $20\mu s$ whereas Fig. 16c shows a multipulse train when a single SM is bypassed and inserted every $20\mu s$ to form the short duration pulses. For the 50V input voltage, each SM capacitor charges to 100V, as shown in Fig. 16. The input boost-converter voltage and current are shown in Fig. 16d, during rectangular pulses generation.
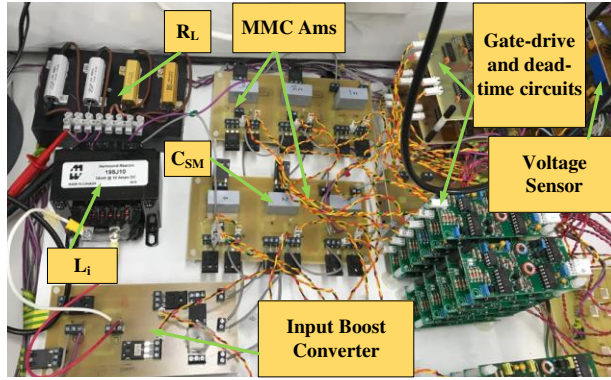
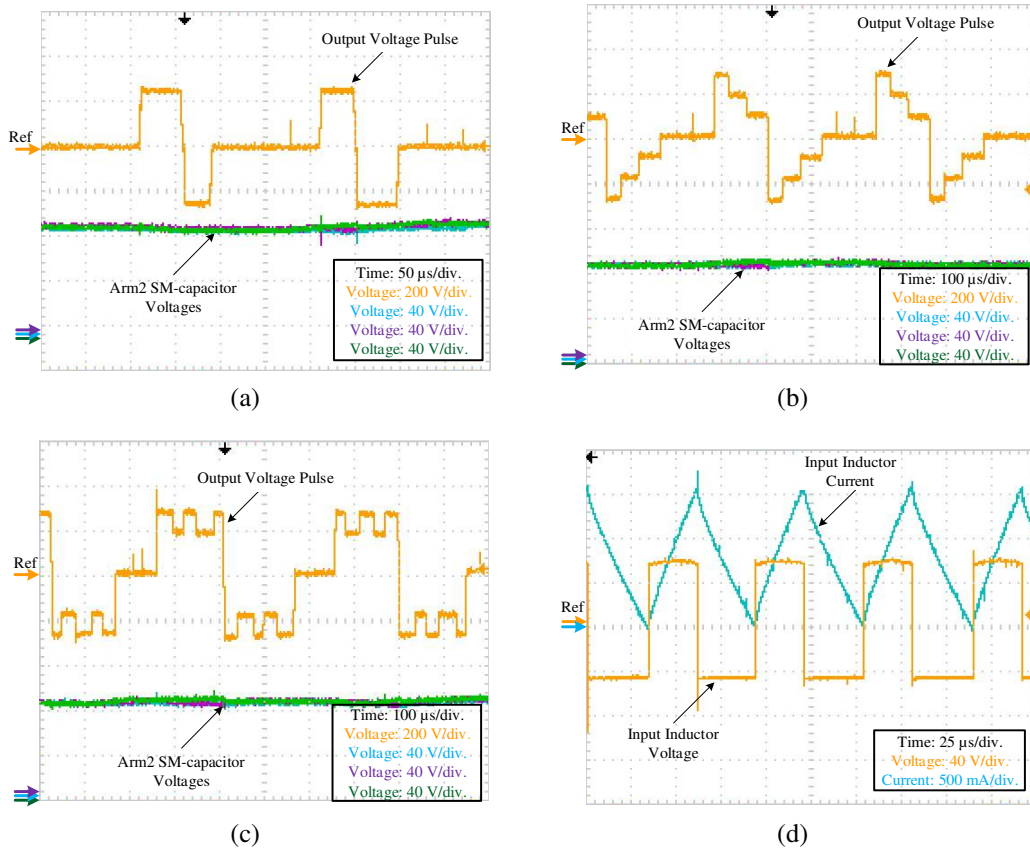Fig. 15. The proof of concept scaled down BMPG experimental rig.

Fig. 16. BMPG experimental results for conventional PEF pulse waveforms ($\lambda = 2$) along with Arm2 SM-capacitor voltages. (a) Bipolar rectangular pulses. (b) Bipolar ramp pulses. (c) Bipolar multipulse pulses. (d) Input inductor voltage and current when generating rectangular pulses.

In order to investigate high gain voltage pulses with low voltage DC input, the input voltage is reduced to 30V with a boost factor $\lambda = 3$, ($\delta = ⅔$). Hence, each SM capacitor is charged to 90V as shown in Fig. 17and the pulse peak voltage is 270V. The generated bipolar rectangular pulses with $t_P = t_N = 50\,\mu s$ and $T_s = 250\,\mu s$ are in Fig. 17a, along with Arm2 capacitor voltages. Not only bipolar pulses can be generated with the BMPG, but unipolar pulse

generation is possible, by disabling (no arm insertion) the unwanted pulse polarity during pulse generation. This is illustrated in Fig. 17b and Fig. 17c for positive unipolar ramp pulses ($T_s = 240\mu s$) and a negative unipolar multipulse ($T_s = 320\mu s$), respectively.
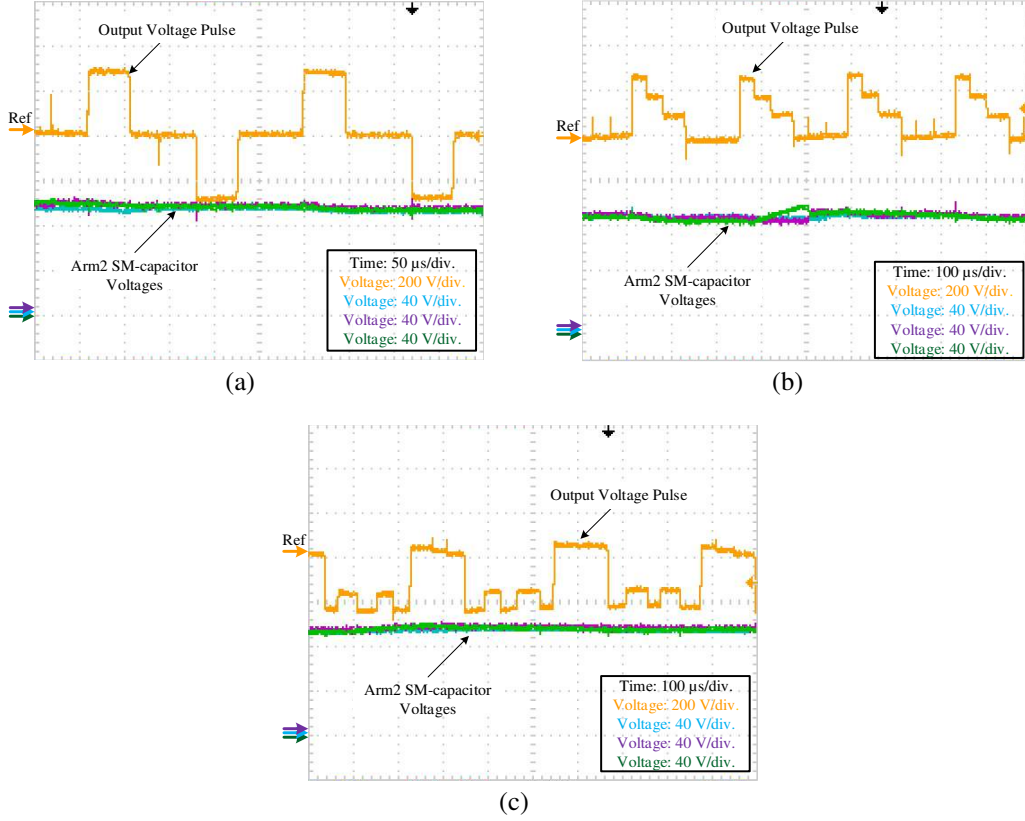

Fig. 17. BMPG experimental results for bipolar pulse waveforms and Arm2 capacitor voltages with $\lambda = 3$. (a) Bipolar rectangular. (b) Positive unipolar ramp. (c) Negative unipolar multipulse.

VII.   BMPG COMPARED TO SIMILAR SOLID-STATE MARX PGs

As previously illustrated, the proposed BMPG shares the Marx concept of operation with several topologies (Fig. 6) namely SMPG1, SMPG2, and SMPG3 mentioned in section II. As a result in order to complete this study, a detailed comparison between these topologies and the unipolar/bipolar versions of the BMPG is presented in Table III. The quantitative comparison is based on generating a rectangular 5kV, 10μs pulse waveform, with a pulse repetition time of 100μs, using an input voltage of 1kV, and a resistive load of 1kΩ.

Without employing any voltage droop compensation, the proposed BMPG has smaller capacitor sizes and a lower number of modules, therefore, it has a smaller footprint. For the same input voltage, the voltage stresses on the unipolar BMPG switches are 67% higher than SMPG1 and SMPG2 while in bipolar BMPG case, the voltage stresses are reduced by 33% in comparison with SMPG3. The voltage stresses in the BMPG case can be reduced by adding one more module and reducing the boosting factor. This is application-dependent, and a trade-off between size and cost. The charging efficiency for all the topologies is acceptable, providing that ideal switches are assumed. Generally, an SMPS (the LV DC to DC converter) can have a high efficiency (typically around 99%), with losses associated with semiconductor on-state and switching losses, and inductor losses [41]. The voltage gain efficiency, as expected, in resistive charging based SMPGs, is lower than the proposed BMPG, as the capacitor voltages cannot be 100% equal to the input supply voltage. In contrast, the boost converter in the proposed BMPG, assures 100% assigned average capacitor voltage, therefore 100% voltage gain efficiency. The fixed average voltage is formed by assuring that the start of the pulse peak voltage is slightly higher than the end of pulse voltage peak.

VIII. BMPG TOPOLOGY VARIATIONS

A. *Input Converter Stage Variations*

With Arm1 and Arm2 intact, the input terminals A, B and C can be connected to a buck-boost converter (rather than a boost converter) as shown in Fig. 18a. This feature may be necessary for soft starting from a fixed or uncontrolled DC source. Hence, by utilizing the buck-boost converter, the range of the SM voltage is extended from 0 to λV_s (instead of V_s to λV_s in boost converter case). If soft starting is not required, a boost converter is possible, since it has a wider control range and less stresses on the input switches, compared to the buck-boost converter

[42]. Depending on DC converter stress levels, a single switch boost or buck-boost converter can be used, thereby minimizing the number of components, as shown in Fig. 18b and Fig. 18c.

Table III: Comparison between Proposed and Main literature Marx generator based Topologies

	Literature Marx solid state topologies			Proposed BMPG topologies	
	SMPG1	SMPG2	SMPG3	Unipolar	Bipolar
Topology	Fig. 6a	Fig. 6b	Fig. 6c	Fig. 19	Fig. 20
Charging element	$r_c = 0.333\Omega$	$r_c = 0.333\Omega$	$r_c = 0.333\Omega$	$L_i = 0.167\text{mH}$	$L_i = 0.167\text{mH}$
Number of modules	5	5	5	3	3
Number of capacitors	5	5	6	3	3
Module Capacitance	$C = 10.8\mu\text{F}$	$C = 10.8\mu\text{F}$	$C = 9.6\mu\text{F}$	$C_{SM} = 3\mu\text{F}$	$C_{SM} = 6\mu\text{F}$
Number of IGBTs	10	5	20	8	16
Number of Diodes	5	10	10	3	3
Max. voltage stress on switches	V_s	V_s	$2V_s$	$1.67V_s$	$1.67V_s$
Percentage capacitor voltage droop [1]	1.1%	3%	0.7%	0.3%	0.3%
Charging efficiency [2]	99.45%	98.5%	99.65%	99.85%[3]	99.85%[3]
Voltage gain efficiency [4]	99.1%	97%	99.3%	100%	100%
Generic pulse waveform mode	Not possible	Not possible	Possible with five voltage sensors	Possible with one voltage sensor	Possible with one voltage sensor
Special requirements	Modules near power supply must be handle higher currents than the far ones	Input supply current must be sensed and controlled during capacitors charging. During pulse generation, proper isolation of the supply is needed.	Pulse participating IGBTs must be rated at the double the input voltage. Some ratings may require series connected switches.	Closed loop control is required for proper pulse voltage generation. An inner capacitor is always inserted before an outer capacitor and bypassed after it.	

[1] The percentage voltage droop is calculated as $(1 - \beta)\%$, where, β is the per unit remaining capacitor voltage after pulse delivery.
[2] The charging efficiency can be calculated as $(1 - \frac{1}{2}(1 - \beta))\%$ as in [36].
[3] SMPS theoretical efficiency is 100%.
[4] The voltage gain efficiency is calculated as $(V_{av}/V_p)\%$, where V_{av} is the average plateau voltage of the generated pulse.
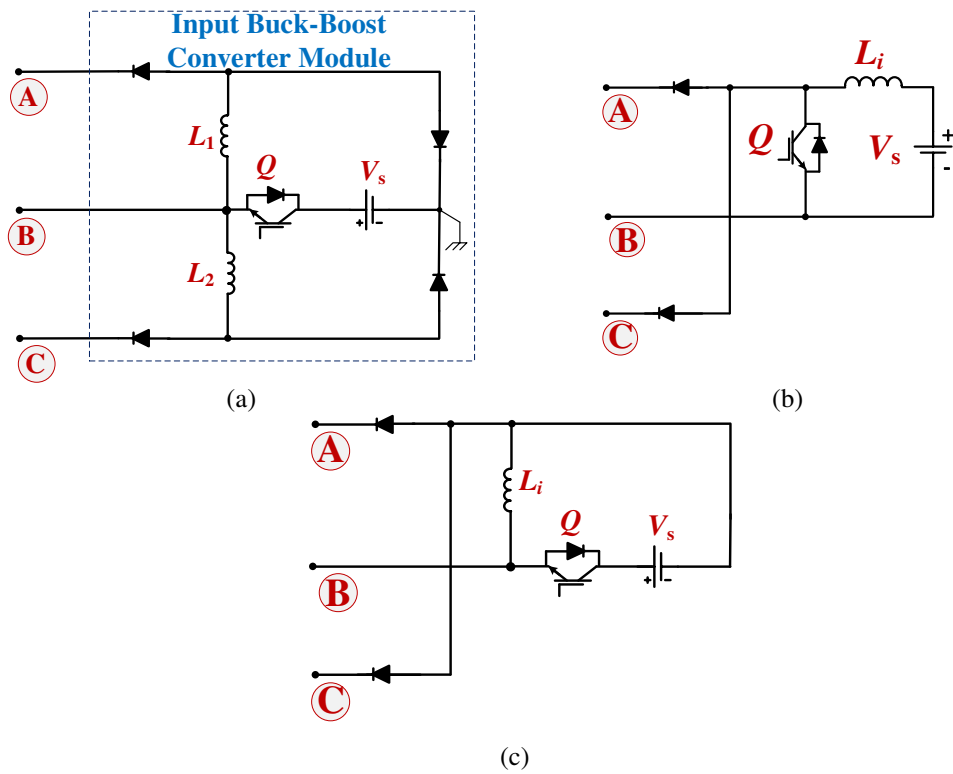
Fig. 18. Input terminal variation. (a) Buck-boost converter module. (b) Single switch boost converter. (c) Single inductor buck-boost.
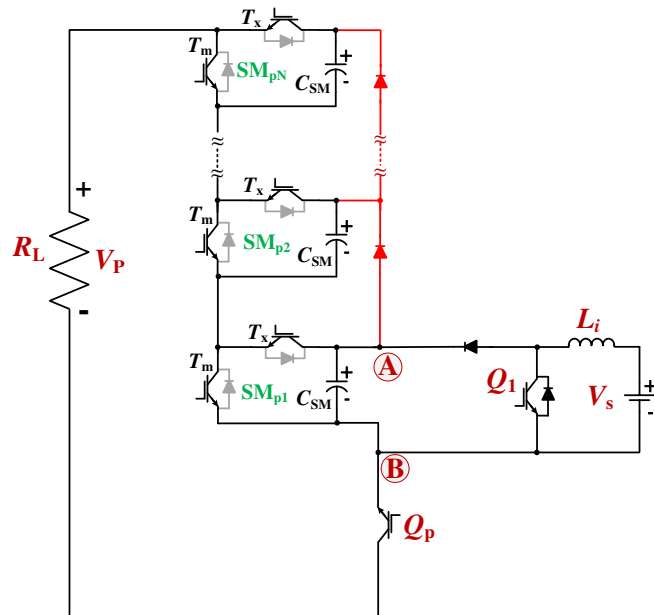

Fig. 19. Unipolar BMPG topology.

B. *Unipolar BMPG Topology*

If the application requires only unipolar pulses, one arm can be removed. For example, Fig. 19 illustrates the unipolar BMPG which can generate rectangular pulses of positive polarity. Arm2 is replaced by an IGBT switch Q_p, rated at the input terminals (AB) voltage level, and this switch is ON during pulse generation and OFF otherwise.

C. *BMPG with Full-Bridge SMs*

The BMPG topology variation in Fig. 20 allows further size/footprint reduction. The HB-SMs of Arm1 are replaced by Full-Bridge (FB) SMs. As a result, two input terminals and one boost/buck-boost converter are only needed to charge the SM capacitors. Arm2 in Fig. 8 is replaced with a bi-directional IGBT/diode switch rated at the input terminals (AB) voltage level. IGBT, Q_p, is ON during positive polarity pulse generation and OFF otherwise. Diode D_n conducts during negative pulse generation. The D/B diodes in Fig. 8 are modified by reverse voltage blocking switches Q_b. During pulse generation, the D/B switches are OFF to prevent short circuiting the lower SM capacitors during negative pulse generation when the D/B diodes are forward biased. During charging/recharging of the SM capacitors, Q_b switches are ON. The switches are rated at the input terminals (AB) voltage level. Each FB-SM is formed of a capacitor and four IGBTs T_1, T_2, T_3 and T_4. Table IV details the topology switch states for $N = 3$ during bipolar rectangular pulse generation and during continuous SM capacitors recharging. Additionally, Table IV shows the sequence of bypassing each SM capacitor used when mimicking various pulse waveforms.
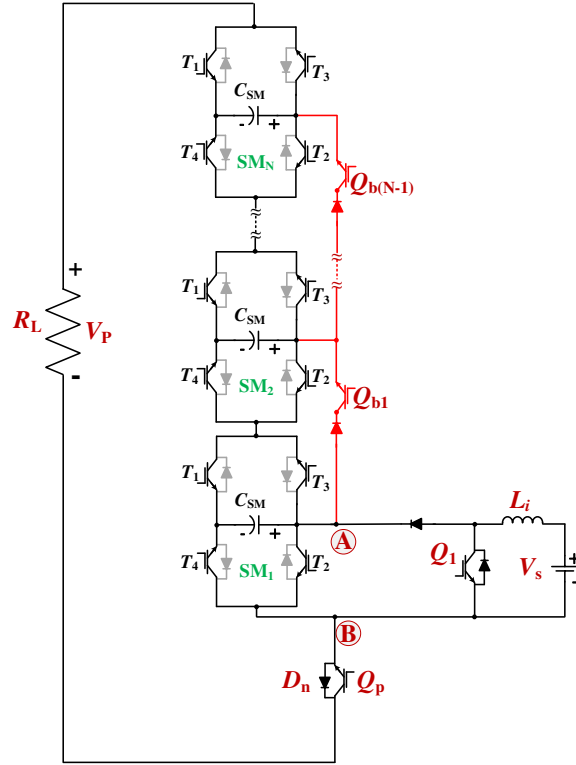
Fig. 20. BMPG topology with FB-SMs.

Table IV: Switch States of FB based BMPG during Pulse Generation,
SM Bypass and Continuous Charging Mode for $N = 3$

Operation	Q_p	D_n	T_1	T_2	T_3	T_4	Q_{b1}	Q_{b2}
+ve pulse polarity	ON	×	OFF	OFF	ON	ON	OFF	OFF
-ve pulse polarity	×	ON	ON	ON	OFF	OFF	OFF	OFF
Marx Mode	×	×	ON	OFF	OFF	ON	ON	ON
SMs Bypass +ve pulse	ON	×	OFF	OFF	OFF	ON	OFF	OFF
SMs Bypass -ve pulse	×	ON	ON	OFF	OFF	OFF	OFF	OFF

IX. CONCLUSION

After introducing a classification of the power electronics-based pulse generators, this paper presented a novel HV pulse generator based on two arms of series MMC HB-SMs. An SM capacitor charging technique was proposed using a low voltage input boost converter such that all the capacitors in both arms are charged simultaneously. The SM capacitor charging process can be divided into two processes. First (black start), all the arms SM capacitors are resonantly charged in parallel from 0V, simultaneously via directing diodes. After first pulse delivery and subsequent pulses, the energy of the SM capacitors decreases due to the generated pulse. Then,

for continuous operation without fully discharging the SM capacitors or having a large voltage droop, the SM-capacitors are re-charged in parallel to the desired voltage level. Thus, the BMPG acts as a Marx generator during continuous pulse generation allowing high repetition rate HV pulses from an LV DC input. However, the main differences are that the capacitors are not recharged from 0V after each pulse delivery or need droop mitigation control, and the BMPG can imitate all pulse waveform shapes.

With a single voltage sensor measuring the first SM capacitor voltage, the input boost converter duty ratio is controlled to charge the SM capacitors to the desired voltage boost level. The proposed structure for SM capacitor charging and SM directing/blocking diodes, allow individual control of each arm SM capacitor without voltage sensors for each SM capacitor, with voltage balancing assured.

Conventional electroporation pulse waveforms can be generated in bipolar and unipolar forms by controlling the insertion/bypass of the SM capacitors. Topology variations were presented to suit different application requirements and optimize available converter size/space. Replacing the input boost with a buck-boost converter, hence, giving start-up ramp charging of SM capacitors is possible. If unipolar pulses are sought, the unnecessary arm polarity can be replaced by a single IGBT switch rated at the boost converter voltage level. Replacing the HB-SMs with FB-SMs is also possible.

A wide range of pulse waveforms was simulated and produced experimentally using a scaled-down rig. The proposed BMPG has the general features of modularity, voltage sharing, scalability, flexibility, and controllability with a reduced footprint, which promotes it for electroporation application.

R E F E R E N C E S

[1] S. H. Jayaram, "Sterilization of liquid foods by pulsed electric fields," *IEEE Electr. Insul. Mag.,* vol. 16, no. 6, pp. 17-25, 2000.S.

[2] C. Jiang, R. V. Davalos, and J. C. Bischof, "A review of basic to clinical studies of irreversible electroporation therapy," *IEEE Trans. Biomed. Eng.*, vol. 62, no. 1, pp. 4-20, 2015.

[3] S. Haberl, D. Miklavcic, G. Sersa, W. Frey, and B. Rubinsky, "Cell membrane electroporation-part 2: The applications," *IEEE Electr. Insul. Mag.,* vol. 29, no. 1, pp. 29-37, 2013.

[4] K. H. Schoenbach, F. E. Peterkin, R. W. Alden, and S. J. Beebe, "The effect of pulsed electric fields on biological cells: Experiments and applications," *IEEE Trans. Plasma Sci.,* vol. 25, no. 2, pp. 284-292, 1997.

[5] H. Sarnago, O. Lucia, A. Naval, J. M. Burdio, Q. Castellvi, and A. Ivorra, "A versatile multilevel converter platform for cancer treatment using irreversible electroporation," *IEEE Journal. Emerg. Select. Topics in Power Electronics,* vol. 4, no. 1, pp. 236-242, 2016.

[6] K. H. Schoenbach, R. P. Joshi, R. H. Stark, F. C. Dobbs, and S. J. Beebe, "Bacterial decontamination of liquids with pulsed electric fields," *IEEE Trans. Dielect. Elect. Insulation,* vol. 7, no. 5, pp. 637-645, 2000.

[7] M. Rebersek and D. Miklavcic, "Advantages and disadvantages of different concepts of electroporation pulse generation," *Automatika–Journal for Control, Measurement, Electronics, Computing and Communications,* vol. 52, no. 1, pp. 12-19, 2011.

[8] M. A. Elgenedy, A. Darwish, S. Ahmed, and B. W. Williams, "A transition arm modular multilevel universal pulse-waveform generator for electroporation applications," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 8979-8991, 2017.

[9] M. A. Elgenedy, A. Darwish, S. Ahmed, and B. W. Williams, "A modular multilevel generic pulse-waveform generator for pulsed electric field applications," *IEEE Trans. Plasma Sci.,* vol. 45, no. 9, pp. 2527-2535, 2017.

[10] I. Abdelsalam, M. A. Elgenedy, S. Ahmed, and B. W. Williams, "Full-bridge modular multilevel submodule-based high-voltage bipolar pulse generator with low-voltage dc, input for pulsed electric field applications," *IEEE Trans. Plasma Sci.,* vol. 45, no. 10, pp. 2857-2864, 2017.

[11] H. Bluhm, *Pulsed power: Principles and applications*: Berlin. Springer, 2006.

[12] A. Sheikholeslami and J. Adabi, "High-voltage pulsed power supply to generate wide pulses combined with narrow pulses," *IEEE Trans. Plasma Sci.,* vol. 42, no. 7, pp. 1894-1901, Jul. 2014.

[13] J. Clementson, K. Rahbarnia, O. Grulke, and T. Klinger, "Design of a, b, and c pulse forming networks using the vinpfn application," *IEEE Trans. Power Electron.,* vol. 29, no. 11, pp. 5673-5679, 2014.

[14] L. M. Redondo and J. F. Silva, "Flyback versus forward switching power supply topologies for unipolar pulsed-power applications," *IEEE Trans. Plasma Sci.,* vol. 37, no. 1, pp. 171-178, Jan. 2009.

[15] S. Zabihi, F. Zare, G. Ledwich, A. Ghosh, and H. Akiyama, "A novel high-voltage pulsed-power supply based on low-voltage switch-capacitor units," *IEEE Trans. Plasma Sci.,* vol. 38, no. 10, pp. 2877-2887, Oct. 2010.

[16] A. Elserougi, A. M. Massoud, and S. Ahmed, "A boost-inverter-based bipolar high-voltage pulse generator," *IEEE Trans. Power Electron.,* vol. 32, no. 4, pp. 2846-2855, 2017.

[17] A. Elserougi, S. Ahmed, and A. Massoud, "A boost converter-based ringing circuit with high-voltage gain for unipolar pulse generation," *IEEE Trans. Dielectr. Electr. Insul.,* vol. 23, no. 4, pp. 2088-2094, 2016.

[18] L. M. Redondo, "A dc voltage-multiplier circuit working as a high-voltage pulse generator," *IEEE Trans. Plasma Sci.,* vol. 38, no. 10, pp. 2725-2729, 2010.

[19] A. Elserougi, A. M. Massoud, A. M. Ibrahim, and S. Ahmed, "A high voltage pulse-generator based on dc-to-dc converters and capacitor-diode voltage multipliers for water treatment applications," *IEEE Trans. Dielectr. Electr. Insul.,* vol. 22, no. 6, pp. 3290-3298, 2015.

[20] M. Rezanejad, A. Sheikholeslami, and J. Adabi, "Modular switched capacitor voltage multiplier topology for pulsed power supply," *IEEE Trans. Dielect. Elect. Insulation,* vol. 21, no. 2, pp. 635-643, Apr. 2014.

[21] M. R. Delshad, M. Rezanejad, and A. Sheikholeslami, "A new modular bipolar high-voltage pulse generator," *IEEE Trans. Ind. Electron.,* vol. 64, no. 2, pp. 1195-1203, 2017.

[22] L. M. Redondo, J. F. Silva, P. Tavares, and E. Margato, "High-voltage high-frequency marx-bank type pulse generator using integrated power semiconductor half-bridges," in *2005 European Conference on Power Electronics and Applications*, 2005, pp. 8 pp.-P.8.

[23] C. Yao, X. Zhang, F. Guo, S. Dong, Y. Mi, and C. Sun, "FPGA-controlled all-solid-state nanosecond pulse generator for biological applications," *IEEE Trans. Plasma Sci.,* vol. 40, no. 10, pp. 2366-2372, 2012.

[24] L. M. Redondo, "New four-switches bipolar solid-state marx generator," in *2013 19th IEEE Pulsed Power Conference (PPC)*, 2013, pp. 1-5.

[25] H. Canacsinh, L. M. Redondo, and J. F. Silva, "Marx-type solid-state bipolar modulator topologies: Performance comparison," *IEEE Trans. Plasma Sci.,* vol. 40, no. 10, pp. 2603-2610, 2012.

[26] T. Sakamoto, A. Nami, M. Akiyama, and H. Akiyama, "A repetitive solid state marx-type pulsed power generator using multistage switch-capacitor cells," *IEEE Trans. Plasma Sci.,* vol. 40, no. 10, pp. 2316-2321, 2012.

[27] H. Canacsinh, J. F. Silva, and L. M. Redondo, "Dual resonant voltage droop compensation for bipolar solid-state marx generator topologies," *IEEE Trans. Plasma Sci.,* pp. 1-7, 2018.

[28] L. Lamy Rocha, J. F. Silva, and L. M. Redondo, "Multilevel high-voltage pulse generation based on a new modular solid-state switch," *IEEE Trans. Plasma Sci.,* vol. 42, no. 10, pp. 2956-2961, Oct. 2014.

[29] L. L. Rocha, J. F. Silva, and L. M. Redondo, "Seven-level unipolar/bipolar pulsed power generator," *IEEE Trans. Plasma Sci.,* vol. 44, no. 10, pp. 2060-2064, 2016.

[30] A. A. Elserougi, A. M. Massoud, and S. Ahmed, "Modular multilevel converter-based bipolar high-voltage pulse generator with sensorless capacitor voltage balancing technique," *IEEE Trans. Plasma Sci.,* vol. 44, no. 7, pp. 1187-1194, 2016.

[31] M. A. Elgenedy, A. Darwish, S. Ahmed, and B. W. Williams, "A modular multilevel-based high-voltage pulse generator for water disinfection applications," *IEEE Trans. Plasma Sci.,* vol. 44, no. 11, pp. 2893-2900, 2016.

[32] A. A. Elserougi, M. Faiter, A. M. Massoud, and S. Ahmed, "A transformer-less bipolar/unipolar high-voltage pulse generator with low-voltage components for water treatment applications," *IEEE Trans. Ind. Applicat.,* vol. 53, no. 3, pp. 2307-23019, 2017.

[33] A. A. Elserougi, A. M. Massoud, and S. Ahmed, "A modular high-voltage pulse-generator with sequential charging for water treatment applications," *IEEE Trans. Ind. Electron.,* vol. 63, no. 12, pp. 7898-7907, 2016.

[34] A. A. Elserougi, I. Abdelsalam, A. M. Massoud, and S. Ahmed, "A full-bridge submodule-based modular unipolar/bipolar high-voltage pulse generator with sequential charging of capacitors," *IEEE Trans. Plasma Sci.,* vol. 45, no. 1, pp. 91-99, 2017.

[35] A. Darwish, M. A. Elgenedy, S. Finney, B. Williams, and J. R. McDonald, "A step-up modular high-voltage pulse generator based on isolated input-parallel/output-series voltage-boosting modules and modular multilevel sub-modules," *IEEE Trans. Ind. Electron.,* vol. 66, no. 3, pp. 2207-2216, 2019.

[36] M. A. Elgenedy, A. M. Massoud, S. Ahmed, and B. W. Williams, "A high-gain, high-voltage pulse generator using sequentially charged modular multilevel converter submodules, for water disinfection applications," *IEEE Journal. Emerg. Select. Topics in Power Electronics,* vol. 6, no. 3, pp. 1394-1406, 2018.

[37] M. A. Elgenedy, A. Darwish, S. Ahmed, B. W. Williams, and J. R. McDonald, "High-voltage pulse generator based on sequentially charged MMC-SMs operating in a voltage-boost mode", *IET Power Electronics,* 2018, DOI: 10.1049/iet-pel.2018.5438.

[38] M. A. Elgenedy, A. S. Abdel-Khalik, A. A. Elserougi, S. Ahmed and A. Massoud, "A Current-Source-Converter-Based PMSG Wind Energy Conversion System: Simulation Study," *in Proc.15th International Middle East Power System Conference (MEPCON)*, Alexandria, Dec. 2012.

[39] M. A. Elgenedy, A. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "Indirect field oriented control of five-phase induction motor based on SPWM CSI," *in Proc. ICEM*, 2014, pp. 2101–2106.

[40] T.-F. Wu, S.-Y. Tseng, and J.-C. Hung, "Generation of pulsed electric fields for processing microbes," *IEEE Trans. Plasma Sci.,* vol. 32, no. 4, pp. 1551-1562, 2004.

[41] M. A. Elgenedy, A. M. Massoud, and S. Ahmed, "Energy in smart grid: Strategies and technologies for efficiency enhancement," *in Proc. 1st Workshop Smart Grid Renew Energy (SGRE)*, Mar. 2015, pp. 1–6.

[42] B. W. Williams, *Power Electronics: Devices, Drivers, Applications, and Passive Components*. London, U.K.: Macmillan, 1992.