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***Abstract*—In this paper, a new strategy for voltage balancing of distinct dc buses in cascaded H-bridge rectifiers is presented. This method ensures that the dc bus capacitor voltages converge to the reference value, even when the loads attached to them are extracting different amounts of power. The proposed method can be used for an arbitrary number of series H-bridges, different voltage levels, and different power levels in unidirectional or bidirectional rectifiers. To reduce the current harmonics and distortion, the input current is programmed to be sinusoidal and in phase with the input voltage; however, it is possible to adjust the input power factor to control both the active and reactive powers. In the proposed approach, both the low frequency (stepped modulation) and high frequency [pulse-width modulation (PWM)] switching methods are utilized to improve the performance of the rectifier. Using theoretical analysis, the acceptable load power limits for a rectifier with N-H-bridge cells are derived. The validity of the proposed method is verified by simulation and experimental results.**

***Index Terms*—Active rectifier, cascaded H-bridge, multilevel converter, power-factor correction, voltage balancing.**

I. Introduction

With THE advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices [1], [2]. The multilevel topologies are divided into three major categories: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) converters. Among them, the CHB topology is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels. Additionally, due to its modular structure, the hardware implementation is rather simple and maintenance operation easier than alternative multilevel converters. The CHB converters can be used as inverters in ac motor drives, high power conditioning and active power filters [3]–[5]. They also can be utilized as active front-ends or pulse-width modulation (PWM) rectifiers. This kind of application has not been thoroughly investigated yet [6], [7].

The major drawback of the CHB converter, working as a voltage source inverter, is the need for isolated power supplies. However, when it is used as an active rectifier, the topology is even more attractive because of the available distinct dc links feeding separate loads [8]. In the rectification mode, the CHB converter aims to establish N equal dc voltages across the capacitors. This can become difficult if the loads attached to the cells are not equal, or the series H-bridges have slightly different characteristics. Thus, a variety of methods have been proposed to maintain the voltage balancing across the capacitors [7]–[18].

In [9], a low frequency predictive current control for a single-phase CHB rectifier has been proposed. It demonstrates good controller performance in terms of ac current waveform quality, power factor correction and reduced switching frequency. But, it does not provide adequate control strategy to avoid voltage imbalances that could appear across the capacitors when the H-bridge cells are slightly different. In [10], dc voltage balancing control method, based on low frequency modulation techniques, has been proposed. The proposed method, however, does not provide full current control and power factor correction. A low frequency selective harmonic-elimination PWM scheme has been presented in [11] to control energy flow through the CHB topology. Control of power flow in this method requires decoupled control of the converter cells. The balancing scheme involves the use of a proportional-integral (PI) controller at each cell to regulate power flow into cell.

In [12]–[16], dc bus voltage balancing methods have been proposed for single-phase static compensator (STATCOM) devices that are based on the CHB multilevel topology. They achieve voltage balancing while the reactive power is delivered to the ac power line. But, these methods are not applicable in CHB rectifiers. In [7], [8], and [17], balancing of capacitor voltages and power factor correction have been realized for a rectifier with two series H-bridges, while the extension of theses methods to a higher number of series H-bridges is not straightforward. In [18], an energy-based approach has been applied to the control of an N-H-bridge active rectifier. The proposed approach is based on the full decoupling of the H-bridges via the proper design of a passivity-based controller for each cell.

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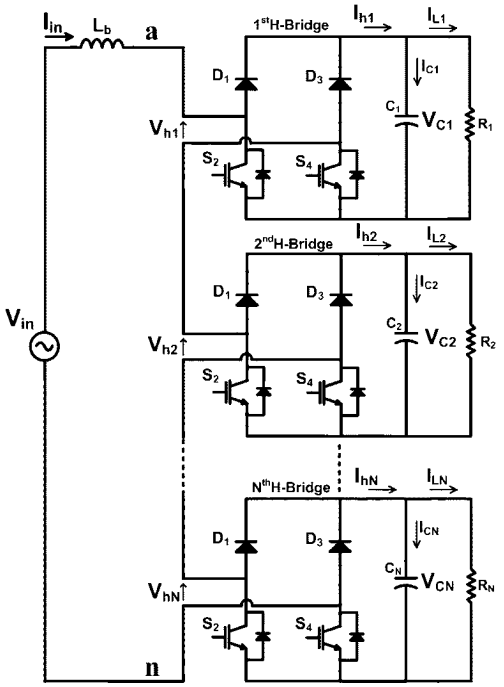

Fig. 1. Unidirectional CHB rectifier with N-H-bridge cells.

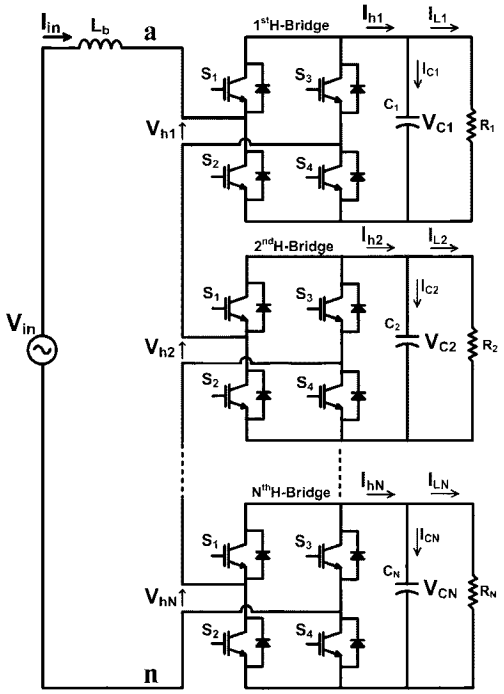

Fig. 2. Bidirectional CHB rectifier with N-H-bridge cells.

In this paper, a simple control method is presented to maintain the voltage balancing across the capacitors in a CHB rectifier. The proposed controller consists of one analog and one digital control unit. The analog controller programs the input current to be sinusoidal and in phase with the input voltage. It can also adjust the input power factor to control both the active and reactive powers. The digital controller provides the voltage balancing across the capacitors, even if the loads connected to the cells are not equal or the cells do not match perfectly. Using analytical approach, the validity regions and the load power limits for a CHB converter with N-H-bridges are derived. The semiconductor loss analysis is also presented to estimate the switching and conduction losses in the proposed approach.

II. System Configuration

A. Configuration of the Rectifier

The CHB rectifier is the best choice for working in high-voltage and high-power applications because of its extreme modularity, simple physical layout, and reduced losses. Figs. 1 and 2, respectively, show the configurations of single-phase unidirectional and bidirectional CHB rectifiers. The first structure may be used for feeding the variable-speed drive in applications such as variable speed fans, pumps, and compressors [19]. The bidirectional structure may be used in front-end applications, traction, high power electric drives, and electronic transformers addressed in [6], [7], and [20].

This paper focuses only on the single-phase ac/dc rectifiers. The results, however, can be easily extended to three-phase structures. Furthermore, the unidirectional rectifier can be realized from bidirectional rectifier by turning off the upper switches of the H-bridge cells. Therefore, only the bidirectional rectifier is analyzed and its results used for the unidirectional rectifier as well.

The rectifier in Fig. 2 has N-series-connected H-bridge cells. Each H-bridge consists of four power switches (with anti-parallel diodes) and a dc bus capacitor. Each capacitor feeds its own load and the loads may be passive or active converter cells. In Fig. 2, the ac terminal voltage of the rectifier, $V_{\rm an}$, can be written as follows:

$$V_{\rm an} = V_{h1} + V_{h2} + \cdots + V_{hN} \tag{1}$$

$$V_{hi} = h_i \cdot V_{Ci}, \quad i = 1, 2, \ldots, N \tag{2}$$

where V_{hi}, V_{Ci}, and h_i are the ac terminal voltage, the capacitor voltage, and the switching function of the ith H-bridge (or cell), respectively. Assuming $V_{C1} = \cdots = V_{CN} = V_C$, where V_C is the reference voltage of dc buses, each cell can generate three voltage levels: $+V_C$, $-V_C$, and zero on the ac side. So, using N-H-bridge cells a maximum of $2N+1$ different voltage levels are obtained to synthesize the ac terminal voltage $V_{\rm an}$.

In Fig. 2, applying Kirshhoff's Voltage Law (KVL) at the input voltage loop yields

$$V_{\rm in} = V_{\rm an} + L_b \frac{dI_{\rm in}}{dt} \tag{3}$$

where $V_{\rm in}$ is the input voltage, $I_{\rm in}$ the input current, and L_b the input inductance, the last used to shape the input current. Applying Kirshhoff's Current Law (KCL) for each cell leads to

$$I_{hi} = h_i I_{\rm in} = I_{Ci} + I_{Li}, \quad i = 1, \ldots, N \tag{4}$$

where I_{hi} is the current of ith H-bridge and is a function of the input current. $I_{\rm Ci}$ is the capacitor current and $I_{\rm Li}$ the load current. Equations (1)–(4) describe a linear time varying (LTV)

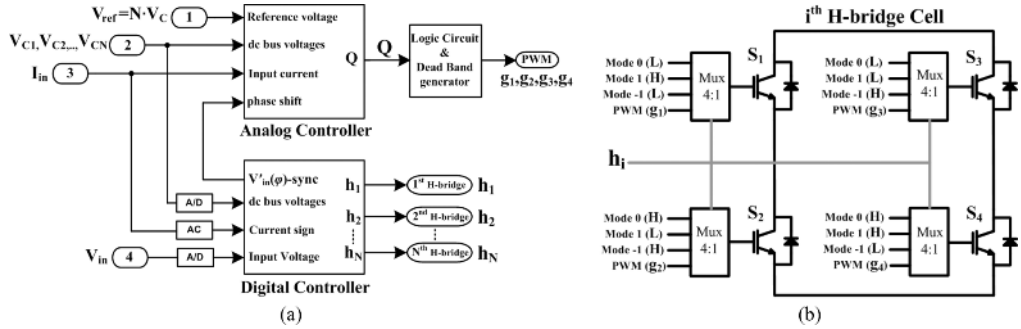

Fig. 3. (a) Basic block diagram of the proposed controller. (b) Drive circuit of an arbitrary H-bridge cell.

TABLE I
TRUTH TABLE OF GATE SIGNALS IN PWM MODE

V =sign (V_{in})	Q	g_1	g_2	g_3	g_4
0	0	0	1	0	1
0	1	0	1	1	0
1	0	1	0	0	1
1	1	0	1	0	1

system with one input ($V_{\rm in}$) and $N+1$ states (V_{C1} to $V_{\rm CN}$ and $I_{\rm in}$). The controller should determine the switching functions, h_1 to h_N, to achieve the control goals.

B. Configuration of Controller

The basic block diagram of the controller is shown in Fig. 3(a). This block consists of analog and digital controllers. The analog controller generates the PWM signal, Q, and the digital controller determines the appropriate switching functions h_1 to h_N. The necessary feedback signals for the controller are the dc bus voltages V_{C1} to V_{CN}, the input voltage $V_{\rm in}$, and the input current $I_{\rm in}$. The voltage signals are sensed using the isolation amplifiers and conditioned to proper magnitude to feed the controllers. The input current is measured using a Hall-effect sensor, conditioned and used as a feedback in the current control loop. The digital controller also generates a synchronized square-wave signal [$V'_{\rm in}(\varphi)$ in Fig. 3(a)] to adjust the input power factor.

Each switching function h_i $(i = 1, \ldots, N)$ corresponds to four operating modes: "0," "+1," "−1," and PWM. The switching functions are determined by the digital controller and applied to the H-bridge cells. Then, the corresponding operating modes are selected by 4:1 multiplexers [see Fig. 3(b)]. The operating mode "0" corresponds to the conduction of bottom switches (S_2, S_4). In modes "+1," and "−1," the diagonal switches (S_1, S_4) and (S_2, S_3) are turned on, respectively. Mode "+1" is used if the input voltage is positive; otherwise, mode "−1" is used. In the PWM mode, the gate signals, g_1 to g_4, drive the corresponding cell. These signals are obtained from Q, output of analog controller, according to Table I.

In Table I, V is the sign of input voltage (V is 1 if the input voltage is positive; otherwise it is 0). From Table I, one can see that the PWM gate signals are generated by the following logic circuits:

$$g_1 = V\overline{Q}, \quad g_2 = \overline{V\overline{Q}} \tag{5}$$

$$g_3 = \overline{V}Q, \quad g_4 = \overline{\overline{V}Q}. \tag{6}$$

III. PRINCIPLE OF OPERATION

The main challenges associated with the CHB rectifier control are: 1) shaping the input current and controlling the input power factor and 2) maintaining voltage balance across the dc bus capacitors. The first goal will be achieved by the analog controller and the second one by the digital controller, as explained in the following paragraphs.

A. Analog Controller

The functional block diagram of the analog controller is shown in Fig. 4. This controller is intended to shape the input current and regulate the total voltage of dc buses. The controller has two control loops: the inner current loop and the outer voltage loop. The voltage loop contains a PI controller to regulate the total voltage of dc buses to the reference value $N \cdot V_C$. In the classical methods, the output of PI controller is multiplied by the sample of input voltage to generate a sinusoidal reference current, $I^*_{\rm in}$. In this paper, the digital controller generates a square-wave synchronized signal, $V'_{\rm in}$, from the input voltage. The sync signal has the same frequency as the input voltage and its phase is adjusted by the digital controller. The square-wave signal is filtered by a forth-order Butterworth filter (Sallen-Key topology) and the output is multiplied by the output of PI controller. Using this method, a pure sinusoidal reference is generated even in the polluted environments with noise and harmonics. Additionally, the input power factor and the reactive power flow are controlled, and the gain of voltage loop becomes independent from the input voltage variations.

After generating the reference current $I^*_{\rm in}$, the inner current loop programs the input current to follow the reference waveform. Some of the reported current mode control techniques are peak-current mode, average-current mode, and hysteresis-current mode controls [21]. In this paper, the hysteresis-current control is utilized, which has the advantages of simple analog implementation and fast dynamics, but other fast dynamic current control methods can also be used.

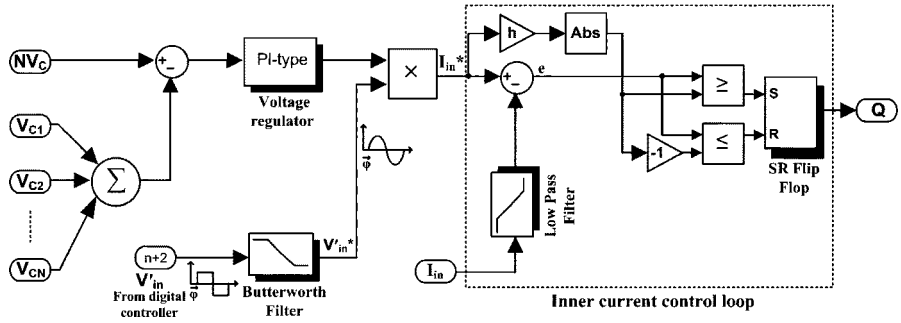

Fig. 4. Details of the analog controller employed in Fig. 3.

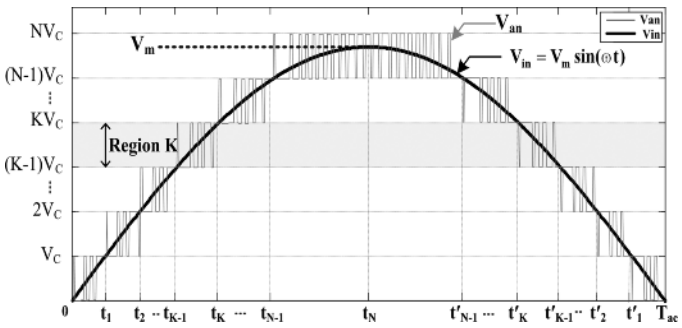

Fig. 5. Definition of voltage regions for $K = 1, \ldots, N$.

In hysteresis controller, the lower limit of current $I_{l,\mathrm{ref}}$ and the upper limit of current $I_{u,\mathrm{ref}}$ are defined as follows:

$$I_{l,\mathrm{ref}} = I^*_{\mathrm{in}} - h\,|I^*_{\mathrm{in}}|\,, \quad I_{u,\mathrm{ref}} = I^*_{\mathrm{in}} + h\,|I^*_{\mathrm{in}}| \tag{7}$$

where, h represents the hysteresis band. According to this control method, Q becomes 1 when the input current goes below the lower limit and it becomes 0 when the input current goes above the upper limit.

B. Definition of Voltage Regions

To take advantage of both low frequency (stepped modulation) and high frequency (PWM) modulation techniques, hybrid modulation method shown in Fig. 5 is employed. In this method, the input voltageV_{in} is divided into equal sections with the scale of V_C (V_C is the dc bus voltage reference and each cell tolerates no more than V_C). Now, the voltage region K is defined as follows:

$$(K-1)\cdot V_C < |V_{\mathrm{in}}| < K\cdot V_C, \quad K = 1, \ldots, N. \tag{8}$$

Region K is where the magnitude of input voltage,$|V_{\mathrm{in}}|$, lies between $(K-1)V_{\mathrm{C}}$ and KV_C. It is worth noting that the minimum number of cells to synthesize the multilevel waveform, V_{an}, is equal to the closest integer greater than (V_m/V_C), where V_m is the peak input voltage. In Fig. 5, T_{ac} is the mains half-cycle, t_K and t'_K $(K = 1, \ldots, N-1)$ corresponds to the change of voltage region, where $V_{\mathrm{in}} = KV_C$, and t_N is equal to $T_{\mathrm{ac}}/2$. The voltage region K can be represented by the time intervals (t_{K-1}, t_K) and (t'_K, t'_{K-1}) as well. Assuming $V_{\mathrm{in}} = V_m \sin(\omega t)$, t_K and t'_K are derived as follows:

$$t_K = \frac{1}{\omega} sin^{-1}\left(\frac{KV_C}{V_m}\right) \; or \; sin(\omega t_K) = \frac{KV_C}{V_m} \tag{9}$$

$$t'_K = \pi/\omega - t_K, \quad \omega = 2\pi f_{\mathrm{line}} \quad \text{for } K = 1, \ldots, N. \tag{10}$$

The following benefits can be achieved by utilizing the hybrid modulation technique:

- considerable reduction in the size and volume of the input inductance L_b; because the input inductance tolerates no more than V_C;
- reduction in the THD and EMI at the input side;
- low switching loss; because at each time only one cell works in high frequency switching mode.

To determine the duty cycle of the PWM signal, the following method is used. Assuming that the operating voltage region is K and the amplitude of input voltage is constant during the switching period, the change of inductor current Δi can be approximated as follows:

$$\begin{cases} \Delta i^+ = \frac{(|V_m \sin(\omega t)| - (K-1)V_C)\cdot t_{\mathrm{on}}}{L_b}, & \text{if } V_{\mathrm{in}} > 0 \\ \Delta i^- = -\frac{(|V_m \sin(\omega t)| - (K-1)V_C)\cdot t_{\mathrm{on}}}{L_b}, & \text{if } V_{\mathrm{in}} < 0 \end{cases} \tag{11}$$

where t_{on} is the duration of time during which the power switches (S_2, S_4) are on. During t_{off}, the diagonal switches (S_1, S_4) or (S_2, S_3) are on and the change of inductor current is calculated as follows:

$$\begin{cases} \Delta i^- = \frac{(|V_m \sin(\omega t)| - KV_C)\cdot t_{\mathrm{off}}}{L_b}, & \text{if } V_{\mathrm{in}} > 0 \\ \Delta i^+ = -\frac{(|V_m \sin(\omega t)| - KV_C)\cdot t_{\mathrm{off}}}{L_b}, & \text{if } V_{\mathrm{in}} < 0. \end{cases} \tag{12}$$

Using (11) and (12), and considering the approximation of $\Delta i^+ \approx -\Delta i^-$, one can conclude that

$$d_K(t) = \frac{t_{\mathrm{on}}}{T_S} = \frac{t_{\mathrm{on}}}{t_{\mathrm{on}} + t_{\mathrm{off}}} = K - \frac{|V_m \sin(\omega t)|}{V_C} \tag{13}$$

where T_S is the switching period, and d_K $(K = 1, \ldots, N)$ is the duty cycle of PWM signal which depends on the value of voltage region K.

C. Proposed Control Algorithm

The digital controller performs the control algorithm to maintain voltage balance across the capacitors, while the analog con-

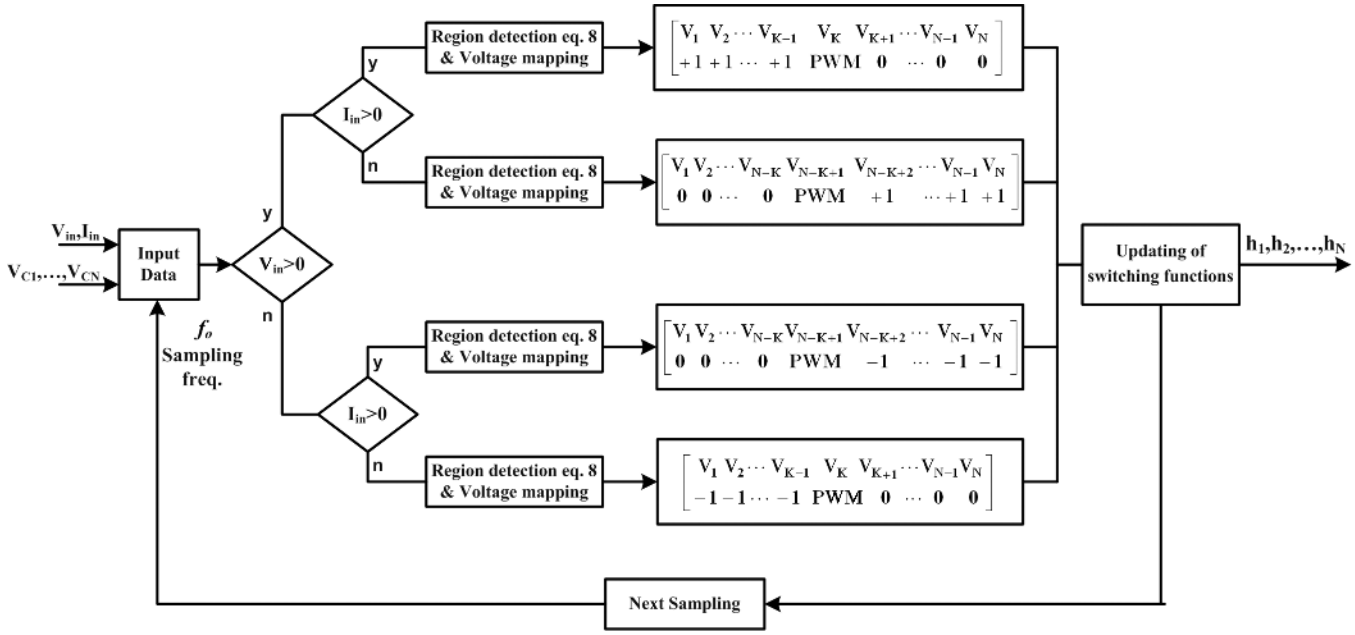

Fig. 6. Flowchart of the control algorithm, the vector $(V_1, V_2, \ldots, V_N)$ is a mapping for the voltage of dc buses, sorted in ascending order, i.e., $V_1 < V_2 < \cdots < V_N$.

troller regulates the sum of dc bus voltages to $N \cdot V_C$. The proposed control rules, defined hereafter, aim to synthesize the waveform shown in Fig. 5 and to maintain voltage balancing.

1) If $V_{\rm in} > 0$, $I_{\rm in} > 0$, and voltage region is K, then $(K-1)$ cells with the lowest dc bus voltage are chosen to be charged in mode "+1," the Kth cell in PWM mode, and the rest in mode "0".
2) If $V_{\rm in} > 0$, $I_{\rm in} < 0$, and voltage region is K, then $(K-1)$ cells with the highest dc bus voltage are chosen to be discharged in mode "+1," the Kth cell in PWM mode, and the rest in mode "0".
3) If $V_{\rm in} < 0$, $I_{\rm in} > 0$, and voltage region is K, then $(K-1)$ cells with the highest dc bus voltage are chosen to be discharged in mode "−1," the Kth cell in PWM mode, and the rest in mode "0".
4) If $V_{\rm in} < 0$, $I_{\rm in} < 0$, and voltage region is K, then $(K-1)$ cells with the lowest dc bus voltage are chosen to be charged in mode "−1," the Kth cell in PWM mode, and the rest in mode "0".

To perform the previous rules, the digital controller employs the flowchart shown in Fig. 6. In the flowchart, the vector $(V_1, V_2, \ldots, V_N)$ is a mapping for the dc bus voltages, sorted in the ascending order. The value of V_i: "0," "+1," "−1," or PWM, represents the cell operating mode.

In Fig. 6, the digital controller takes voltage and current samples with the sampling frequency f_o. Then, the region of input voltage K is updated according to (8), the control algorithm is performed, and the appropriate switching functions h_1 to h_N are determined. The switching functions are applied to the H-bridge cells and the corresponding operating modes are selected by the multiplexers. This procedure is repeated in the succeeding sampling periods. As a result, the voltage of each capacitor is regulated by controlling the power flow to the capacitors. For example, the cell feeding a heavy load will operate in the charging mode, most of the time, and in the PWM mode when K is small. But, the cell supplying a light load will operate mostly in "0" mode, and when K is close to N, in PWM mode. The operational behavior of other cells will be between these two extremes (see Fig. 12).

The following remarks about this method are worth noting.

- In the proposed controller, there are two modulation mechanisms. One is carried out by the analog controller, termed as PWM mode, and the other performed by the digital controller, termed as voltage balancing algorithm.
- The PWM mode is used to control the input current and to regulate the sum of dc bus voltages to the reference value, i.e., $\Sigma V_{\rm Ci} = N \cdot V_C$. This condition, besides the voltage balancing condition, leads to $V_{\rm Ci} = V_C$ for $i = 1, \ldots, N$.
- The voltage balancing algorithm is repeated with the sampling frequency f_o.
- During the sampling period $T_o = 1/f_o$, the switching functions h_1 to h_N do not change.
- The switching period T_S (or PWM period) is lower than the sampling period T_o, and the sampling period is lower than $(t_K - t_{K-1})$; on the other hand, during the time interval (t_{K-1}, t_K), the switching functions (or operating modes) may change due to change in dc bus voltages.

As an example, it is assumed that the number of H-bridge cells is $N = 3$, voltage region is $K = 2$, $V_{\rm in} > 0$, $I_{\rm in} > 0$, and the sort of dc bus voltages is $V_{C1} \le V_{C3} \le V_{C2}$ at t_1. According to the control rules, the switching functions are determined as $h_1 =$ "+1," $h_2 =$ "0", and $h_3 = \rm PWM$. For this situation, the configuration of power switches is shown in Fig. 7(a) and the cells currents are shown in Fig. 7(b).

In Fig. 7(a), it can be seen that the first cell is completely on and its current is equal to the input current, i.e., $I_{h1} = I_{\rm in}$. The

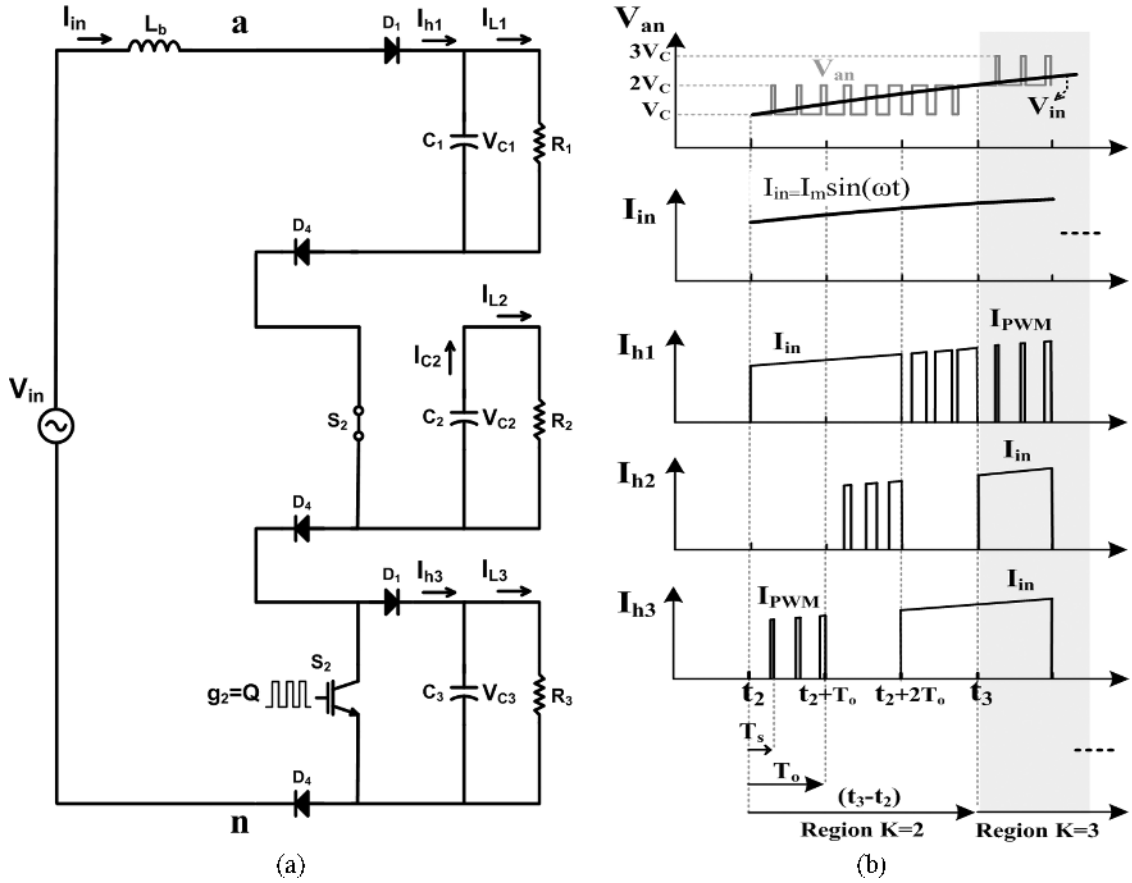

Fig. 7. (a) Configuration of power cells when $N = 3$, $K = 2$, and the sort of dc bus voltages is $V_{C1} \leq V_{C3} \leq V_{C2}$ at $t = t_1$ (this configuration is valid for $t_1 < t < t_1 + T_o$). (b) Illustration of cells currents for four sampling periods: $V_{C1} \leq V_{C3} \leq V_{C2}$ at $t = t_1$, $V_{C1} \leq V_{C2} \leq V_{C3}$ at $t = t_1 + T_o$, $V_{C3} \leq V_{C1} \leq V_{C2}$ at $t = t_1 + 2T_o$, and $V_{C3} \leq V_{C2} \leq V_{C1}$ at $t = t_2$.

second cell does not participate in the modulation and its current is zero. The third cell works in PWM mode and its current is a PWM function of the input current ($I_{h3} = I_{\rm PWM}$). The third cell is charged but not as much as the first one. This state lasts $T_o = 1/f_o$ seconds and again a new update occurs.

In Fig. 7(b), the illustration of cells currents are extended for the next three sampling periods, where the sorts of dc buses are $V_{C1} \leq V_{C2} \leq V_{C3}$ at $t_1 + T_o$, $V_{C3} \leq V_{C1} \leq V_{C2}$ at $t_1 + 2T_o$, and $V_{C3} \leq V_{C2} \leq V_{C1}$ at t_2. At t_2 the voltage region changes to $K = 3$, and hereafter, two cells are selected to work in mode "+1" and one in PWM.

IV. Establishing the Controller Validity Regions

In this section, the load power limits and the validity regions for the proposed control algorithm are derived. The following assumptions are used in the analysis:

1) all converter components are ideal;
2) output capacitors are large enough to be treated as constant voltage sources during switching periods;
3) The input current is sinusoidal, i.e., $I_{\rm in} = I_m \sin(\omega t + \varphi)$ (due to presence of the analog controller).

To simplify the representation of equations, the average value of variable "X" over the time period "y" is hereafter denoted by "$\langle X \rangle_y$" symbol. Also, the subscript "i" is used to represent the cell number.

The first assumption implies that the CHB rectifier is a lossless converter and the average input power over a half-cycle $\langle P_{\rm in} \rangle_{\rm Tac}$ is equal to the total power of distinct loads, i.e.,

$$\langle P_{\rm in} \rangle_{T_{\rm ac}} = \frac{1}{2} V_m I_m \cos(\varphi) = \sum_{i=1}^{N} P_i \tag{14}$$

where I_m is the peak input current, V_m the peak input voltage, $\cos(\varphi)$ the input power factor, and P_i the ith H-bridge load. From (4), the cell current can be rewritten as follows:

$$I_{\rm hi} = h_i I_{\rm in} = \begin{cases} I_{\rm in} \cdot V, & \text{if } h_i = \pm 1 \\ I_{\rm PWM} \cdot V, & \text{if } h_i = \text{PWM} \\ 0, & \text{if } h_i = 0 \end{cases} \tag{15}$$

where $I_{\rm hi}$ is the ith cell current, V the sign of input voltage, and $I_{\rm PWM}$ the PWM current which is expressed as follows:

$$I_{\rm PWM} = \begin{cases} 0, & t_x < t \leq t_x + d_K T_s \\ I_{\rm in}, & t_x + d_K T_s < t \leq t_x + T_s \end{cases} \tag{16}$$

where t_x is an arbitrary time. Equations (15) and (16) show that the cell current $I_{\rm hi}$ $(i = 1, \ldots, N)$ contains a dc term, a low frequency harmonic $(2f_{\rm line} = 1/T_{\rm ac})$, and a high frequency switching ripple. At steady state, the low and high frequency components flow into the ith capacitor and the dc term (cell average current over a half-cycle, i.e., $\langle I_{\rm hi} \rangle_{\rm Tac}$) is equal to the ith load current $I_{\rm Li} = P_i / V_{\rm Ci}$.

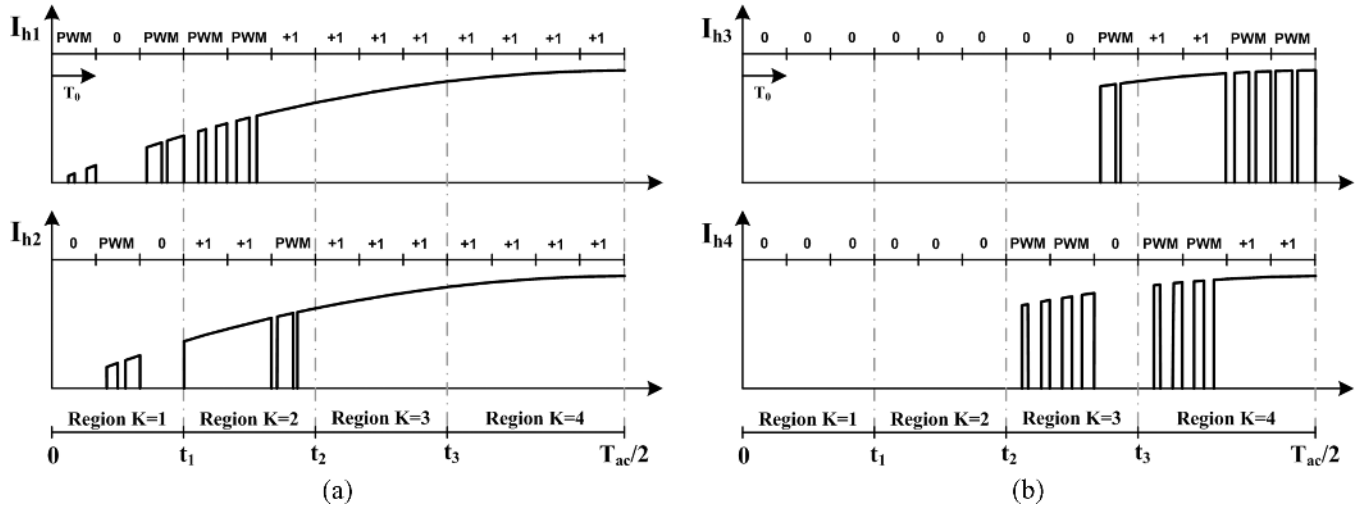

Fig. 8. Worst case of charging when $N = 4$ and $M = 2$: (a) current waveforms of the cells attached to the heavy loads and (b) current waveforms of the cells attached to the light load.

As the favored dc bus voltage is V_C, the desired load current would be $I_{\rm Li} = P_i/V_C$. Setting the cell average current equal to the desired load current yields

$$\langle I_{\rm hi}\rangle_{T_{\rm ac}} = \frac{P_i}{V_C}. \tag{17}$$

Equation (17) is a sufficient condition for $V_{\rm Ci} = V_C$, where $V_{\rm Ci}$ is the ith cell voltage. The control goal is that all the dc bus voltages, V_{C1} to $V_{\rm CN}$, become equal to V_C. Therefore, (17) should be satisfied for all the cells. In the following section, the load power limits and the boundary conditions that satisfy the previous relation for $i = 1, \ldots, N$, are determined.

A. Unity Power Factor Application

1) Load Power Limits in Steady State: In this part, the acceptable power limits for each dc load, which can still guarantee the voltage balancing, are determined. Let the N loads be divided into M "heavy" loads and N-M "light loads" (M is an arbitrary number between 1 and $N-1$). The goal is to find the maximum power which can be fed to the M-loads when the total power is equal to P_t, i.e., $\Sigma P_i = P_t$, and the input current is in phase with the input voltage. The condition $\Sigma P_i = P_t$ is equivalent to the condition $\Sigma V_{\rm Ci} = N \cdot V_C$ which is satisfied by the analog controller.

In the voltage region K, $(K-1)$ cells must work in mode "+1" (or "−1"), one in PWM and the rest in mode "0" so, the total current fed to all the cells in the region K is as follows:

$$\sum_{i=1}^{N} I_{\rm hi} = (K-1)\cdot|I_{\rm in}| + |I_{\rm PWM}|. \tag{18}$$

According to (18), at the sampling periods of the region K, only K cells have the chance of being charged. So, in the worst case scenario, only the cells attached to the heavy loads are selected to take part in the modulation if $K \le M$, and to be completely on if $K > M$.

As an example, it is assumed that the number of H-bridge cells is $N = 4$ and the cells loads P_1 and P_2 are very heavy $(M = 2)$. One case of charging is shown in Fig. 8. It is observed that in the region $K = 1$, the cells attached to the heavy loads are chosen to work in PWM mode (one cell at each sampling period). Also, in the region $K = 2$, one cell works in mode "+1" and the other in PWM mode. In the regions $K = 3$ and $K = 4$, the first and second cells are completely on, and the cells connected to the light loads are chosen to be charged according to their dc bus voltages. This procedure is repeated with the mains half-cycle period $T_{\rm ac}$.

Equation (18) and the previous discussion imply that the maximum average current fed to the M-loads over a half-cycle is as follows:

$$\langle I_{\max,M}\rangle_{T_{\rm ac}} = \frac{2}{T_{\rm ac}}\left(\sum_{K=1}^{M}(t_K - t_{K-1})\left((K-1)\langle I_{\rm in}\rangle_K + \langle I_{\rm PWM}\rangle_K\right) + M\int_{t_M}^{T_{\rm ac}/2} I_{in}(t)dt\right) \tag{19}$$

where $\langle I_{\max,M}\rangle_{T_{\rm ac}}$ is the upper limit of average current fed to the M-loads over a half-cycle. $(t_K - t_{K-1})$ represents the region K, in time domain. Further, $\langle I_{\rm in}\rangle_K$ and $\langle I_{\rm PWM}\rangle_K$ are the average of $I_{\rm in}$ and $I_{\rm PWM}$ over the region K.

In (19), the sigma term corresponds to the regions that $K \le M$ and the integral term to the regions that $K > M$. By using (16) and considering the fact that $I_{\rm in} = I_m \sin(\omega t)$, the average currents $\langle I_{\rm in}\rangle_K$ and $\langle I_{\rm PWM}\rangle_K$ are obtained, thus

$$\langle I_{\rm in}\rangle_K = \frac{1}{(t_K - t_{K-1})}\int_{t_{K-1}}^{t_K} I_m \sin(\omega t)dt = \frac{I_m}{\omega(t_K - t_{K-1})}\left(\cos(\omega t_{K-1}) - \cos(\omega t_K)\right) \tag{20}$$

$$\langle I_{\rm PWM}\rangle_K \approx -\frac{(K-1)}{2}\langle I_{\rm in}\rangle_K + \frac{V_m I_m}{2V_C} - \frac{I_m}{2\omega(t_K - t_{K-1})}$$

$$\times \cos(\omega t_K), \quad 1 \le K \le N. \tag{21}$$

The derivation for (21) is shown in Appendix I. Substituting (20) and (21) into (19) and simplifying the equation results in

$$\langle I_{\max,M}\rangle_{T_{\rm ac}} = \frac{1}{\pi}\left(\frac{V_m I_m}{V_C}\omega t_M + M \cdot I_m \cos(\omega t_M)\right). \tag{22}$$

Multiplying $\langle I_{\max,M}\rangle_{\rm Tac}$ by V_C gives the maximum power fed to the M-loads

$$P_{\max,M} = \frac{2P_t}{\pi}\left(\omega t_M + M\frac{V_C}{V_m}\cos(\omega t_M)\right) \tag{23}$$

where $P_{\max,M}$ is the maximum power that can be fed to the M-loads over a half-cycle. The cells loads P_1 to P_N must satisfy the limits of (23) for $M = 1, \ldots, N-1$.

Using (23) and (9), the upper limits of the cells loads are obtained as function of the total power. For example, if $N = 5$, $V_C = 600$ V, $V_m = 2694$ V, and $P_t = 30$ kW, the upper limits of the power are calculated as $P_{\max,1} = 8.42$ kW, $P_{\max,2} = 16.43$ kW, $P_{\max,3} = 23.47$ kW, and $P_{\max,4} = 28.72$ kW. It means that the cells loads P_1 to P_4 should satisfy four power limits: $P_1 < P_{\max,1}$, $P_1+P_2 < P_{\max,2}$, $P_1+P_2+P_3 < P_{\max,3}$, and $P_1+P_2+P_3+P_4 < P_{\max,4}$, where $P_4 \le P_3 \le P_2 \le P_1$. If the upper limits are not satisfied, voltage imbalances will appear at the dc bus voltages.

As the total power fed to the N-loads is equal to P_t, the lower limit of power fed to the M-loads is obtained simply from (23) as follows:

$$\langle P_{\min,M}\rangle_{T_{\rm ac}} = P_t - \langle P_{\max,N-M}\rangle_{T_{\rm ac}} \tag{24}$$

where $P_{\min,M}$ is the minimum power that can be fed to the M loads over a half-cycle.

2) Power Limits During Load-Increase: It is assumed that each cell supplies its own load and the loads of M cells increase at $t = t_o$ (M is an arbitrary number between 1 and N). After this change, the analog controller increases the peak input current I_m to inject more active power to the loads. Due to this increase in current, the modulation of the cells feeding constant loads must change, so that their average currents remain constant. In this case, most of the time, the cells attached to the increased loads will operate in the charging mode and the rest in "0" mode. The worst case of the charging occurs when the total power of the unchanged loads P_{t0} becomes equal to the minimum power fed to the (N-M) cells, i.e., $\langle P_{\min,N-M}\rangle_{\rm Tac}$. Therefore, from (14) and (24), it is concluded that

$$P_{t1} = \frac{V_m I_{m1}}{2} = \frac{P_{\rm to}}{\left(1 - \frac{2}{\pi}\left(\omega t_M, + M\frac{V_C}{V_m}\cos(\omega t_M)\right)\right)} \tag{25}$$

where P_{t0} is the total power of the constant loads, P_{t1} the new upper limit of total power, and I_{m1} the new upper limit of the peak input current after the load-increase. If the input current increases beyond this upper limit, the controller will lose the regulation of dc buses. On the other hand, to maintain voltage balancing and stability, the total power of all loads must be less than P_{t1}, and (23) must be satisfied for $M = 1, \ldots, N-1$, in the new condition.

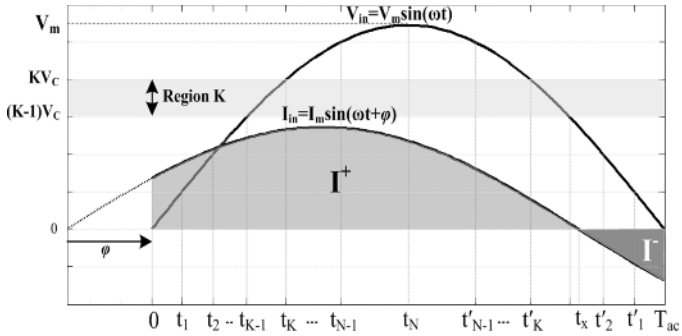

Fig. 9. Calculation of $\langle I_{\rm in}\rangle_K$ and $\langle I_{\rm PWM}\rangle_K$ when the input current leads the voltage by an angle φ.

B. Reactive Power Control Application

In this case, the phase of input current is shifted relative to the input voltage to control both the active and reactive powers. This feature improves the flexibility of the rectifier due to capability of reactive compensation. To correctly calculate the power limits and validity regions, the expressions given for $\langle \rm Iin\rangle_K$ and $\langle I_{\rm PWM}\rangle_K$ in (20) and (21) must be modified.

We consider the scheme shown in Fig. 9, where the input current leads the voltage by an angle φ. Following a similar approach as the one in Section III, the new expressions for $\langle \rm Iin\rangle_K$ and $\langle I_{\rm PWM}\rangle_K$ are derived and shown in (26) and (27)

$$\langle I_{\rm in}\rangle_K = \frac{I_m \cdot (\cos(\omega t_{K-1}+\varphi) - \cos(\omega t_K + \varphi))}{\omega(t_K - t_{K-1})} \tag{26}$$

$$\langle I_{\rm PWM}\rangle_K = -(K-1)\langle I_{\rm in}\rangle_K + \frac{V_m I_m}{2V_C}\cos\varphi - \frac{V_m I_m(sin(2\omega t_K+\varphi) - \sin(2\omega t_{K-1}+\varphi))}{4V_C\omega(t_K - t_{K-1})}. \tag{27}$$

It is to be noted that during computation of the previous equations, t_K and t_{K-1} should be replaced by t'_K and t'_{K-1} [defined in (10)] if the time variable "t" is between $T_{\rm ac}/2$ and $T_{\rm ac}$. When the power factor is not unity, one can find different power limits and validity regions for the controller by using (26) and (27). For example, by solving the following equation, the minimum phase shift is achieved to manage a no-load cell in the bidirectional rectifier:

$$\tan\varphi_{\min} - \varphi_{\min} = \pi - (2\omega t_{N-1} + \sin(2\omega t_{N-1})). \tag{28}$$

In contrast, in unidirectional rectifiers, an additional H-bridge should be used to manage a no-load cell if $(N-1)\cdot V_C < V_m < N \cdot V_C$.

V. Semiconductor Loss Analysis

At an early design stage, knowledge of switching behavior is desirable for the designer to estimate the converter switching losses. In the proposed method, the analytical derivation of the

operating modes for an arbitrary cell is complex and beyond the scope of this paper. However, it is possible to calculate the conduction and switching losses by analytical functions, regardless of the individual cell's behavior.

It is assumed that the input current is positive and in phase with the input voltage. In mode "+1," the input current is conducted by the diagonal diodes, D_1 and D_4, and in mode "0," by the bottom switch S_2 and the diode D_4 [see Fig. 7(a)]. In PWM mode, the current is commutated between S_2 and D_1 with the switching frequency f_S, and with D_4 completely on. Thus, the total semiconductor losses for the N cells can be expressed as follows (in simplified form):

$$\begin{aligned} P_{\text{cond}} = &\frac{2I_m N V_D}{\pi} + \frac{2I_m V_D}{\pi}\sum_{K=1}^{N-1}\cos(\omega t_K) \\ &+ \left[\frac{2I_m}{\pi}\sum_{K=1}^{N-1}\left(V_{\text{CEO}}\left(1-\cos(\omega t_K)\right)\right)\right. \\ &\left. + \frac{r_{CE} I_m^2}{T_{\text{ac}}}\left(t_K - \frac{1}{2\omega}\sin(2\omega t_K)\right)\right] \\ &+ \frac{2V_D}{T_{\text{ac}}}\sum_{K=1}^{N}(t_K - t_{K-1})\langle I_{\text{PWM}}\rangle_K \\ &+ \frac{2}{T_{\text{ac}}}\sum_{K=1}^{N}(t_K - t_{K-1}) V_{CE}\cdot\langle I_{\text{in}} - I_{\text{PWM}}\rangle_K \end{aligned} \quad (29)$$

where V_D is the diode voltage drop, V_{CE} the collector-emitter voltage, V_{CEO} the collector-emitter threshold voltage, r_{CE} the on-state resistance of the switch, and t_K $(K = 1, \ldots, N)$ the instant that the voltage region changes. The first term in (29) determines the conduction losses in D_4 and the second term the conduction losses in D_1 (for all cells). The next expression is related to the conduction losses in S_2 over a half-cycle. The last two terms calculate the conduction losses generated by D_1 and S_2 in PWM mode (V_{CE}, in the last term, can be approximated by $V_{CE} \approx V_{\text{CEO}} + r_{\text{CE}} \cdot I_m(2K-1)V_C/(2V_m)$).

In the proposed method, there are two types of switching losses: the high-frequency switching (PWM) loss and the switching loss due to voltage balancing control. In this paper, a hysteresis current controller has been utilized. To determine the PWM switching loss, the switching frequency is estimated approximately in the hysteresis mode. Using (11), (12), and the approximation of $\Delta i^+ \approx -\Delta i^- \approx 2hI_m\sin(\omega t)$ (sinusoidal-band hysteresis current controller), it is concluded that

$$\begin{aligned} f_S(t) &= \frac{1}{t_{\text{on}} + t_{\text{off}}} \\ &\approx \frac{(V_m\sin(\omega t) - (K-1)V_C)(KV_C - V_m\sin(\omega t))}{2hL_bI_mV_C\cdot\sin(\omega t)} \end{aligned} \quad (30)$$

where $f_S(t)$ is the instantaneous switching frequency, and t_K $(K = 1, \ldots, N)$ is calculated from (9). The average of switching frequency over the region K, i.e., $\langle f_S\rangle_K$, is obtained from (30) as follows:

$$\begin{aligned} \langle f_S\rangle_K &= \frac{1}{(t_K - t_{K-1})}\int_{t_{K-1}}^{t_K} f_S(t)dt \\ &= \frac{1}{2hL_bI_mV_C} \\ &\quad\cdot\left[(2K-1)V_CV_m + \frac{V_m^2}{\omega}\right. \\ &\quad\cdot\frac{(\cos(\omega t_K) - \cos(\omega t_{K-1}))}{(t_K - t_{K-1})} + \frac{K(K-1)V_C^2}{2\omega(t_K - t_{K-1})} \\ &\quad\left.\times\log\left(\frac{(1+\cos(\omega t_K))\cdot((1-\cos(\omega t_{K-1}))}{(1+\cos(\omega t_{K-1}))\cdot((1-\cos(\omega t_K))}\right)\right]. \end{aligned} \quad (31)$$

From (31), the average switching frequency over the region K, for $K = 1, \ldots, N$, is calculated. Assuming that the energy dissipation during the switching is linearly dependent on the collector current, the average switching loss (over the mains half-cycle) can be calculated by

$$\begin{aligned} P_{\text{sw,PWM}} &\approx \frac{2}{T_{\text{ac}}}\sum_{K=1}^{N}(t_K - t_{K-1})\cdot\langle f_S\rangle_K \\ &\quad\times\left[E_{\text{on}}\left(V_C, \langle I_{\text{in}}\rangle_K\right) + E_{\text{off}}\left(V_C, \langle I_{\text{in}}\rangle_K\right)\right] \\ &\approx \frac{2}{\pi}\sum_{K=1}^{N}\langle f_S\rangle_K\cdot\left(\cos(\omega t_{K-1}) - \cos(\omega t_K)\right) \\ &\quad\times\left[E_{\text{on}}(V_C, I_m) + E_{\text{off}}(V_C, I_m)\right]. \end{aligned} \quad (32)$$

In (32), the average input current over the region K, i.e., $\langle I_{\text{in}}\rangle_K$, has been substituted from (20). E_{on} and E_{off} are the energy dissipation during turn-on and turn-off times, respectively. Using the device datasheet, E_{on} and E_{off} are determined for the desired operating point. Also, the average switching frequency over the region K, i.e., $\langle f_S\rangle_K$, is estimated form (31).

Another component of the switching loss is due to the change of operating mode with the sampling frequency f_o (changing

TABLE II
SIMULATION DATA USED IN THE STUDY OF 11-LEVEL CHB RECTIFIER

Parameter	Symbol	Value
Number of H-bridges	N	5
Nominal power	P_t	30 kW
Peak input voltage	V_m	2694 V
DC bus voltage	V_C	600 V
DC bus capacitors	C_i	470 uF
Input inductance	L_b	10 mH
Hysteresis band	H	5 %
Proportional gain	K_p	2
Integral gain	K_I	1000
Sampling frequency	f_o	3 kHz
Line frequency	f_{line}	50 Hz

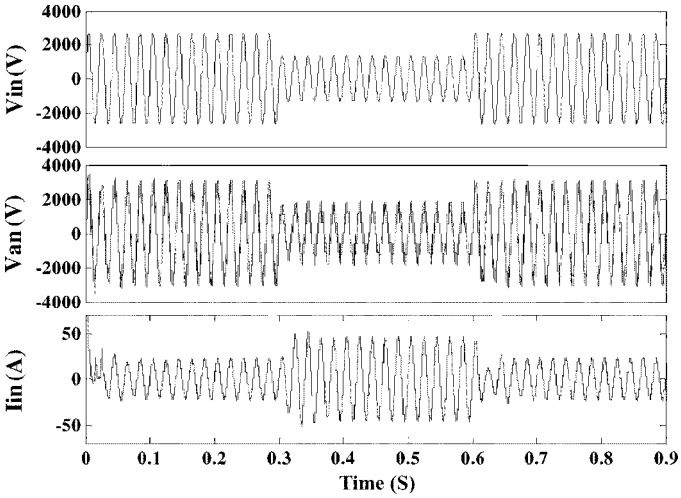

Fig. 10. Mains voltage (top), ac terminal voltage $V_{\rm an}$ (middle), and input current (bottom) during voltage sag.

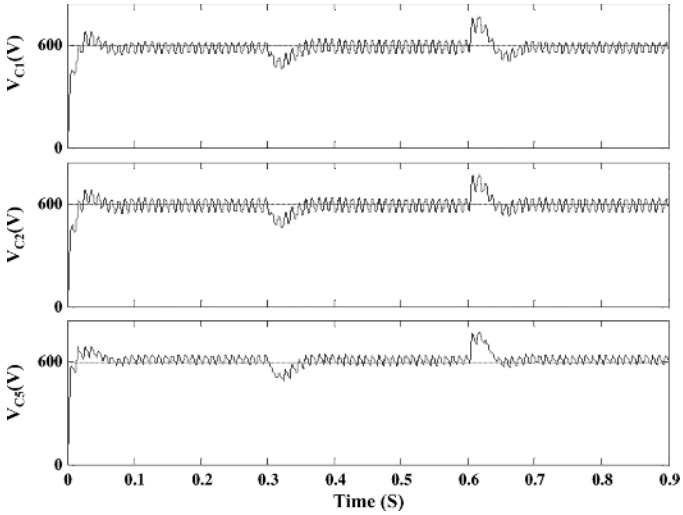

Fig. 11. DC bus voltage waveforms during voltage sag, $P_1 = 8.4$ kW, $P_2 = P_3 = P_4 = 6.55$ kW, and $P_5 = 1.4$ kW (V_{C3} and V_{C4} are same as V_{C2}).

from "0" to "+1" and vice versa). In the region K, $(K-1)$ cells must operate in the mode "+1" and (N-K) cells in the mode "0" so, the number of transitions from 0 to +1 must be equal to the transitions from +1 to 0. Thus, the maximum number of transitions in the region K is limited to the minimum of $(K-1)$ and (N-K), and the maximum switching loss due to voltage balancing is derived as follows:

$$\begin{aligned} P_{\rm sw,VB} &\approx \frac{2f_o}{T_{\rm ac}} \sum_{K=1}^{N} \min(K-1, N-K) \cdot (t_K - t_{K-1}) \\ &\quad \times \left[E_{\rm on}\left(V_C, \langle I_{\rm in}\rangle_K\right) + E_{\rm off}\left(V_C, \langle I_{\rm in}\rangle_K\right)\right] \\ &\approx \frac{2f_o}{\pi} \sum_{K=1}^{N} \min(K-1, N-K) \\ &\quad \cdot \left(\cos(\omega t_{K-1}) - \cos(\omega t_K)\right) \\ &\quad \times \left[E_{\rm on}(V_C, I_m) + E_{\rm off}(V_C, I_m)\right] \end{aligned} \tag{33}$$

where $P_{\rm sw,VB}$ is the maximum switching loss caused by the voltage balancing control. It should be noted that the maximum loss is occurred when the cells loads are equal, i.e. $P_1 = \cdots = P_N$. Otherwise, the switching loss is lower than (33).

As an example, it is assumed that $N = 5$, $V_m = 2694$ V, $V_C = 600$ V, $P_t = 29.5$ kW, $h = 0.05$, $L_b = 10$ mH, and $f_o = 3$ kHz. The IGBT module SKM50GB123D is considered as the main power switch and the device specifications are extracted from the datasheet ($V_D = 1.4$ V, $V_{\rm CEO} = 1$ V, $r_{\rm CE} = 35$ mΩ, $E_{\rm on}$(600 V,22 A) = 3.9 mWs and $E_{\rm off}$(600 V,22 A) = 2.9 mWs, and etc.). In this case, the conduction and switching losses are calculated as $P_{\rm cond} = 197.2$ W, $P_{\rm sw,PWM} = 32.8$ W, and $P_{\rm sw,VB} = 8.3$ W, respectively. It is evident that conduction loss is dominant (82.7%) and the maximum switching loss due to the voltage balancing is only 3.5% of the total losses. The loss partitioning shows that the proposed control method is suitable for the high power applications.

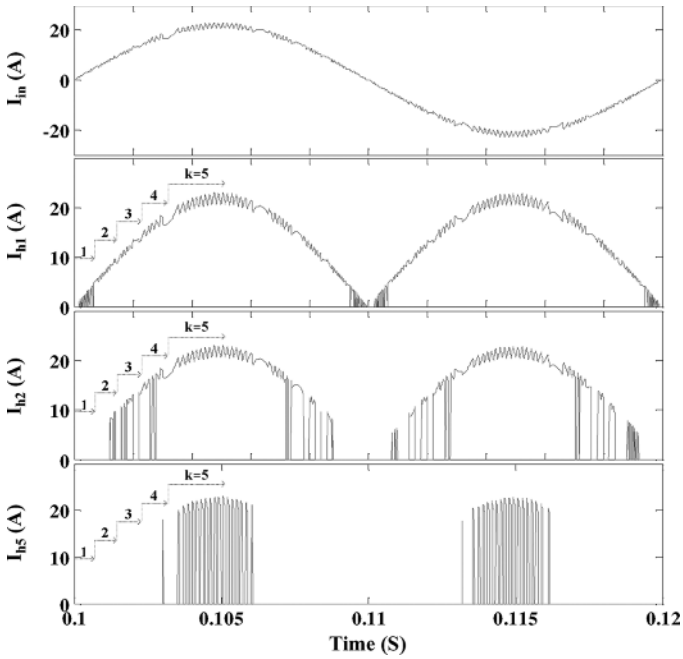

Fig. 12. Input current (top) and cells currents (I_{h1}, I_{h2}, and I_{h5}) for a line-period. The load of first cell P_1 is close to the upper limit and the load of last cell P_5 is close to the lower limit of the load power.

VI. Simulation Results

The configuration which has been chosen to verify the controller behavior is a 30 kW, 11-level, medium voltage converter with five series-connected H-bridges. Computer simulations have been carried out using MATLAB/SIMULINK program, with the system parameters given in Table II. The detailed analysis for deriving the PI controller coefficients can be found in [22].

The first simulation investigates the general behavior of the rectifier, when the H-bridge loads are not equal and a voltage sag ride-through occurs. The load values are $P_1 = 8.4$ kW, $P_2 = P_3 = P_4 = 6.55$ kW, and $P_5 = 1.4$ kW, where P_1 and P_5 have

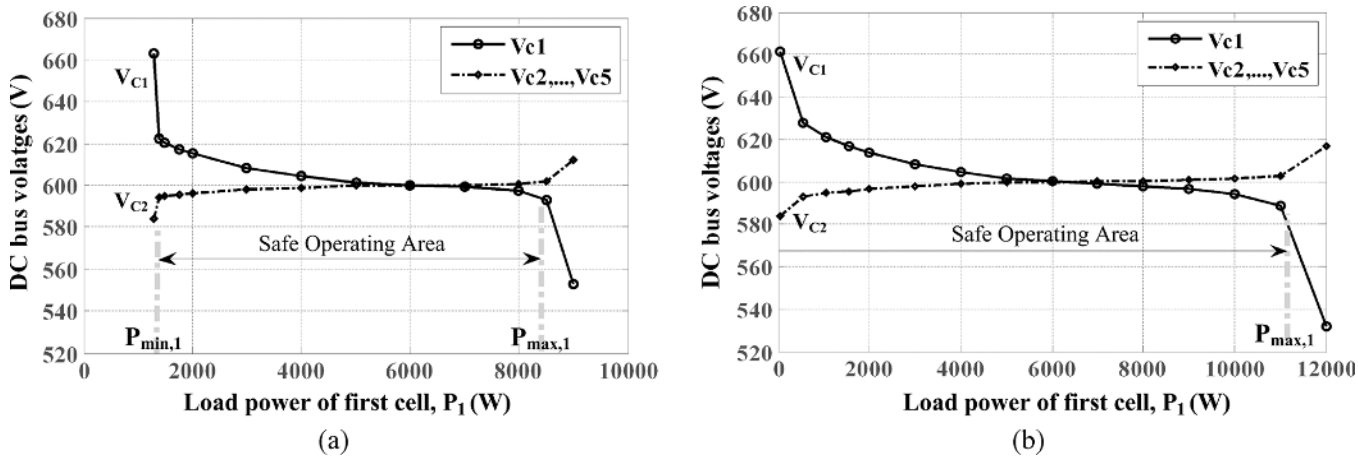

Fig. 13. Average voltage of dc buses as a function of P_1 (load power of first cell). (a) $N = 5$, $V_m = 2694$ V, $V_C = 600$ V, $P_t = 30$ kW, $P_2 = P_3 = P_4 = P_5 = P_t - P_1$, and according to (23), $P_{\min,1} = 1.28$ kW, and $P_{\max,1} = 8.42$ kW; (b) $N = 5$, $V_m = 2020$ V, $V_C = 600$ V, $P_t = 30$ kW, $P_2 = P_3 = P_4 = P_5 = P_t - P_1$, and according to (23), $P_{\min,1} = 0$, and $P_{\max,1} = 11.17$ kW.

TABLE III
LOSS PARTITIONING FOR THE INDIVIDUAL CELLS

Cell number	Load power (kW)	Conduction loss (W)	Switching loss (W)	Loss contribution	Average Freq. (kHz)
1	8.4	38.1	4.2	18.6 %	7.2
2	6.55	38.2	5.9	19.4 %	2.6
3	6.55	38.2	6.1	19.5 %	2.8
4	6.55	38.2	6.2	19.5 %	2.9
5	1.4	40.2	12.5	23.0 %	1.9
All cells	29.5	192.9	34.9	100 %	17.4

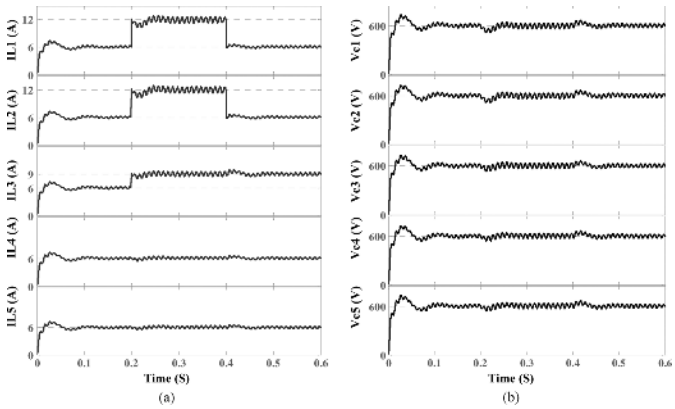

Fig. 14. Performance of the proposed scheme under load steps: (a) loads currents and (b) corresponding dc bus waveforms.

been chosen close to the upper and lower power limits according to (23) ($N = 5$, $P_t = 29.5$ kW, $V_m = 2694$ V, $V_C = 600$ V, and $PF = 1$). In this simulation, a 50% voltage sag appears in the primary voltage at $t = 0.3$ s and lasts 0.3 s. The simulation results are shown in Figs. 10–12.

Fig. 10 shows the waveforms of the mains voltage, ac terminal voltage, and the input current (from top to bottom), respectively. During the voltage sag, the number of voltage regions is automatically adjusted to the change of V_m and a seven-level waveform is synthesized on the ac side. According to (23) and (24), the minimum and maximum load power are $P_{\min,1} = 1.3$ kW and $P_{\max,1} = 8.42$ kW, before voltage sag, and $P_{\min,1} = 0$ and $P_{\max,1} = 16.43$ kW in sag condition. As a result, the safe operating area has increased owing to the two extra cells available for synthesizing $V_{\rm an}$. It is also observed that the input current is sinusoidal and in phase with the input voltage. Its amplitude increases from 22.3 to 45.5 A, during the sag period.

Fig. 11 shows the dc bus voltages V_{C1}, V_{C2}, and V_{C5} during voltage sag compensation. It is seen that all dc buses follow the reference voltage $V_C = 600$ V in both transient and steady state conditions, although the load values are not equal. After the voltage transitions at $t = 0.3$ s and $t = 0.6$ s, the capacitor voltages again approach the reference value and the settling time is less than 100 ms. The low frequency voltage ripple $(2f_{\rm line})$, which is observed at the dc buses, is inherent to the Power Factor Correction. Increasing the value of smoothing capacitors will reduce the voltage ripple.

In Fig. 12, the input current and the cells current waveforms have been shown. The input current is a sinusoidal waveform with a high frequency ripple generated by the PWM method. In fact, the plurality of series-connected cells leads to achieve an effective switching frequency that is many times the switching frequency of individual cells.

As already stated, the first cell feeds the maximum load $P_1 = 8.4$ kW and the last one the minimum load $P_5 = 1.4$ kW. It is observed that the first cell works in the charging mode, most of the time, and the last cell in the PWM mode in the region $K = 5$. The conduction and switching losses for these cells are determined by measuring the device voltage and current waveforms and calculating the device losses by the off-line program (IGBT SKM50GB123D is considered as the main power switch). The results of the loss partitioning are shown in Table III.

From Table III, it is observed that conduction losses in the H-bridge cells are almost equal, and the switching losses depend on the cells loads (switching loss is the sum of PWM

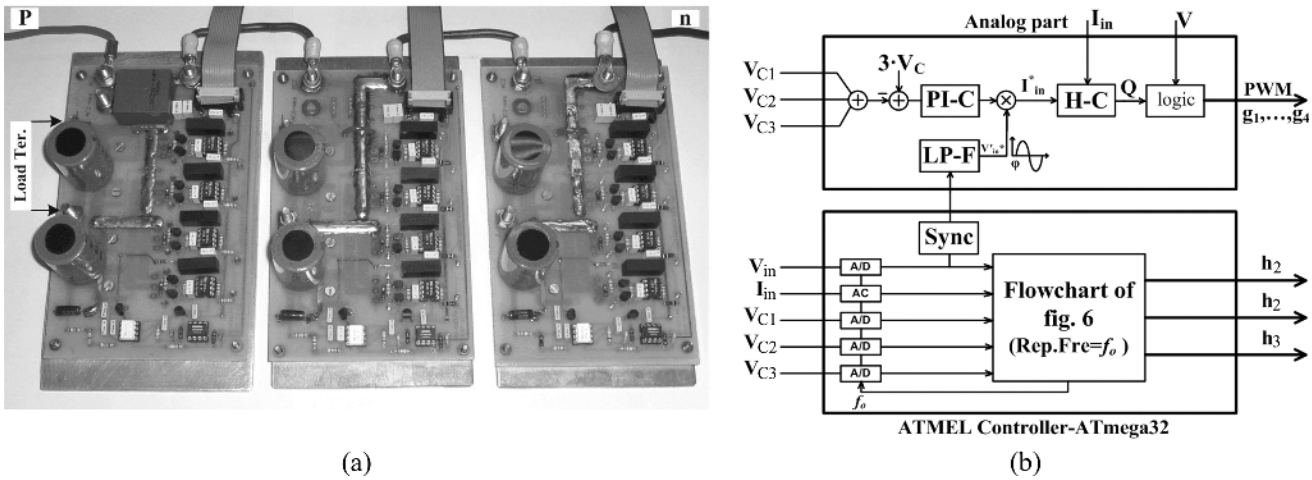

Fig. 15. (a) Prototype of the single-phase seven-level bidirectional CHB rectifier and (b) hardware block diagram of the controller.

TABLE IV
SYSTEM PARAMETERS USED IN THE SEVEN-LEVEL CHB RECTIFIER PROTOTYPE

Parameter	Symbol	Value
Number of H-bridges	N	3
DC bus capacitors	C_i	1 mF, 250V
Input inductance	L_b	2 mH
H-bridge switches	S_i	IRFP250
Nominal power	P	1800 W
Maximum power	P_{max}	2500 W
Input voltage	V_{in}	70-260 V rms
Hysteresis band	h	5 %
Proportional gain of voltage loop	K_p	0.5
Integral gain of voltage loop	K_I	235
Attenuation gain of current signal	K_{fI}	0.5
Attenuation gain of voltage signals	K_{fV}	0.008

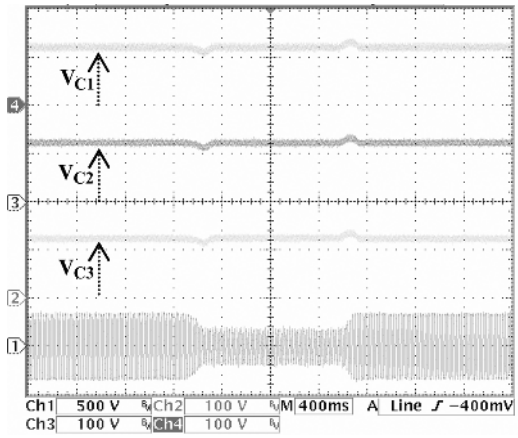

Fig. 16. DC bus voltage waveforms under voltage sag Ch_1: V_{in} (500 V/div), $\mathrm{Ch}_{2,3,4}$: V_{C1}, V_{C2}, and V_{C3} (100 V/div).

switching loss and the loss due to the voltage balancing control). The cell feeding the heavy load (8.4 kW) has the lowest switching loss and the cell feeding the light load (1.4 kW) has the highest switching loss. The loss distribution among the various cells is approximately even and the cells attached to the equal loads have equal switching losses.

In the first cell, the average switching frequency over a half-cycle, is nearly 3.8 times higher than the last cell ($f_{\mathrm{cell},1} \approx$ 7.2 kHz and $f_{\mathrm{cell},5} \approx 1.9$ kHz), but its switching loss is lower. Because, during the PWM mode of the first cell, the current amplitude is close to zero, and during the PWM mode of the last cell, it is near to the peak current (see Fig. 12).

To verify the validity of the semiconductor loss analysis, presented in Section V, the conduction and switching losses are calculated according to (29), (32), and (33). The calculated conduction and switching losses are $P_{\mathrm{cond}} = 197.2$ W and $P_{\mathrm{sw}} = 32.8 + 8.3 = 41.1$ W. Comparing the results with the data in Table III shows a good agreement between the simulation and approximate analytical results. Moreover, the calculated average switching frequencies, from (31), for the first and last cells are $f_{\mathrm{cell},1} \approx 8.6$ kHz and $f_{\mathrm{cell},5} \approx 1.65$ kHz, which are close to the results in Table III.

Fig. 13(a) and (b) verify the analysis of upper and lower limits of the load power, presented in Section IV. These figures show the average voltage of V_{C1} and V_{C2} as a function of P_1 while the total power is $P_t = 30$ kW, $V_C = 600$ V, PF $= 1$, and $P_2 = P_3 = P_4 = P_5$.

As can be seen from Fig. 13, the safe operating area in case (b) is wider than that in case (a). This is because, in case (b), the peak input voltage V_m is 2020 V and a maximum of four cells are needed to synthesize the multilevel waveform, whereas in case (a), five cells are needed to synthesize V_{an}. In both cases, crossing the power limits will cause instability of dc buses and lose of voltage balancing.

The last simulation verifies the performance of the proposed scheme under load steps. In this simulation, the loads of three cells P_1–P_3, increase simultaneously at $t = 0.2$ s. Then, the loads of two cells revert to the initial values at $t = 0.4$ s. The current waveforms and the corresponding dc bus voltages are shown in Fig. 14(a) and (b).

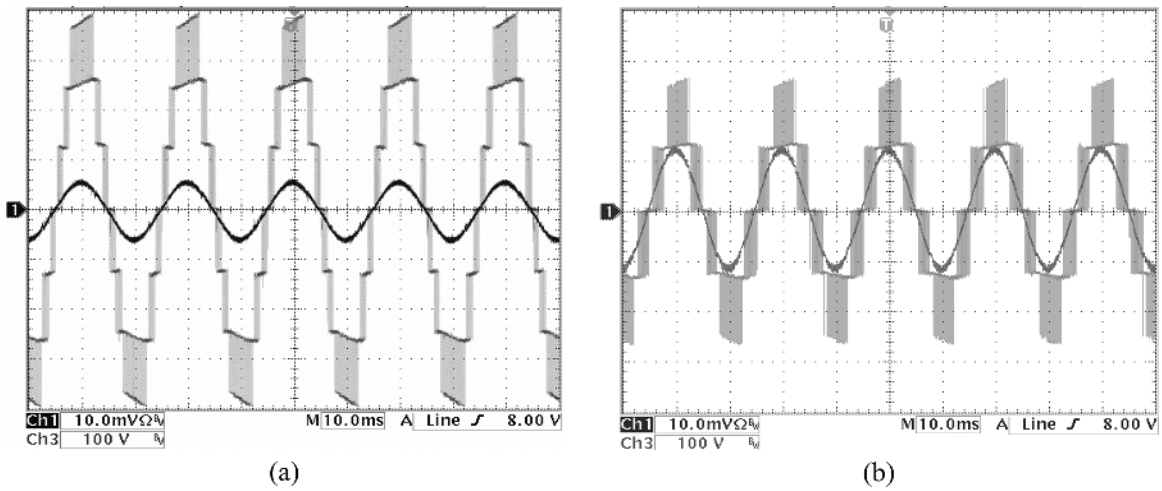

Fig. 17. AC terminal voltage $V_{\rm an}$ and input current waveforms; (a) before voltage sag and (b) during 50% voltage sag. (Current scale: 10 A/div; voltage scale: 100 V/div).

Based on the analysis presented in Section IV-A, the power limits during load-increase are derived as follows: $P_{t1} = 33$ kW, $P_{\max,1} = 9.29$ kW, $P_{\max,2} = 18.1$ kW, $P_{\max,3} = 25.85$ kW, $P_{\max,4} = 31.64$ kW and the simulation data are $P_t = 27$ kW, $P_1 = 7.2$ kW, $P_1 + P_2 = 14.4$ kW, $P_1 + P_2 + P_3 = 19.8$ kW, and $P_1 + P_2 + P_3 + P_4 = 23.4$ kW. As the loads satisfy the power limits, voltage balancing is achieved. The simulation results confirm the validity of analysis.

VII. Experimental Results

The validity of the proposed method is verified using the experimental results of the laboratory scale prototype. The prototype is a single-phase, seven-level, bidirectional rectifier with three series-connected H-bridges. The dc bus voltage reference is 125 V, and the nominal power 1800 W. The nominal ac voltage is 230 V and it can vary between 70 and 260 V rms. Other principal parameters of the prototype are given in Table IV.

Fig. 15(a) and (b), respectively, show the prototype and the hardware block diagram of the controller employed in the experimental system. It is to be noted that low voltage power MOSFETs (MOSFET+Internal Body Diode with the break down voltage of 200 V) have been intentionally used in the prototype to demonstrate a scale-down of the real situation. However, in medium voltage levels, the IGBTs would be the best choice owing to better voltage and current ratings.

First experiment investigates the voltage regulation of dc buses in steady-state and sag ride-through event. In this experiment, the input voltage decreases by 50% from the nominal value and regains the initial value after 1200 ms. At all times, the cells loads are constant and the total power is 1000 W. The results are shown in Figs. 16 and 17.

In Fig. 16, it can be seen that all dc buses closely follow the reference voltage $V_C = 125$ V and the steady-state errors are less than 1%. The voltage restoration times are less than 200 ms and the amplitude of the overshoots (or undershoot) are less than 17%.

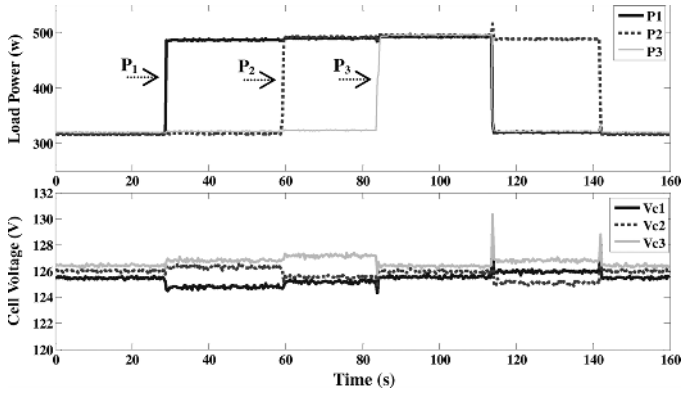

Fig. 18. Performance of proposed controller under load steps; cells loads (top), and response of dc buses under load steps (bottom).

In Fig. 17, the ac terminal voltage of rectifier $V_{\rm an}$ and the input current $I_{\rm in}$ are shown before voltage sag (left), and during voltage sag (right). During sag ride-through, the number of voltage regions is automatically adjusted to the change of V_m and a five-level waveform is generated. The current amplitude also increases from 4.14 to 8.37 A.

The second experiment evaluates the performance of the proposed controller under load steps. In this experiment, the input voltage is 230 V, and the cells loads are changed in a step-wise manner. The power and voltage of each cell is measured, using the power analyzer NORMA 5000.

In Fig. 18, initially all loads are equal to 320 W. P_1, P_2, and P_3 are increased to 480 W at $t = 30$ s, $t = 60$ s, and $t = 85$ s, respectively. Then, P_1 and P_3 are reduced to 320 W at $t = 115$ s, and P_2 returns to the initial value at $t = 140$ s. The response of different dc bus voltages under load steps is depicted in Fig. 18 (bottom). It is observed that all dc buses closely follow the reference voltage $V_C = 125$ V, despite sudden load variations. The small steady-state errors observed at dc buses are due to mismatching of isolation amplifiers utilized in the measurement of capacitor voltages.

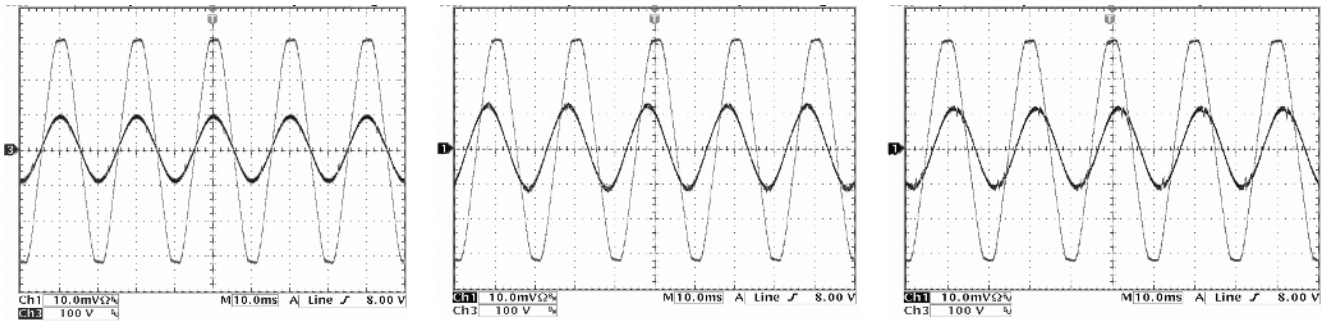

Fig. 19. Correction of power factor and reactive power compensation capability: (a) $\mathrm{PF_{in}} = 1$; (b) $\mathrm{PF_{in}} = -0.8$ lead; (c) $\mathrm{PF_{in}} = +0.8$ lag. (Current scale: 10 A/div; voltage scale: 100 V/div).

In the last experiment, the capability of the controller to adjust the input power factor and to control the reactive power is investigated. The input voltage is 230 V, P_t is 1500 W and the controller performance is verified for three values of the power factor, $\mathrm{PF} = 1$, $\mathrm{PF} = -0.8$ lead, and $\mathrm{PF} = +0.8$ lag. The corresponding waveforms are shown in Fig. 19.

In Fig. 19(a), the current and voltage waveforms have been shown when the power factor is unity. It is observed that the input current and the input voltage are in phase and the shape of input current is sinusoidal, although the input voltage has some low order harmonic content. Fig. 19(b) shows a case in which the rectifier works in capacitive mode. In this mode, the converter injects 1125 VA reactive power to the mains and absorbs 1500 W active power from it. In Fig. 19(c), the inductive case is studied, where the rectifier absorbs 1125 VA reactive power and 1500 W active power from the input source. In both inductive and capacitive modes, the amplitude of input current increases from 6.5 to 8 A rms in order to compensate the input reactive power.

VIII. Conclusion

In this paper, a new control approach for voltage balancing of distinct dc buses in CHB rectifiers has been introduced. In the proposed method, the voltage balancing and the current control are performed even if the load values are not equal or the series H-bridges have slightly different characteristics. The suggested method is extremely modular and easy to implement. It is shown that availability of extra cells for modulation improves the flexibility and the safe operating area. The mathematical formulation has been presented to determine the load power limits and validity regions of the controller. The accuracy of the theoretical analysis and control algorithm has been verified using the simulation and experimental results. The experimental prototype confirmed the feasibility of working at voltage levels beyond the classic semiconductor limits using series-connected H-bridges. This structure can be used in traction, high power conditioning and applications where a solid-state transformer is preferred to a heavy and bulky step-down transformer.

Appendix I
Calculation of Average PWM Current Over the Region K

To calculate the average of PWM current over the region K, i.e., $\langle I_{\mathrm{PWM}}\rangle_K$, we assume that the amplitude of input current and the input voltage is constant during the switching period $T_S = 1/f_S$. Considering the definition of I_{PWM} in (16), the average of PWM current over T_S is approximated as follows:

$$\langle I_{\mathrm{PWM}}\rangle_{T_S} = \frac{1}{T_s}\int_{t}^{t+T_s} I_{\mathrm{PWM}}dt \approx I_m \sin(\omega t)(1-d_K) \quad \text{(A.1)}$$

where d_K is the duty cycle of PWM signal in the region K. If for each $T_s : T_s \ll (t_K - t_{K-1})$, the average of PWM current over the region K can be approximated by the following integral:

$$\begin{aligned}\langle I_{\mathrm{PWM}}\rangle_K &\approx \frac{1}{(t_K - t_{K-1})}\int_{t_{K-1}}^{t_K} \langle I_{\mathrm{PWM}}\rangle_{T_S} dt \\ &= \frac{1}{(t_K - t_{K-1})}\int_{t_{K-1}}^{t_K} I_m \sin(\omega t)\cdot(1-d_K)dt.\end{aligned} \quad \text{(A.2)}$$

Substituting the value of d_K [given in (13)] into (A.2) and simplifying the equation results in

$$\begin{aligned}\langle I_{\mathrm{PWM}}\rangle_K \approx &-\frac{(K-1)}{2}\langle I_{\mathrm{in}}\rangle_K + \frac{V_m I_m}{2V_C} \\ &-\frac{I_m}{2\omega(t_K - t_{K-1})}\cos(\omega t_K), \quad 1 \le K \le N\end{aligned} \quad \text{(21)}$$

where $\langle I_{\mathrm{PWM}}\rangle_K$ is the average of PWM current over the region K.

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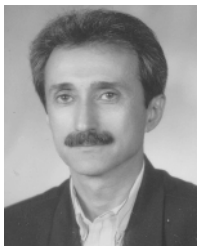

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