A Monolithic, 500°C Operational Amplifier in 4H-SiC Bipolar Technology

Raheleh Hedayati, Luigia Lanni, Saul Rodriguez, *Member, IEEE,* B. Gunnar Malm, *Senior Member, IEEE,* Ana Rusu, *Member, IEEE,* and Carl-Mikael Zetterling, *Senior Member, IEEE*

***Abstract*— A monolithic bipolar operational amplifier (opamp) fabricated in 4H-SiC technology is presented. The opamp has been used in an inverting negative feedback amplifier configuration. Wide temperature operation of the amplifier is demonstrated from 25°C to 500°C. The measured closed loop gain is around 40 dB for all temperatures whereas the 3dB bandwidth increases from 270 kHz at 25°C to 410 kHz at 500°C. The opamp achieves 1.46 V/µs slew rate and 0.25% Total Harmonic Distortion (THD). This is the first report on high temperature operation of a fully integrated SiC bipolar opamp which demonstrates the feasibility of this technology for high temperature analog integrated circuits (ICs).**

***Index Terms*— Bipolar integrated circuits (ICs), High temperature ICs, Negative feedback, Operational amplifiers.**

I. Introduction

SILICON Carbide (SiC) technology is a promising candidate for circuits operating in harsh environments with extreme ambient temperature up to 600°C, well beyond the present temperature limit of Silicon on Insulator (SOI) technology [1, 2]. High temperature operation of GaN analog and digital ICs have been reported up to 375°C to date [3, 4]. The key advantages of SiC are its wide bandgap (3.2eV for 4H-SiC), and high critical electric field (2.2 MV/cm) [5] enabling operation at high temperature in applications including Venus exploration, oil and gas drilling, aviation, and automotive industries.

Operational amplifiers are widely used in analog and mixed signal systems. High temperature opamps have been demonstrated using SiC MOSFETs and JFETs [6-8]. SiC MOSFET ICs suffer from reliability issues of the gate oxide at elevated temperatures. CMOS ICs have been demonstrated to operate up to 400°C to date [9] whereas JFET and bipolar devices suggest better reliability and stability by eliminating gate oxide and relying on p-n junctions [10, 11]. In [7] an opamp based on discrete SiC JFET devices was fabricated and characterized only at room temperature. In [8] an integrated opamp in SiC JFET was fabricated and characterized up to 576°C; however, BJTs have higher speed and better linearity and driving capability compared to JFETs.

This paper reports on performance of a monolithic two-stage opamp with negative feedback, fabricated in a 4H-SiC bipolar technology, over a wide temperature range. Although only NPN transistors with resistive loads were used, open loop gain of the opamp is still high enough and achieves stable closed loop gain with less than 0.5 dB gain reduction from 25°C to 500°C.

The Swedish Foundation for Strategic Research is acknowledged for funding. The authors are with the KTH Royal Institute of Technology, School of ICT, Kista SE-16440, Sweden (email: rahelehh@kth.se)

The integrated opamp has been fabricated on 4-inch SiC wafers with 6 epi layers. Emitter, base, and collector mesas were plasma etched. Only NPN transistors (area ≈ 0.01 mm^2) and one metal layer for interconnects were available and used. However, a recent report [12] reveals the potential use of PNP transistors in future work. More details about the processing are presented in [13].

Fig.1 (a) shows the cross section of the NPN transistor with the thickness and doping of the six epitaxial layers. The measured forward current gain (ß) versus collector current at V_{BC} = 0 V is illustrated Fig.1 (b) in which the maximum ß is reduced from 38 at 25°C to 15 at 500°C. The Spice Gummel Poon (SGP) model based on extracted parameters at 25°C and 225°C from [14] are used to simulate the circuit using Cadence Spectre. As indicated in Fig.1 (b) with the dashed lines, transistors of the opamp are biased at different operating points between 0.4 mA for the input pair and 14 mA for the output stage exhibiting ß ranging from 22 to 36 at room temperature.

II. Opamp Design

The main purpose of designing and fabricating this opamp is to demonstrate the feasibility of bipolar SiC analog circuit operating in a wide temperature range. The opamp circuit with ±7.5 V dual supply is illustrated in Fig.2 (a). It is composed of two gain stages, buffers, a level shifter and an output stage.

In the proposed opamp the input stage is a differential amplifier with resistive loads ($R_{C1,2}$). A single ended differential pair is used as the second stage. In addition, a buffer has been used between the first and second stage to decrease the loading effect on the first stage. A symmetrical layout of the differential input is attempted to improve the matching, thus reducing the input offset voltage. In the next stage, a level shifter composed of a transistor, Q_7, a resistor, R_3, and a current source, Q_{17} is used to shift the output dc level to zero. An output stage formed by Q_9 and Q_{10} is chosen as the last stage. Owing to the low output impedance of this topology the circuit is capable of driving low resistances. In addition, large swing between $(V_{CC} - V_{sat9})$ and $(V_{EE} + V_{sat10})$ is provided at the output.

Accordingly, the low frequency open loop gain of the

opamp is given by

$$A_{OL} = \frac{I_{C1} \cdot I_{C2} \cdot R_{eq} (gm_{5,6} \cdot R_{C3})}{V_T \cdot I_{EE}}, \quad (1)$$

where $gm_{5,6}$ is the transconductance of $Q_{5,6}$ and $R_{eq} = R_{C1,2} \parallel (r_{\pi 3,4} + \beta_{3,4}(r_{\pi 5,6} + \beta_{5,6} \cdot R_E))$ is the effective load of the single ended amplifier. Equation (1) implies that the open loop gain is temperature dependent. The simulated open-loop gain decreases from 79 dB at 25°C to 68 dB at 225°C respectively. Provided that there is enough loop gain in the negative feedback configuration this dependency can be mitigated. Precise gain with high linearity can be achieved, using negative feedback. The opamp has been used in a negative feedback configuration which is illustrated in Fig.2 (b). The closed loop gain (A_{CL}) is expressed as

$$A_{CL} = \frac{A_{OL}}{1+\beta A_{OL}} \cong \frac{A_{OL}}{1-\frac{R_1}{R_2}A_{OL}} \cong -\frac{R_2}{R_1}. \quad (2)$$

To acquire sufficient gain accuracy, a high open loop gain is desired. In this process, the integrated resistors, with ratio of R_2/R_1=100, are implemented in the highly doped collector epitaxial layer resulting in $A_{CL} \cong -100$. An integrated capacitor (C_3) of 6 pF parallel to R_2 was used to improve the stability. In addition, lag compensation is realized by an integrated 4 pF capacitor, C_2, which rolls-off half of the contribution of the first stage at high frequencies.

III. Experimental Results

The fabricated opamp was characterized in the range 25°C to 500°C using on wafer measurements in a high temperature probe station. Although no reliability testing has been performed, no performance degradation was seen during the two hours measurements at 500°C. Fig.3 shows the microphotograph of the opamp in closed-loop configuration.

The Miller compensation method has been used to stabilize the closed loop opamp. An integrated 30 pF Miller capacitor (C_1) was implemented for compensation; however, in the measurement 30 pF did not provide stability thus an extra 330 pF off-chip capacitor (C_{ext}) was also required to stabilize the opamp. This method results in much smaller bandwidth by imposing a dominant low frequency pole at the input of the second stage.

The critical parameters of opamp have been measured. Fig.4 shows the frequency response of the closed-loop opamp with RL= 500Ω connected to the output at different temperatures. The achieved DC gain and gain bandwidth (GBW) at room temperature are 39.86 dB and 5.92 MHz, respectively. Increasing temperature up to 500°C results in a slight gain and GBW reduction to 39.46 dB and 4.36 MHz, respectively. However, the 3dB bandwidth increases from 270 kHz at room temperature to 410 kHz at 500°C. As the temperature increases up to approximately 200°C, the value of the integrated resistors decreases. In particular, the reduction of R_{bias} results in larger currents available at the output of the current mirrors. The increase of biasing currents and reduction of resistor values have two visible effects on the performance of the amplifier. First, the cutoff frequency (f_t) of the transistors increases, which in addition to smaller RC constants enable the amplifier to achieve larger bandwidth (BW). Second, the slew rate (SR) increases at higher temperatures. Although the extrapolated results from (2) show that the open-loop gain of the opamp decreases from 76.3 dB at room temperature to 64 dB at 500°C, it is sufficient to preserve a relatively constant closed-loop gain over the wide temperature range.

The measured dynamic range of the opamp at different temperatures is shown in Fig.5 (a). The amplifier is working in the linear region. With $\pm$7.5 V dual supply voltage, the output swing is 10 V at room temperature. Increasing temperature results in slightly larger output swing due to negative temperature coefficient of V_{BE} i.e. -2 mV/°C. The opamp achieves 10.6 V output swing at 500°C.

To measure the slew rate, a 33 pF capacitor (C_L) in parallel with a 500 Ω resistor (R_L) are connected externally as load. Slew rate can be estimated as $SR = \max(\frac{d_{vo}}{d_t}) = \frac{2I_{C1}}{C_C+C_L}$. Since the compensation capacitor, $C_C = C_1 \| C_{ext} = 360\,pF$, is about eleven times larger than the load capacitor, the output node is not slew limiting. Fig.5 (b) shows the slew limiting of the step response at the output of the opamp. All the external components (R_L, C_L, and C_{ext}) are kept at room temperature. The positive and negative slew rates are $1.46\ \frac{V}{\mu s}$ and $1.25\ \frac{V}{\mu s}$ respectively at room temperature. The load sees lower resistance in the positive going edge, which results in the higher positive slew rate. However, due to larger currents and faster discharge at elevated temperatures a higher negative SR of $2.16\ \frac{V}{\mu s}$ has been identified at 500°C.

Power supply rejection ratio (PSRR) for the positive and negative lines are measured separately. For this purpose, an AC signal is injected to the corresponding power line, while the input is grounded. The measured positive and negative PSRR at 1kHz decreases from -88.8dB and -77.6 dB at 25°C to -68.5 dB and -67.5 dB at 500°C.

Total Harmonic Distortion (THD) of the fabricated opamp is derived from $(\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2})/V_1$ with fundamental frequency of 9.9 kHz. Considering the first nine harmonics of the output spectrum from spectrum analyzer, THD of 0.25% and 0.3% are achieved at 25°C and 500°C respectively. Very little linearity degradation has been identified at 500°C. The opamp is operational with similar performance for the supply range between $\pm$5.5 V and $\pm$13.5 V and consumes 7 mA and 104 mA respectively.

Table I summarizes the measured performance of the opamp in inverting configuration. Finally, a comparison of high temperature opamps is provided in Table II. Higher gain bandwidth was achieved compared to [8] due to inherently higher speed of bipolar devices.

IV. Conclusion

A monolithic 4H-SiC bipolar two-stage opamp has been fabricated and characterized. Successful operation of the opamp with stable gain has been demonstrated over a wide temperature range from 25°C up to 500°C. Stable closed-loop gain with 0.4 dB gain reduction from 25°C to 500°C was achieved.

REFERENCES

[1] L. Toygur, A. C. Patil, J. Guo, *et al.*, "A 300°C, SOI transimpedance amplifier with application to capacitive temperature sensing." IEEE Sensors, pp.1-4, 2012.

[2] K. Grella, *et al.*, "Reliability Investigations up to 350° C of Gate Oxide Capacitors Realized in a Silicon-on-Insulator CMOS Technology." *J. Microelectron. Electron. Packag.*, vol. 10, pp. 150-154, 2013.

[3] A. M. H. Kwan, X. Liu, and K. J. Chen, "Integrated gate-protected HEMTs and mixed-signal functional blocks for GaN smart power ICs," *IEEE International Electron Devices Meeting (IEDM)*, pp. 7–3, 2012.

[4] Y. Cai, *et al.*, "High-temperature operation of AlGaN/GaN HEMTs direct-coupled FET logic (DCFL) integrated circuits," *IEEE Electron Device Lett.*, vol. 28, pp. 328–331, 2007.

[5] C.-M. Zetterling, *Process Technology for Silicon Carbide Devices*. London, UK: IET, 2002.

[6] Z. Stum, *et al.*, "300°C Silicon Carbide Integrated Circuits," *Mater. Sci. Forum*, vol. 679–680, pp. 730–733, 2011.

[7] A. Maralani and M. S. Mazzola, "The design of an operational amplifier using silicon carbide JFETs," *IEEE Trans. On Circuits Syst.*, vol. 59, pp. 255–265, 2012.

[8] A. C. Patil, *et al.*, "Fully-monolithic, 600°C differential amplifiers in 6H-SiC JFET IC technology." *IEEE CICC*, pp. 73-76, 2009.

[9] R. A. R. Young, *et al.*, "High temperature digital and analogue integrated circuits in silicon carbide," *Materials Science Forum*, vol. 740, pp. 1065–1068, 2013.

[10] L. Lanni, B. G. Malm, M. Ostling, and C.-M. Zetterling, "500 Bipolar Integrated OR/NOR Gate in 4H-SiC," *IEEE Electron Device Lett.*, vol. 34, pp. 1091–1093, 2013.

[11] P. G. Neudeck, *et al.*, "Stable Electrical Operation of 6H-SiC JFETs and ICs for Thousands of Hours at 500," *IEEE, Electron Device Lett.* vol. 29, pp. 456–459, 2008.

[12] L. Lanni, B. G. Malm, M. Ostling, and C.-M. Zetterling, "Lateral pnp Transistors and Complementary SiC Bipolar Technology." *IEEE Electron Device Lett.* vol. 35, pp. 428-430, 2014.

[13] L. Lanni, B. G. Malm, M. Östling, and C. M. Zetterling, "SiC Etching and Sacrificial Oxidation Effects on the Performance of 4H-SiC BJTs," *Materials Science Forum*, vol. 778, pp. 1005–1008, 2014.

[14] L. Lanni, R. Ghandi, B. G. Malm, C. Zetterling, and M. Ostling, "Design and characterization of high-temperature ECL-based bipolar integrated circuits in 4H-SiC," *IEEE Trans. On Electron Devices*, vol. 59, pp. 1076–1083, 2012.

[15] D. M. Brown, "Silicon Carbide MOSFET Integrated Circuit Technology," *Phys. Status Solidi A*, vol. 162, pp. 459-479, 1997.

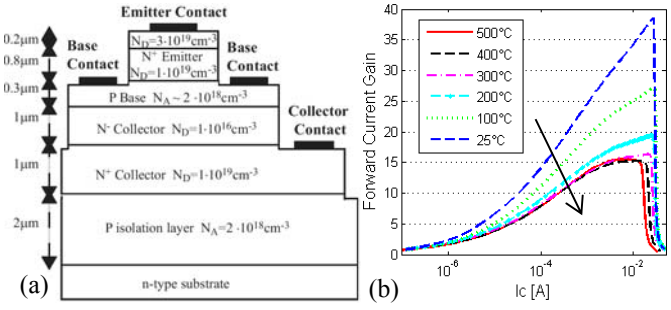

Fig.1. (a) Cross section view of SiC NPN transistor and its microphotograph (b) Measured ß versus I_C of NPN transistor from 25°C to 500°C.

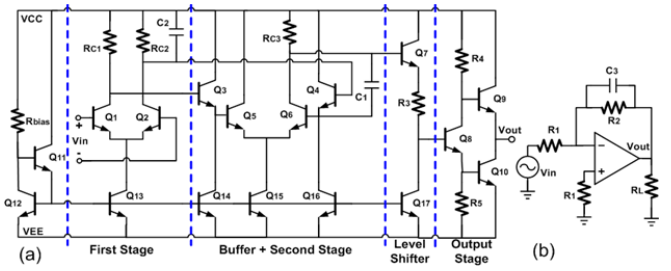

Fig.2. (a) Operational amplifier schematic (b) Opamp in closed loop configuration.

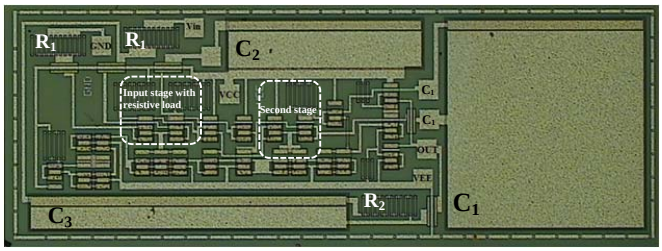

Fig.3. Microphotograph of the Op-Amp with integrated feedback resistor (Total area ~ 3.75 mm^2)

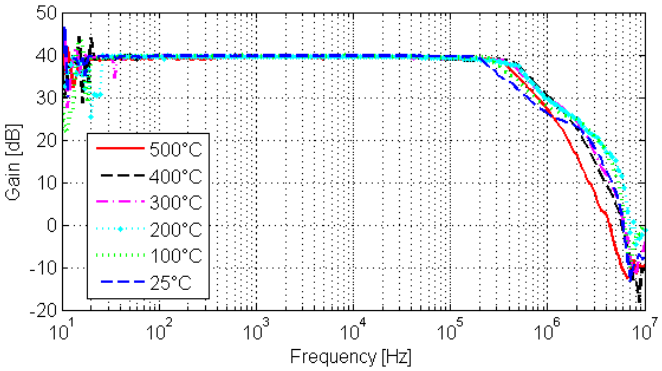

Fig.4. Measured frequency response of the closed loop opamp by applying a sinusoidal voltage with V_{P-P} = 30 mV at the input from 25°C to 500°C.

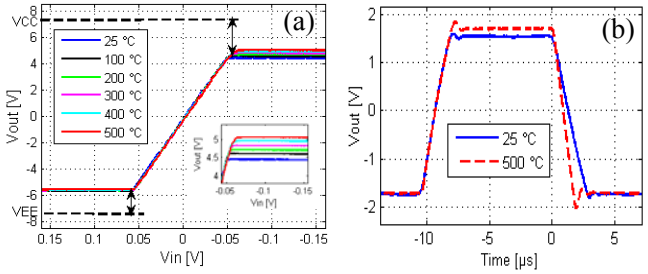

Fig.5. (a) Output swing from 25°C to 500°C (b) Step response of the opamp

TABLE I
MEASURED PERFORMANCE OF THE INVERTING OPAMP

Parameter	25°C	500°C
DC closed loop gain (dB) (R_L= 500 Ω)	39.86	39.46
3dB-bandwidth (kHz)	270	410
Unity gain frequency (MHz)	5.92	4.36
Positive/Negative Slew Rate (V/µs)	1.46/1.25	1.46/2.16
Output swing (V)	10	10.6
Positive/Negative PSRR (dB) @ 1 kHz	-88.8/-77.6	-68.5/-67.5
Total Harmonic Distortion	-52dB/0.25%	-50dB/0.3%
Input referred offset (mV)	0.24	0.79
Output resistance (Ω)	1.7	7
Input resistance (Ω)	101	138
Input referred noise (nV/$\sqrt{\text{Hz}}$)	835	-
Current consumption (mA) @ ±7.5 V	16	21

TABLE II
COMPARISON OF HIGH TEMPERATURE OPAMPS IN SILICON CARBIDE

Technology	Temperature	A_{OL}(dB)	Gain-Bandwidth GBW(kHz)
4H-SiC MOSFET [6]	300°C	57	-
6H-SiC MOSFET [15]	300°C	53	269
6H-SiC JFET [8]	576°C	69	1400
4H-SiC bipolar (this work)	500°C	64	4360