A MONOLITHIC THERMOPILE DETECTOR FABRICATED USING INTEGRATED-CIRCUIT TECHNOLOGY

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ABSTRACT

A thermopile infrared detector fabricated using silicon integrated-circuit technology is described. The device uses a series-connected array of thermocouples whose hot junctions are supported on a thin silicon membrane formed using anisotropic etching and a diffused boron etch-stop. The membrane size and thickness control the speed and responsivity of the structure, which can be designed for a given application. For a membrane measuring 2mm x 2mm x 1μm and containing sixty bismuth-antimony couples, the structure produces a responsivity of 7 volts/watt and a time constant of about 15 msec. Polysilicon couples and the use of slotted membranes can provide further performance improvements while retaining compatibility with on-chip signal processing circuitry.

INTRODUCTION

Thin-film thermopile infrared detectors(1-5) offer a combination of low cost, very broad spectral response, low noise, and insensitivity to ambient temperature which makes them attractive for many applications, including intrusion alarms, radiometers, and gas analyzers. In the past, such detectors have typically been realized using vacuum evaporation and shadow masking on plastic or alumina substrates. This has resulted in relatively large feature and die sizes and in processes which lack the batch fabrication, flexibility, and on-chip circuit compatibility characteristic of devices based on the full range of silicon integrated-circuit process technology. This paper describes a monolithic silicon thermopile detector based on this broader technology and explores the tradeoffs among responsivity, speed, and minimum detectable power for these structures.

DETECTOR STRUCTURE AND FABRICATION

The basic detector structure is shown in Fig. 1. It consists of a series of thermocouples whose hot junctions are supported by a thin silicon membrane (window) and whose cold junctions are formed on the thick chip rim. The membrane area is coated with a thin layer of an absorbing material such as bismuth oxide so that energy incident on the chip is absorbed over a broad spectral range (from the visible to the far infrared). This energy absorption causes a temperature rise in the area of the hot junctions due to the high thermal resistance between this area and the thick rim. The temperature rise is converted into an electrical output via the Seebeck coefficient of the thermocouple employed. Both bismuth-antimony and polysilicon-gold couples have been used. Figure 2 shows a typical Bi-Sb thermopile. The die size is 3.5mm x 3.5mm x 1μm thick. The detector uses 10μm minimum features and employs 60 thermocouples.

The process used to realize this detector structure has been designed to be compatible with the eventual inclusion of on-chip circuitry for signal amplification and conditioning. To begin this process, a shallow highly-doped boron diffusion is first performed over the intended window area. The depth of this diffusion will determine the final thickness of the membrane. If on-chip circuitry is to be used, the diffusion can be selectively masked from the rim areas using a conventional silicon dioxide layer; otherwise, the diffusion can be unmasked. A thin dielectric layer is next grown or deposited over the wafer. It is important that this layer be relatively low in stress to avoid deformation of the window following its formation. Both thermal silicon dioxide and CVD silicon oxynitride layers have been investigated.

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Following deposition of the dielectric layer, the thermocouple materials and interconnecting metallization are deposited and patterned. Gold-on-chromium is used for interconnections and is patterned using conventional lithography. For bismuth-antimony couples, these materials are patterned using inverse masking (lift-off) at present. The thermocouples are aligned with a silicon dioxide layer on the back of the wafer which is used to selectively define the membrane area. The membrane is formed using an ethylene diamine-pyrocatechol (EDP) mixture(6), whose etch rate in silicon is known to fall to virtually zero for boron concentrations exceeding $5 \times 10^{19} cm^{-3}$ (7). This etch is the final step in the process, which minimizes handling problems and allows the etch to be used to separate the chip from the wafer as well. Membranes as thin as 0.5μm have exhibited high yield and considerable strength over areas as large as $10mm^2$.

DETECTOR MODELING AND CHARACTERIZATION

Three parameters are of primary interest in these devices: responsivity (output voltage per watt of incident power), response time, and minimum detectable input power. In order to assess the relative roles of the various structural components of the detector in determining these parameters, a thermal model for the structure has been developed. A simplified version of this model is shown in Fig. 3. Using the model, the expected output voltage (responsivity) and speed of the detector can be computed. Excellent agreement between the calculated and experimentally measured characteristics has been obtained using a value of 0.7 watts/°C-cm for the thermal conductivity of the boron-doped silicon membrane. This value is also in agreement with extrapolations based on published data for more lightly-doped material(8). The thermal resistance of the membrane, together with the type and number of thermocouples used, largely determines the responsivity of the device. The thermal conductances of the dielectric layer and the leads play a relatively minor role. The thermal membrane resistance, when combined with the thermal capacitance of the window, also determines the response time of the device, allowing responsivity to be traded for speed and vice-versa. The minimum input power is largely set by thermal noise in the thermopile, which is reduced by minimizing the electrical resistance of the detector.

While the relatively low thermal resistance of silicon as compared with other window materials such as alumina and plastic implies a faster response and a somewhat lower responsivity for this detector structure, the imporved feature sizes for this process allow for increased responsivity by permitting the use of more couples for a given die size. Furthermore, as more couples are added, the minimum detectable input power will also improve so long as system noise is limited by the interface electronics and not by the thermopile itself.

Figure 4 shows the calculated performance of a silicon-membrane thermopile detector as a function of window size. These calculations have been confirmed experimentally for the sizes presented. For the structure shown in Fig. 2, a responsivity of 7 volts/watt and a time constant of about 15 msec have been measured. This responsivity is comparable to that of commercial detectors of similar die size, while the speed is faster by a factor of about four. Figure 5 shows the amplified response of such a detector to a chopped 500°K black-body source.

The use of polysilicon-gold couples can improve the responsivity by a factor of two over that of the Bi-Sb couple while simplifying the process by achieving a thermopile which resists attack in EDP. Slotted membranes (e.g., along two sides), produced by masking the boron diffusion, allow additional improvements in responsivity, while sacrificing some speed. Finally, the use of ion-beam milling to achieve improved aspect ratios and lower electrical resistance for the thermopile leads can reduce the thermal noise of such devices, improving the minimum detectable input power and/or the responsivity while maintaining compatibility with the use of on-chip circuitry for signal amplification and conditioning.

ACKNOWLEDGMENTS

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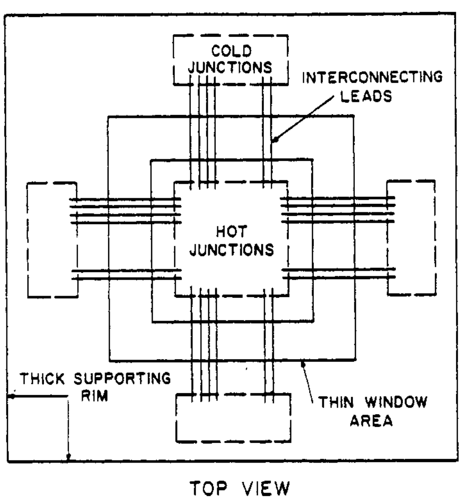

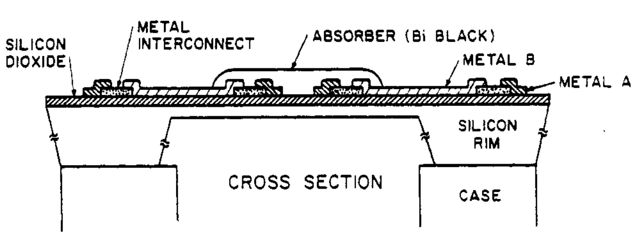

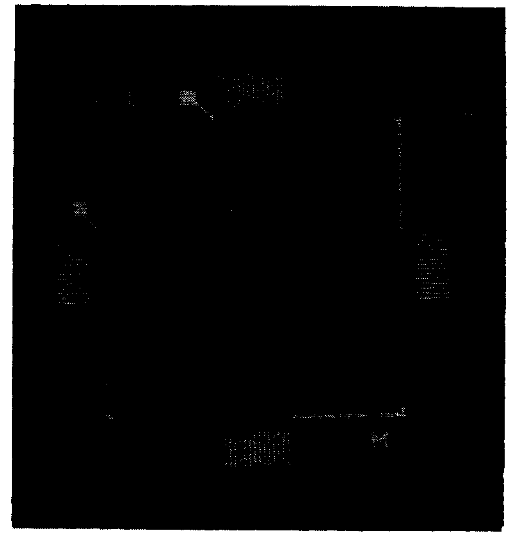

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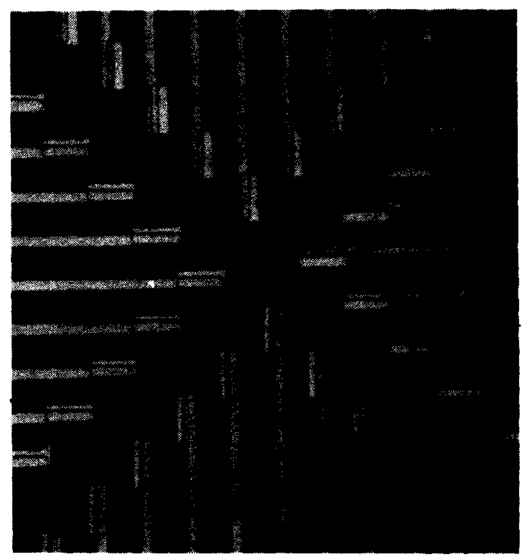
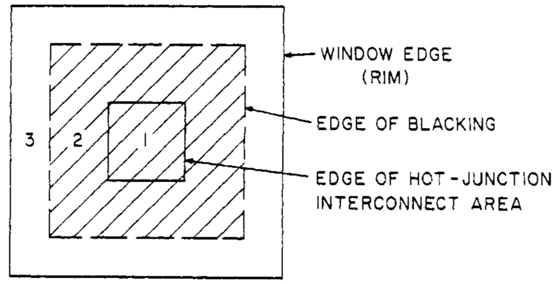


(b)

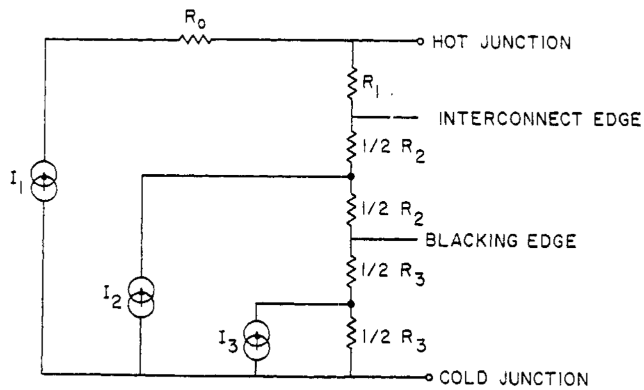
Fig. 2: Actual Thermopile Detector Chip. The device contains 60 Bi-Sb thermocouples on a 2mm x 2mm x 1μm-thick silicon membrane. Die size is 3.5mm x 3.5mm with 10μm minimum features. (a) Complete detector. (b) Close-up of the hot-junction area. (Shown before blacking).

Fig. 1 (at left): A Monolithic Silicon Thermopile Detector Fabricated Using Integrated-Circuit Technology.

Fig. 3 (at right): Simplified lumped model of the thin membrane area.

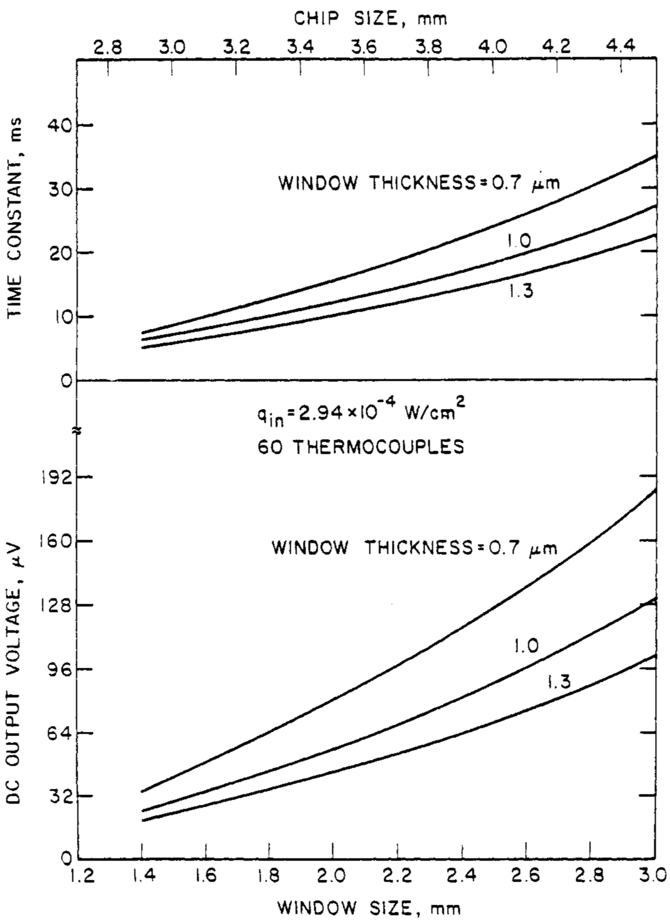


TOP VIEW OF DETECTOR WINDOW



THERMAL WINDOW MODEL

Fig. 4 (below): Calculated performance of silicon-window Bi-Sb thermopile detectors as a function of window size for a fixed thermocouple array.



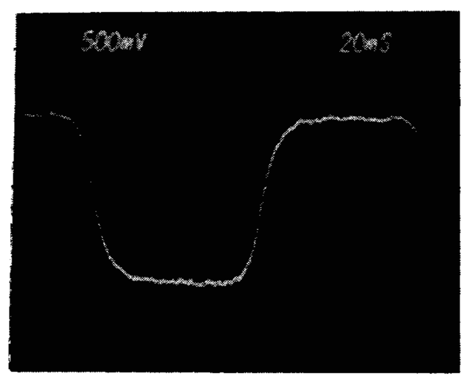


Fig. 5: Amplified response of the thermopile detector to a chopped 500°K black-body source.

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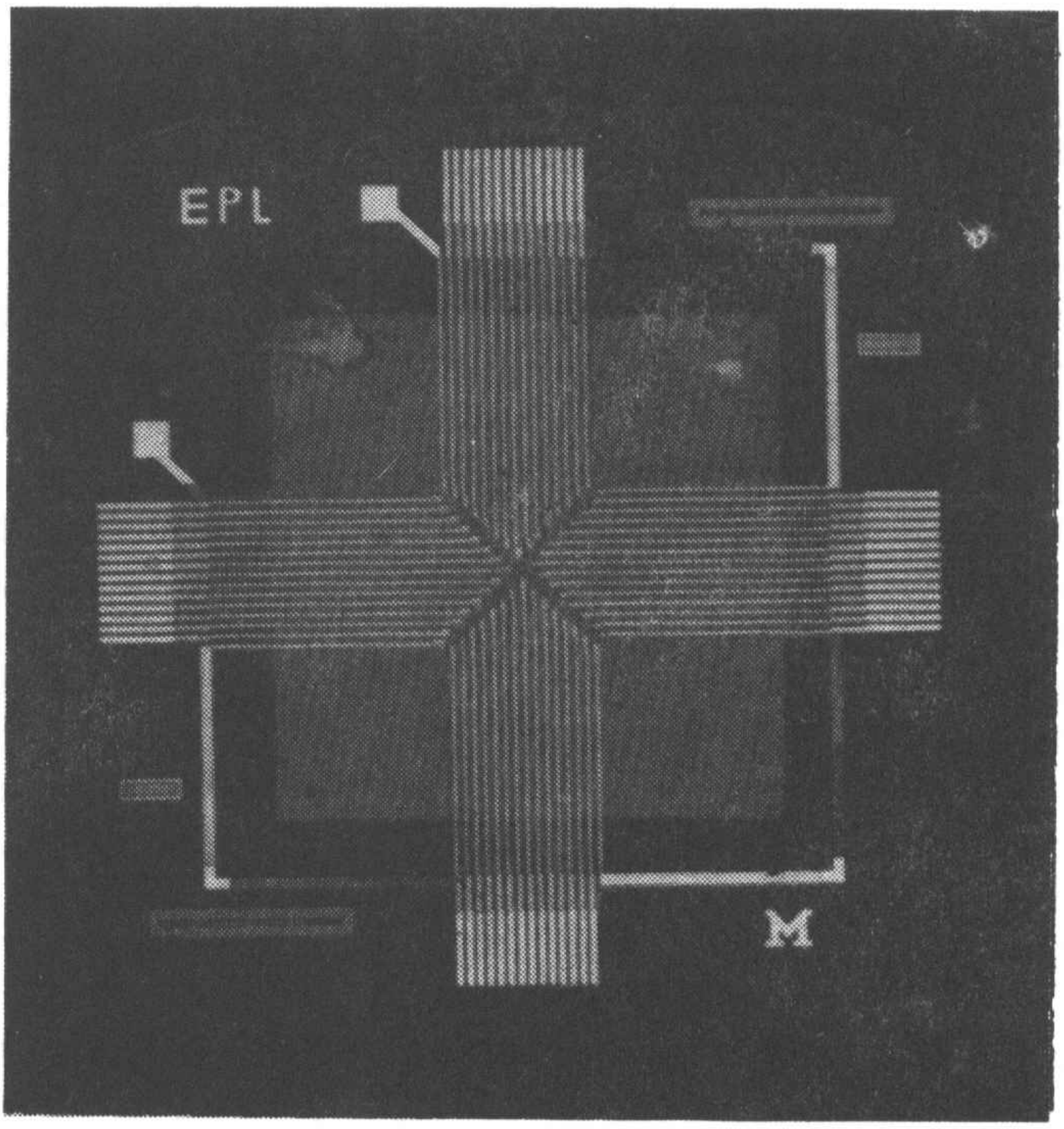

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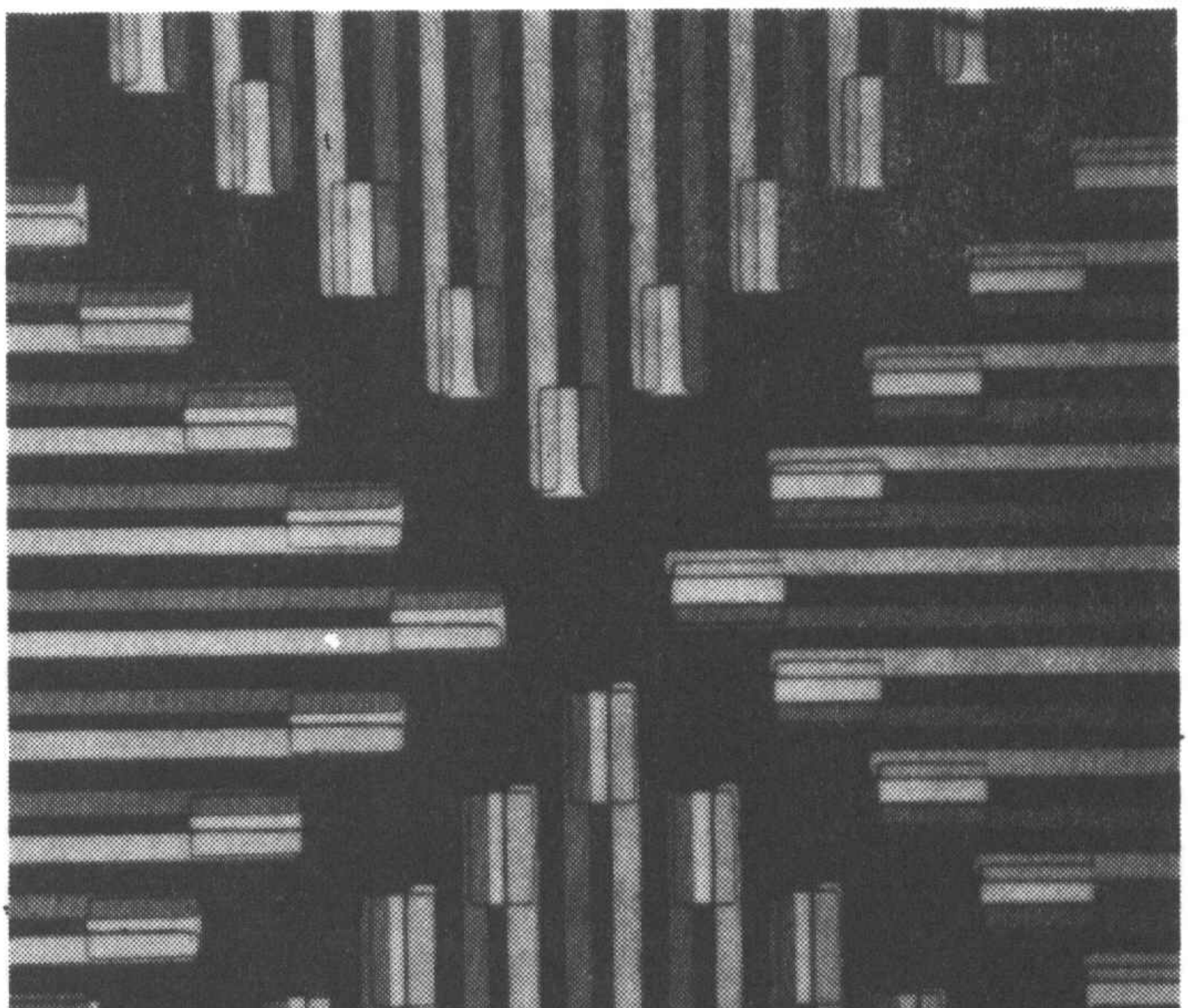

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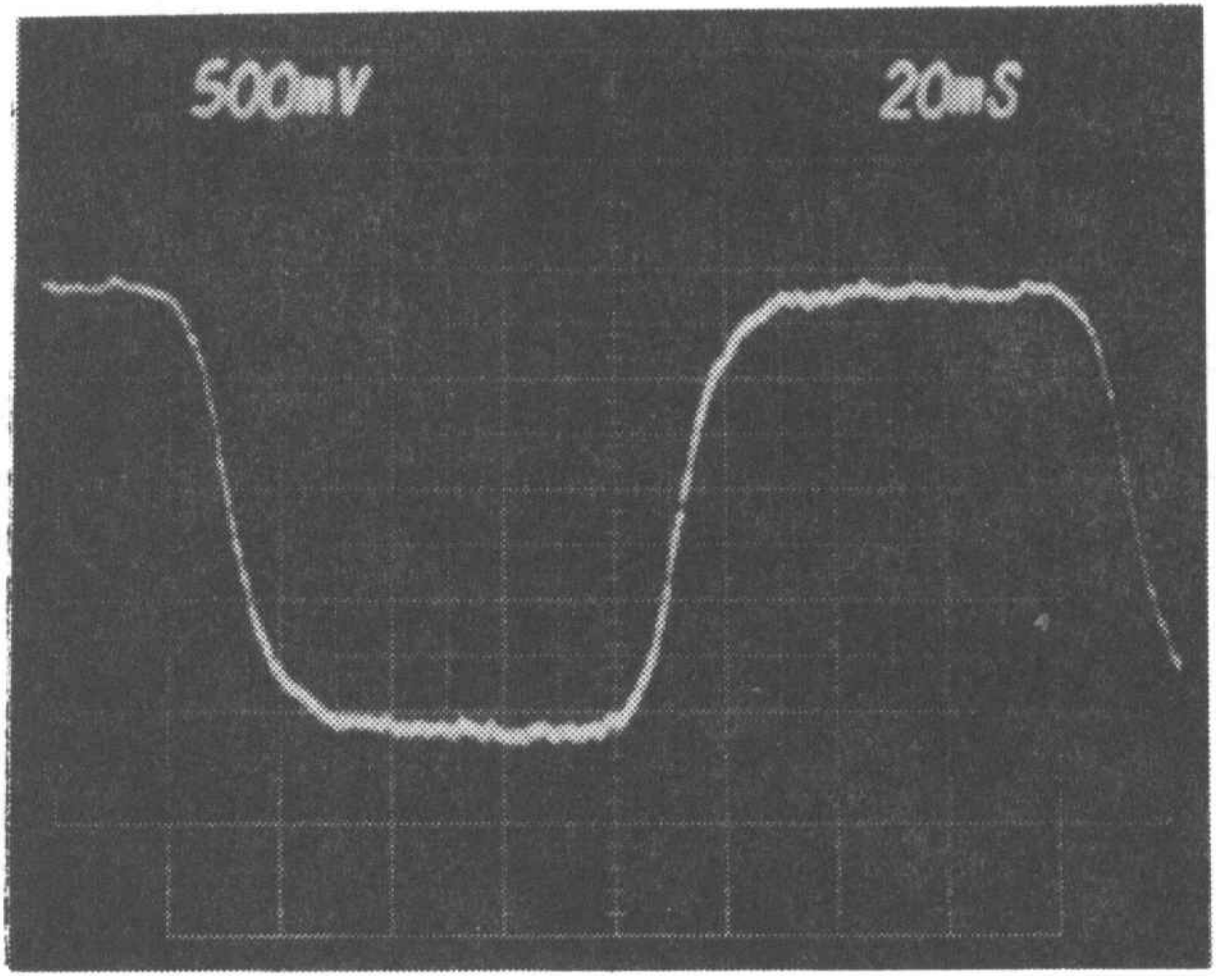

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