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A monolithically integrated optical repeater

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A monolithically integrated optical repeater has been fabricated on a single-crystal semi-insulating GaAs substrate. The repeater consists of an optical detector, an electronic amplifier, and a double heterostructure crowding effect laser. The repeater makes use of three metal semiconductor field effect transistors, one of which is used as the optical detector. With light from an external GaAlAs laser incident on the detector, an overall optical power gain of 10 dB from both laser facets was obtained.

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The potential attractiveness of semiconductor-based integrated optics[1] is due, in large measure, to the possibility of combining electronic and optical functions on single-crystal chips. We have recently demonstrated the integration of a Gunn diode oscillator and a semiconductor injection laser[2] and a field effect transistor and an injection laser.[3] In this letter, we describe an integrated circuit consisting of an optical detector, a current amplifier, and an injection laser. The device performs as an optical repeater, and can be considered as a forerunner of a family of devices having optical inputs and outputs, but with intermediate electronic processing. These devices, while benefitting from the advanced state of the art of semiconductor electronics, also combine the inherent advantages of optical signal transmission for input and output.

A schematic illustration of the repeater is shown in Fig. 1. The repeater consists of the three MESFETS's Q_1, Q_2, Q_3 and the laser diode. The transistors all reside on a common mesa, and the laser sits on a second mesa atop the first mesa. Transistor Q_1 forms a current source, Q_2 is the optical detector, and Q_3 is the laser driver. A MESFET was chosen as the optical detector because of its potential in use as a sensitive high speed detector.[4,5] The laser is of the crowding effect type,[6] with the injected current and hence the optical mode confined to a very narrow region near the edge of the mesa.

The theory of operation of the repeater can be understood by referring to Fig. 2. With no optical signal applied, a negative voltage, which is near V_{ss} in value, appears at G_3, which cuts off Q_3. The only current which then passes through the laser is the external bias current which is adjusted to bias the laser near threshold. When light is incident on the detector, photocarriers are generated in those areas of the channel not covered by the gate metallization. We have found that this results in a change of the I-V characteristics of the detector as shown in Fig. 2(b). The gate voltage V_{G_1} is adjusted to bring the I-V curve of Q_1 roughly midway between the illuminated and unilluminated I-V curves of Q_2. The application of an optical input therefore leads to a positive voltage change ΔV appearing at G_3. This causes Q_3 to conduct and to drive the laser current above threshold, threby regenerating the optical input.

Fabrication of the repeater begins with a five-layer LPE growth on a (001) substrate. After evaporating Cr-Au to form the p-type contact, a mesa is etched along the $[1\bar{1}0]$ direction to form the laser. The laser mesa is formed by first etching through the active layer and into the n-GaAlAs layer is etched away using HF as a selective etchant. The ex-

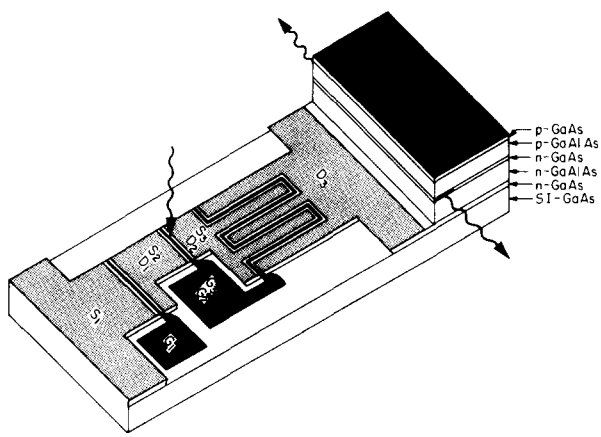

FIG. 1. Schematic view of the integrated optical repeater.

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posed n-GaAs layer layer is then partially etched to obtain the desired transistor characteristics. Metallization for the n-type contacts is applied by shadow evaporating Au-Ge and Au from the direction of the laser mesa. The transistor mesa is defined by etching the surrounding area with 1 : 8 : 8 (H_2SO_4 : H_2O_2 : H_2O) down to the substrate. Use of this etchant results in mesa edges whose slope depends on the orientation of the mesa with respect to the crystal. Because of our choice of device orientation, those mesa edges which are covered by gate metallization are properly sloped to ensure complete coverage by the deposited metal. The Schottky gates are formed using a self-aligned process[3] to deposit the Al gates between the source and drain metallizations. After alloying the Au-Ge contacts, the substrate is thinned and the wafer is cleaved into individual devices whose dimensions are nominally 425 by 1500 μm.

In the device reported here, the laser had a length of 480 μm, a room-temperature pulsed threshold current of 400 mA, and a differential quantum efficiency of 5% per facet. The bottom n-GaAs layer was doped to a carrier concentration of 2×10^{16}cm^{-3} and had a final thickness after etching of 0.6 μm. The gate length for the transistors was 5 μm, and the pinchoff voltage was 5 V. The transconductance of Q_3 was found to be 12 millimho. The amplifier section of the repeater was checked by applying an ac signal having a source impedance of 50 Ω to G_1 and a 50 Ω load to ground at D_3. The power gain was measured as 20 dB at 660 MHz.

Because the laser did not operate cw, the repeater had to be operated on a pulsed basis. This was accomplished by

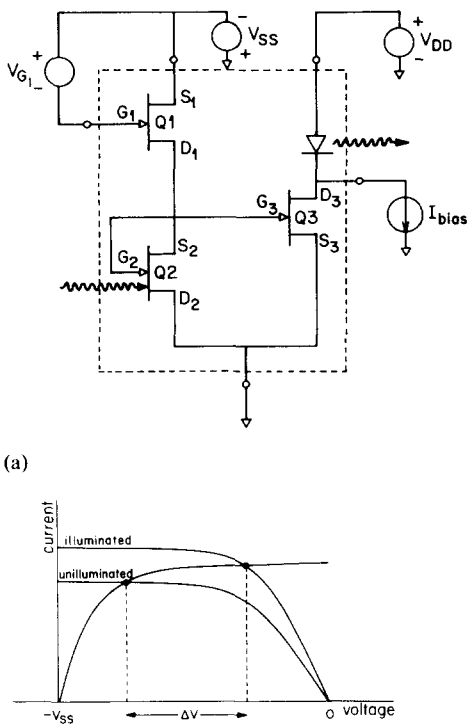

FIG. 2. (a) Schematic diagram of the repeater and external bias sources. (b) I-V curves of the current source Q_1 and the optical detector Q_2. The point of intersection of the curves determines the voltage that appears at the gate of Q_3.

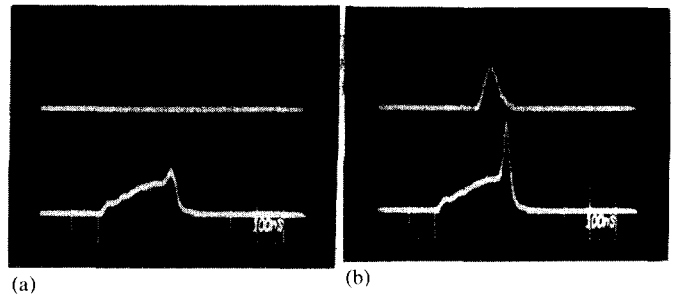

FIG. 3. Response of the repeater with (a) no optical input, and (b) optical input from a GaAlAs laser. The upper traces correspond to the current through the external laser in relative units. The lower traces correspond to light from one of the laser facets from the repeater. The scale in the lower traces is 350 μW/div.

using a pulser to supply V_{DD}, and by using an n-channel Si VFET as a current source to supply the laser bias. The gate voltage of the VFET was adjusted to bias the laser just above threshold for the duration of the power supply pulse. The response of the laser in the absence of an optical input pulse can be seen in Fig. 3(a).

Light was introduced to the detector from an external GaAlAs laser by means of an optical fiber. The excitation of the external laser was timed to synchronize with the application of the power supply pulse to the repeater. With 140 μW of the optical power incident on the active area of the detector, an increase in the light output from one of the laser facets of about 700 μW was observed, as can be seen in Fig. 3(b). This corresponds to an overall optical gain of about 10 dB when light from both laser facets is considered.

Although thermal effects prevented operating the repeater in a cw mode, it is felt that power dissipation will not remain a serious difficulty in future integrated optical circuit designs. By replacing the laser with one possessing a lower value of threshold current, cw repeater operation should be attainable. Lasers with the heat sink connected to the semi-insulating substrate, an obvious requirement for integrated optical circuits, have been successfully operated up to 110 °C.[7] This leads us to believe that power dissipated in the electronic portion of an integrated optical circuit will not seriously degrade the laser performance.

In conclusion, we have demonstrated the feasibility of an integrated optical repeater consisting of a detector, electronic amplifier, and a laser fabricated on a single crystal. Extensions of this basic configuration should find application in optical fiber communication systems and in the interfacing of high speed electronic circuits.

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The influence of annealing ambient on the shrinkage kinetics of oxidation-induced stacking faults in silicon

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The shrinkage behavior of oxidation-induced stacking faults (OSF's) during an annealing in nitrogen, argon, and hydrogen is studied as a function of both annealing temperature and time. Independent of the used gas atmosphere, the OSF shrinkage rate is characterized by an activation energy of 4.9 eV. To explain the different experimental results, an interstitial model for the stacking fault shrinkage is proposed.

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The role of crystal defects in degrading the electrical performance of bipolar MOS and CCD structures has been thoroughly investigated during the last years. Many of these investigations are concentrated on the influence of oxidation-induced stacking faults (OSF's).[1–4] Due to the strong impact of these OSF's on yield hazards in VLSI circuits, the use of different techniques in order to eliminate the OSF's is becoming very important. A complete elimination of the OSF's can be obtained by either suppressing the fault nucleation in the beginning of the processing or implementing a process step which results in the shrinkage of existing stacking faults. This report deals with the shrinkage behavior of the OSF's during an anneal in an inert gas ambient.

The first experimental observation that a high-temperature treatment may result in a shrinkage of the OSF's is reported by Sanders and Dobson[5] for an anneal in vacuum. Later on it was noticed that, dependent on the oxidation temperature, an OSF shrinkage can also be obtained by adding an appropriate amount of chlorine to the oxidizing ambient.[6–8] In order to obtain a sufficiently high shrinkage rate, high oxidation temperatures and/or high chlorine concentrations are needed. For some applications, however, nonoxidizing annealing treatments are preferred. The experiments of Shiraki[6] point out that OSF's also shrink during a high-temperature anneal in nitrogen. After a discussion of the different experimental results available so far in the literature, additional observations of the OSF-shrinkage kinetics due to an anneal in, respectively, argon and hydrogen are reported. To explain the OSF shrinkage, the silicon self-diffusion is taken into account.

The silicon wafers used in this work are 10–15 Ω cm n-type (100)-oriented, CZ grown and selected because of their high amount of grown-in defects. A first wet oxidation at 1150 °C for 150 min results in the formation of OSF's, having a surface length of 52 μm. With this oxide layer left intact, the wafers are annealed for different times at 1100 and 1150 °C in, respectively, nitrogen, argon, and hydrogen. The N_2 anneal has also be done at 1200 °C. After stripping the SiO_2 layer, a Wright etch is used to reveal the OSF's. Experimental results of the OSF length versus annealing time are shown in Fig. 1. This figure points out that (i) at a fixed temperature, the OSF's shrink faster in nitrogen than in argon or hydrogen and (ii) independently of the temperature, the data for an Ar and a H_2 anneal fall together. Additional experiments point out that stripping the wet SiO_2 layer before the annealing step has no influence on the shrinkage rate

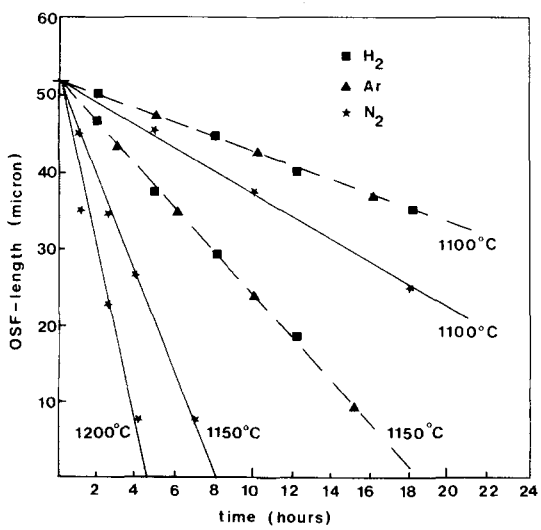

FIG. 1. The shrinkage of the OSF's during an anneal at 1100, 1150, and 1200 °C in nitrogen, argon, and hydrogen.

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