A multi-context holographic memory recording system for Optically Reconfigurable Gate Arrays

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Abstract

Optically Reconfigurable Gate Arrays (ORGAs) offer the possibility of providing a virtual gate count that is much larger than those of currently available VLSIs by exploiting the large storage capacity of a holographic memory. The first ORGA was developed to achieve rapid reconfiguration and a number of reconfiguration contexts; it consisted of a gate array VLSI, a holographic memory, and a laser diode array. The ORGA achieved a 16 μs to 20 μs reconfiguration period that was faster than that of FPGAs, with 100 reconfiguration contexts. However, the ORGA requires the gate array to halt during reconfiguration. Therefore, the ORGA can not be reconfigured frequently because of the associated reconfiguration overhead.

On the other hand, new ORGA-VLSIs that have less than 10 ns reconfiguration capability without any related overhead have already been fabricated. However, to date, a multi-holographic reconfiguration system that is suitable for such rapidly reconfigurable ORGA-VLSIs without any overhead has never been developed. For such realization, this paper proposes a four-context ORGA architecture and a multi-context holographic memory recording system used for it. In addition, experimentally demonstrated results of recording a holographic memory and reconfiguring an ORGA-VLSI are described.

1 Introduction

Field Programmable Gate Arrays (FPGAs) have been used widely in recent years because of their flexible reconfiguration capabilities [1]–[3]. Moreover, demand for high-speed reconfigurable devices has been increasing. If circuit information can be exchanged rapidly between the gate array and memory, an idle circuit can be evacuated into memory; other necessary circuits can be downloaded at that time from memory into the gate array, thereby increasing the gate array's activity. Moreover, such devices offer the possibility of providing a virtual gate count that is much larger than those of currently available VLSIs. However, because FPGA reconfiguration requires more than several milliseconds, FPGAs are unsuitable for dynamically reconfigurable devices.

On the other hand, rapidly reconfigurable devices have been developed: DAP/DNA chips, DRP chips, and multi-context FPGAs [4]-[9]. Those devices package reconfiguration memories and microprocessor arrays or gate arrays onto a chip. The internal reconfiguration memory stores reconfiguration contexts of 4–16 banks. The banks can be changed from one to another on a clock. Thereby, the arithmetic logic unit or gate array of such devices can be reconfigured on every clock cycle in a few nanoseconds. However, increasing the internal reconfiguration memory while maintaining gate density is extremely difficult.

To address such situations, mixed optical and electrical VLSIs [10]–[28] have been developed. In particular, optically reconfigurable gate arrays (ORGAs) [18]–[20] were developed to realize both capabilities of rapid reconfiguration and numerous reconfiguration contexts. An ORGA comprises a gate-array VLSI, a holographic memory, and a laser diode array. The gate array of ORGAs is optically reconfigured using diffraction patterns from a holographic memory that is addressed using a laser diode array. In fact, ORGAs have come to provide a 16 μs reconfiguration period and 50-100 reconfiguration contexts. However, the VLSI architecture never allows the reconfiguration speed to be accelerated. In addition, the gate array can not function during reconfiguration.

We have developed new ORGA-VLSIs that have less-than-10-ns reconfiguration capability without any overhead [21]-[28]. However, up to now, a multi-holographic reconfiguration system suitable for such no-overhead and rapidly reconfigurable ORGA-VLSIs has never been developed.

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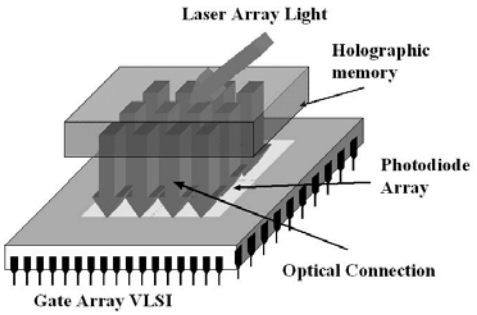

Figure 1. Overview of an ORGA.

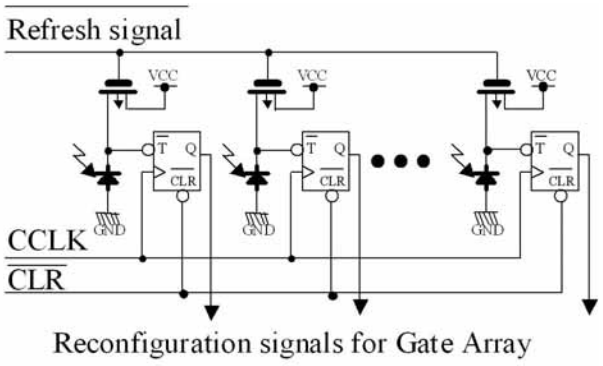

Figure 2. Circuit diagram of an array of optical reconfiguration circuits. Each optical reconfiguration circuit includes a photodiode, a refresh transistor, and a flip-flop; it is placed near and is connected directly to a programming element of a programmable gate array.

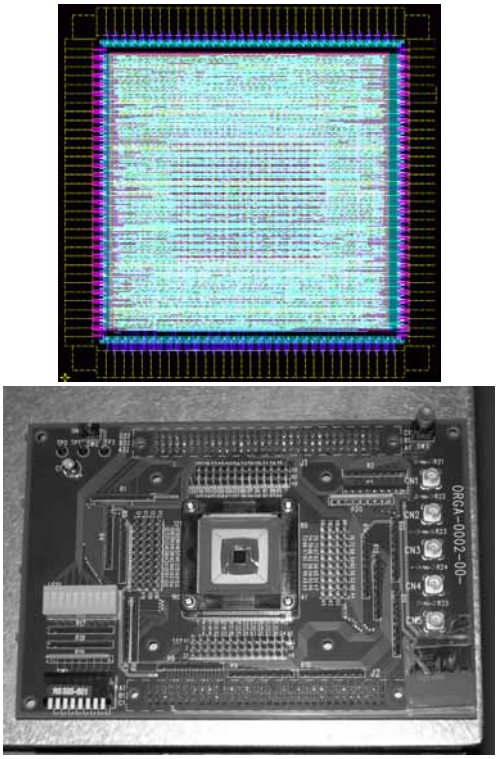

Figure 3. A photograph of an ORGA-VLSI board with a fabricated ORGA-VLSI chip and a CAD layout of the ORGA-VLSI. The ORGA-VLSI was fabricated using a 0.35 μm three-metal 4.9 $\times$ 4.9 mm^2 CMOS process chip. The gate count of a gate array on the chip is 68. In all, 340 photodiodes were used for optical configuration.

For such realization, this paper proposes a four-context ORGA architecture and a multi-context holographic memory recording system used for it. In addition, experimentally demonstrated results of recording a holographic memory and reconfiguring an ORGA-VLSI are shown.

2 ORGA Architecture

2.1 Reconfiguration Architecture

The rapid reconfiguration capabilities of previously proposed OPGAs [18, 19, 20] were not sufficient because of serial transfers between photodiode arrays and programmable gate arrays, as with FPGAs. However, our newly developed ORGA-VLSIs with a perfectly parallel programming capability [21]-[28] allow very-high-speed reconfiguration. In the ORGA-VLSIs, serial transfers were perfectly removed and optical reconfiguration circuits including static memory functions and photodiodes were placed near and directly connected to programming elements of a programmable gate array. An array of optical reconfiguration circuits is shown in Fig. 2. In the reconfiguration procedure, a reconfiguration context is received by photodiodes and is stored instantaneously in toggle flip-flops when a configuration clock (CCLK) is raised. It is then supplied to a gate array of an ORGA-VLSI chip. The toggle flip-flops are used for temporarily storing one context and realizing a bit-by-bit configuration. Using this architecture, the optical configuration procedure for a gate array can be executed perfectly in parallel. Consequently, this architecture never has any overhead for optical reconfiguration.

2.2 Gate array structure

Figure 3 shows that an ORGA-VLSI was fabricated using a 0.35 μm three-metal 4.9 $\times$ 4.9 mm^2 CMOS process chip. The ORGA-VLSI chip consists of four logic blocks,

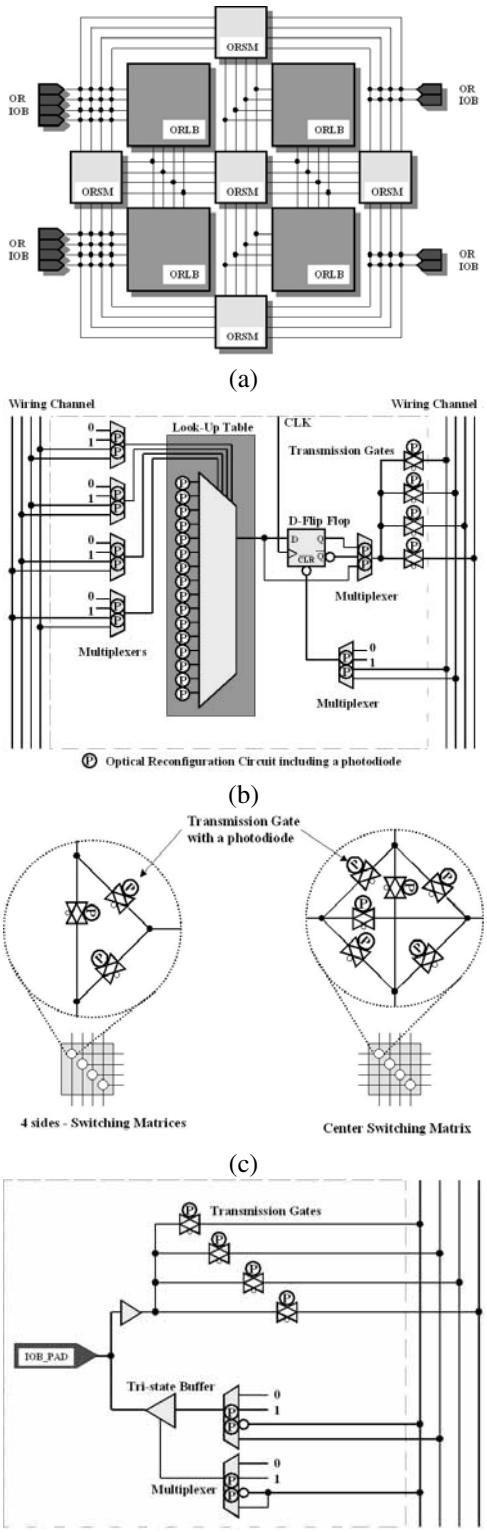

Figure 4. Gate array structure of a fabricated ORGA. Panels (a), (b), (c), and (d) respectively depict block diagrams of a gate array, an optically reconfigurable logic block, an optically reconfigurable switching matrix, and an optically reconfigurable I/O bit.

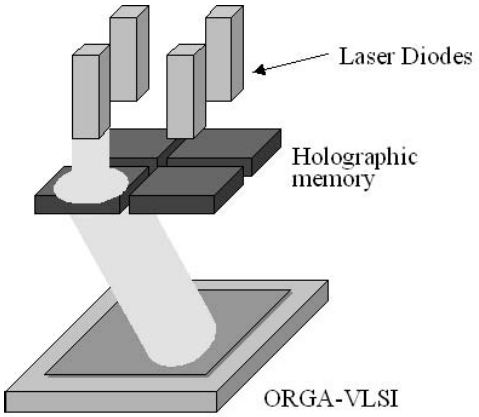

Figure 5. Overview of a four-context ORGA.

five switching matrices, and 12 I/O bits. The gate count of the gate array is 68. The block diagrams of a gate array, a logic block, a switching matrix and an I/O block of the fabricated ORGA-VLSI chip are shown in Fig. 4. In this fabrication, the photodiode size and the distance between the photodiodes were designed, respectively, as 25.5 $\times$ 25.5 μm^2 and 90 μm to ease optical alignment. The total number of photodiodes is 340. Functionality of the VLSI chip is fundamentally identical to that of typical FPGAs. However, each programming element of all blocks of the ORGA-VLSI is connected to an optical reconfiguration circuit to detect an optical configuration context. The logic block consists of a four-input-one-output look-up table (LUT) and a delay flip-flop with a reset function. These functions are optically reconfigurable using 40 optical reconfiguration circuits. Similarly, switching matrices can be reconfigured optically through 12–24 optical connections. Each I/O block is also controlled through nine optical connections. Thereby, the VLSI part can achieve a perfectly parallel configuration.

2.3 Four-context optical system

In the previously proposed ORGA-VLSI with reconfiguration overhead [18]–[20], photodiode arrays and gate arrays were implemented on a different area. Therefore, the illumination from a holographic memory can be concentrated only onto a limited area. However, because these new ORGA-VLSIs without any reconfiguration overhead [21]–[28] have a uniformly distributed photodiode layout style, the illumination from a holographic memory must be dispersed to a larger area than that of the previously proposed one. Therefore, the previously proposed optical system can not be applied directly onto new ORGA-VLSIs. In this paper, as the first step to realize numerous contexts on new ORGA-VLSI, a four-context optical system is proposed as shown in Fig. 5.

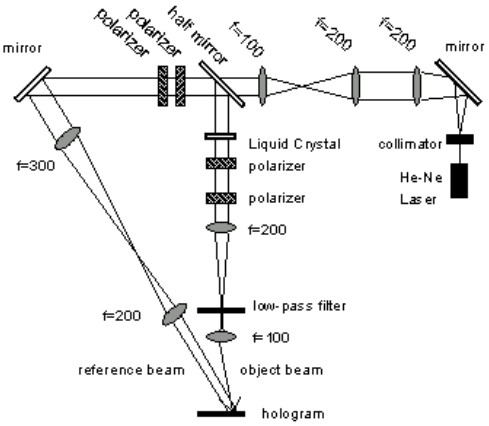

Figure 6. Multi-context holographic memory recording system.

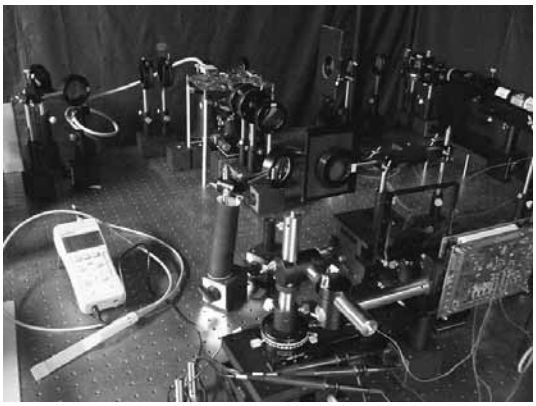

Figure 7. Photograph of the experimental system.

The ORGA optical system comprises four laser sources, an optical holographic memory with four recording regions, and a new ORGA-VLSI. The holographic memory can store four reconfiguration contexts. Each reconfiguration context is addressed using a laser array that is mounted on top of the holographic memory. The diffraction pattern from one region of the holographic memory is receivable on a photodiode-array that is implemented in a gate array of the ORGA-VLSI as a reconfiguration context. Therefore, this architecture enables four different perfectly parallel reconfigurations.

3 Experimental system

A multi-context holographic memory recording system and optical reconfiguration system were constructed to demonstrate a part of the four-context ORGAs explained above.

3.1 Multi-context holographic memory recording system

Figure 6 shows a multi-context holographic memory recording system. A photograph of the experimental system is shown in Fig. 7. A He-Ne laser was used as a light source instead of semiconductor lasers; its respective power and wavelength were about 20 mW and 633 nm. The laser light was collimated and the parallel light beam was divided into two parallel beams: a reference beam and an object beam. The object beam is incident to a liquid crystal television panel that displays a context. The intensity distribution of a context is made for the outgoing beam through a liquid crystal television panel and the first polarizers. The outgoing beam's light intensity is adjusted appropriately using the second polarizer because adjusting the ratio of the light intensities of the object beam to the reference beam is an important for recording holographic memories. On the other hand, the reference beam is incident to a holographic memory after adjustment of the intensity through two polarizers. The angle between the reference wavefront and the holographic memory plane was designed to be 20 degrees. In addition, the distance between an ORGA-VLSI and a holographic memory was designed as 100 mm. Here, it is extremely important that a holographic memory was not placed at the optical axis of the center of the liquid crystal television panel and was placed instead at 1-cm distance from the optical axis. Since the diameter of each interference fringe of a holographic memory is 1.5 cm, the 1 cm offset proves that four contexts can be recorded on a holographic memory as shown in Fig. 5. Similarly, in turn, different contexts are displayed on the liquid crystal television panel and programmed respectively onto the upper-left shift area, the upper-right shift area, the lower-left shift area, and the lower-right shift area of a holographic memory. Finally, using this multi-context holographic memory recording system, we can obtain a four-context holographic memory for a new ORGA-VLSI without any reconfiguration overhead.

3.2 Optical reconfiguration system

Figure 8 shows that an optical reconfiguration system is constructed using only a reference beam-optical system of the multi-context holographic memory recording system. The reference beam is applied onto a recorded holographic memory with the same angle as that used when the holographic memory is recorded. The ORGA-VLSI was placed at 100 mm behind the holographic memory.

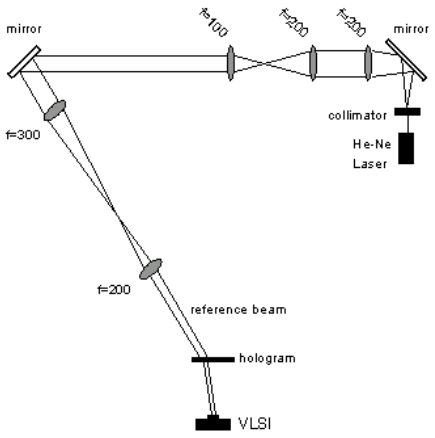

Figure 8. Optical reconfiguration system using the multi-context holographic memory recording system.

4 Experimental Results

Using the multi-context holographic memory recording system and the optical reconfiguration system, a recording experiment of a holographic memory and reconfiguration experiment were executed. Here, as the hologram material, silver film PFG-03 was used as provided by Chuo Precision Industrial Co., Ltd. The hologram material is 12.7 cm $\times$ 10 cm. The coating thickness is 6–7 μm. In this experiment, the light intensities of reference and object beams were adjusted respectively to $750nW/cm^2$ and $30nW/cm^2$. The exposure time is 50 s. A context used for recording, which works as a two-bit up-counter, and a photograph of the holographic memory recording the context are shown in Fig. 9. After recording a holographic memory, we executed an optical reconfiguration that can be completed in less than 66.3 μs. In addition, the correct function of the two-bit counter was demonstrated on an ORGA-board, as shown in Fig. 11. At that time, as shown in Fig. 10, the contrast of a context generated from the holographic memory was good. This confirmed reconfiguration period of 66.3 μs is not superior to the 16 μs of the previously proposed ORGA with reconfiguration overhead. However, this reconfiguration of our proposed system using a new ORGA never requires any reconfiguration overhead and the gate array can function during reconfiguration. That advantage is extremely large when dynamically reconfiguring the gate array. In addition, because our constructed optical reconfiguration system is shared with the multi-context holographic memory recording system, the laser power was not exploited effectively. The reconfiguration speed can easily overcome the 16 μs reconfiguration period of previously proposed ORGAs with reconfiguration overhead if we construct a dedicated optical

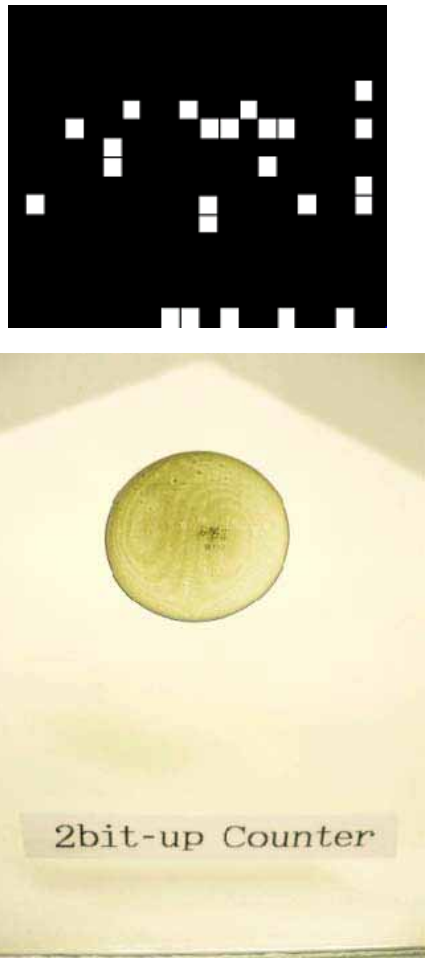

Figure 9. Sample context of a two-bit up-counter and the photograph of a holographic memory recorded with the context.

reconfiguration system.

In addition, the result shows the possibility of a four-context holographic memory recording and reconfiguration systems. Of course, this multi-context holographic memory recording system and optical reconfiguration system are applicable to a larger number of contexts.

5 Conclusion

To date, new ORGA-VLSIs that have less than 10 ns reconfiguration capability without any overhead have been fabricated. However, a multi-holographic reconfiguration system suitable for such rapidly reconfigurable ORGA-VLSIs without any overhead has never been developed. Therefore, this paper has proposed a four-context ORGA architecture and a multi-context holographic memory recording system used for it. Using the proposed system, the

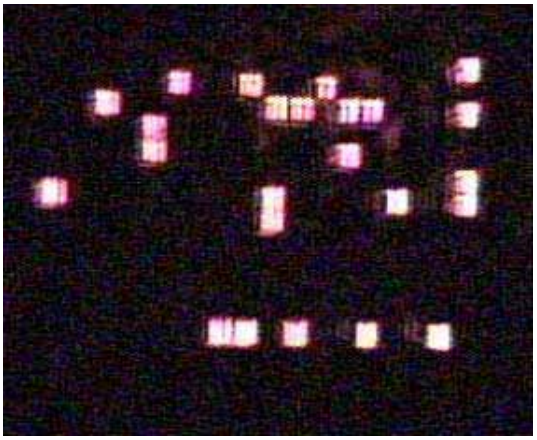

Figure 10. CCD image reconstructed from the holographic memory shown in Fig. 9.

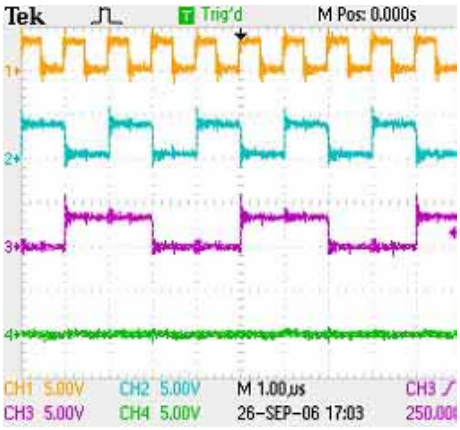

Figure 11. Experimental result of configuration of a two-bit up-counter. The first, second, and third signals of the waveform respectively show a 250 kHz clock, the lower bit of the counter, and the upper bit of the counter.

possibility of realizing a four-context holographic memory recording capability and a four-context reconfiguration capability was confirmed. Experimentally demonstrated results of recording one of four contexts onto a holographic memory and reconfiguring an ORGA-VLSI represent not only the realization of a four-context ORGA but also the possibility of ORGAs with even more numerous contexts.

In addition, we have confirmed that the reconfiguration period of the implementation of a two bit up-counter is less than 66.3 μs without any overhead. Therefore, this architecture allows a gate array to be reconfigured frequently at 15.1 kHz while using its gate array, thereby maximally exploiting the gate-array capability. Of course, the confirmed reconfiguration period is not good: it is slower than the 16 μs to 20 μs of a previously proposed ORGA. However, the new optical reconfiguration systems are shared with the multi-context holographic memory recording system. In the future, when a dedicated optical reconfiguration system is constructed, the reconfiguration speed will be able to surpass that of the 16 μs reconfiguration easily. This remains as a subject for future work.

6 Acknowledgment

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