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A Multi-Level Phase Continuous FSK Modulator

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LINCOLN LABORATORY

A MULTI-LEVEL PHASE CONTINUOUS FSK MODULATOR

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ABSTRACT

A phase continuous FSK modulator has been instrumented using digital techniques. The system allows for the selection of operating modes using multi-frequency level operation along with variable signaling rates. The principal feature of this modulation technique is its property of yielding a spectrum with a narrower bandwidth than conventional FSK at a given keying rate.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

CONTENTS

A MULTI-LEVEL PHASE CONTINUOUS FSK MODULATOR

I. INTRODUCTION

The modulator under discussion is capable of generating phase continuous FSK waveforms in several multiple frequency level modes of operation. In addition to conventional binary where N = 2, N may be selected as 4, 6, 8 or 10. An interesting property of phase continuous FSK is that the power spectrum associated with the output waveforms yields a half-power bandwidth occupancy advantage vis-à-vis conventional FSK. That is, in conventional binary FSK, the half-power bandwidth of the power spectrum is $\frac{1}{T}$ where T is the chip (pulsed sinusoid) duration. For phase continuous binary FSK the bandwidth is $0.595\,(\frac{1}{T})$. This bandwidth advantage extends to the N-ary cases. The results of preliminary tests performed on the Lincoln modulator yield the results shown in Fig. 10. These waveforms are the output voltage spectra generated by the modulator when the data inputs were keyed by a pseudo-random data stream. The results compare favorably with those discussed by B. E. White* in "Spectra of Phase Continuous FSK Waveforms."

Because of the bandwidth feature of phase continuous FSK power spectrum, the attractiveness of this modulation scheme for transmission over a phase-stable channel becomes apparent. In addition, undesirable transients are avoided by the absence of phase discontinuities. These characteristics are of great concern in high power, low-frequency communications systems where antenna bandwidth considerations are paramount.

This design allows for 2-phase switching at zero-crossings only. That is, switching between successive chips occurs at zero-crossings of the sinusoids. The chips are orthogonal with respect to each other. The center of output power spectrum is 45 Hz. The signaling rate is selectable such that

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* Private communication

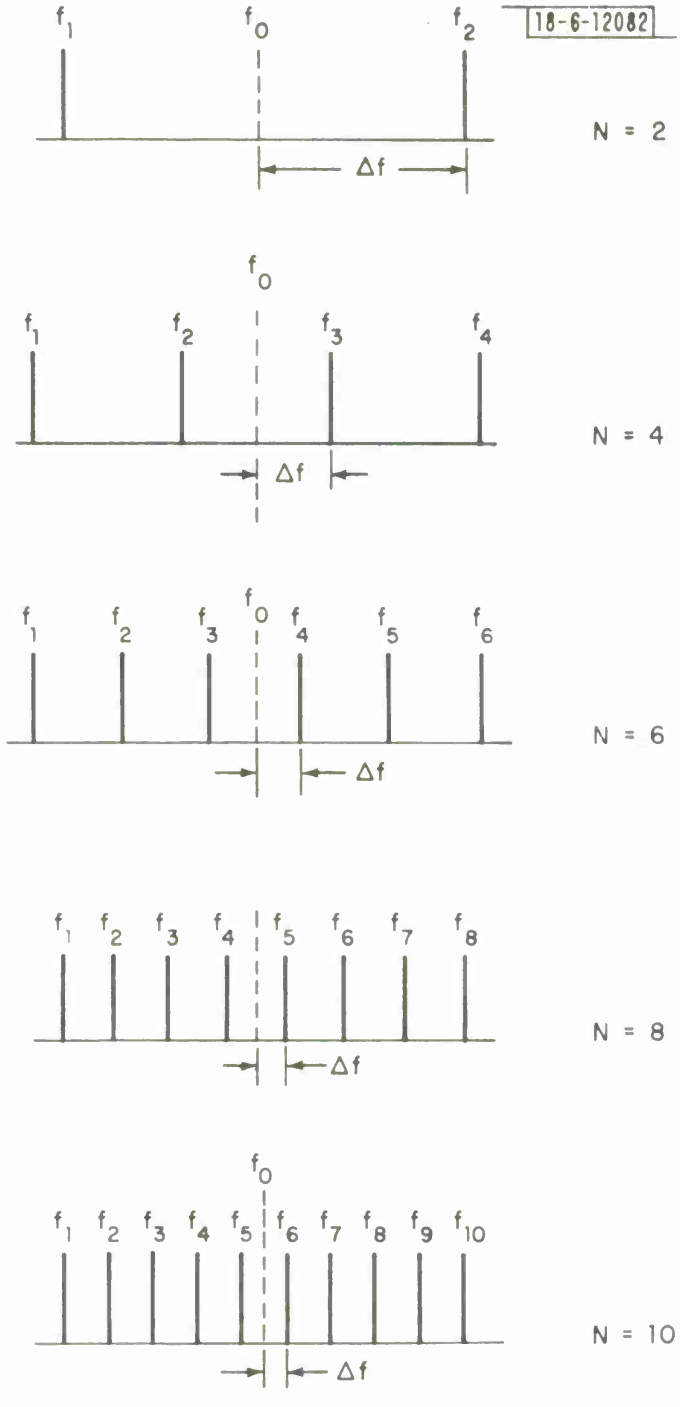


Fig. 1. Transmission spectra.

the bandwidth of the resulting output spectrum varies from less than 1 to 22 Hz depending on the signaling rate (f_m) and N selected. The spectrum center was arbitrarily selected at 45 Hz. Although the output is band limited at 75 Hz, operating modes with bandwidths in the region of 4 to 12 Hz were the only areas evaluated.

The modulator is a self-contained unit with a parallel data input interface. It generates the system clock waveform as well as a center frequency (an ancillary output for reference purposes). A frequency source with good long term stability characteristics as well as stable phase characteristics should be employed to drive the modulator.

The unit is contained in a rack-mountable chassis with 5-1/4" panel height. The circuitry is all solid-state, consisting mainly of monolithic integrated circuitry with some discrete component circuitry. Point-to-point wire-wrapping techniques have been employed throughout, with a state-of-the art I. C. packaging panel containing most of the circuitry.

II. FREQUENCY AND PHASE CONSTRAINTS

The waveforms generated consist of orthogonal chips of duration, T, and initial phases of 0 or π. The chips are contiguous and phase continuous with equal frequency separation between adjacent chip frequencies. See Fig. 1.

This report contains a cursory treatment of the subject of phase continuous FSK spectra with major emphasis on the design of this modulator. An extensive treatment of this subject is given by White.

The minimum frequency spacing consistent with preserving orthogonality is $\frac{1}{2T}$, where T is the chip interval. For the N-ary case, the expression for the selected angular frequency is given by

$$\omega_K = \omega_o + (2K - N - 1)\,\Delta\omega \qquad (1)$$

where

ω_K = angular frequency of the pulsed sinusoid

ω_o = angular center frequency of the output spectrum

K = spectral line designation (from lower to higher magnitudes)

N = frequency level of operating mode

$\Delta\omega$ = one-half angular frequency separation between chip frequencies

where

$\omega_o = \frac{K_+ \pi}{2T}$ for zero-crossing switching, K_+ = positive odd integer

$\Delta\omega = \frac{\pi}{2T}$

The preceding indicates the constraints imposed upon a given operating range; i.e., for operating modes with a fixed center frequency and with bandwidths varying between, say, 5 and 15 Hz, only a limited number of signaling rates ($\frac{1}{T}$) may be selected in order to satisfy Equation (1). See Table I.

III. SYSTEM DESIGN

Several approaches to a system design were considered. An iterative mixing approach was rejected because of the mixing and filter component problems introduced by low frequency operation. The design approach pursued consisted of deriving the ten signals of interest digitally from a single stable frequency source. This was accomplished by dividing down in ten separate divider chains. Each chain consisted of 12 storage elements (shift registers). This allowed a basis for a 12 bit linear shift register arrangement which would yield a maximal length of 2^n-1 or 4095. Because of the availability of MSI (medium scale integration) modules, this function could be realized by three dual-in-line monolithic modules, each containing

an equivalent of 55 gates. The inputs to each shift register stage were externally programmable. This provided the operator with the capability of selecting any divisor between 2 and 4095. For the system application, frequencies with accuracies of up to 1 part per 4095 could be realized. See Fig. 2. In order to employ divisors of high magnitude (for better accuracy), the frequency of the source was in the region of 300 kHz.

This design allows for the generation of N frequencies by virtue of the programmable divider chains. See Fig. 3. At the output of each chain a divide-by-two circuit is added. This conditions the digital waveform to a 50% duty cycle. A signal is selected for transmission via a FET analog gate. The switching of these waveforms is controlled by the phase selection logic. Prior to transmission a selected square wave passes through a low pass filter which selects the fundamental component from the pulse train, thus providing a sinusoidal waveform for transmission. The low pass filter is a passive lumped constant configuration with a cut-off frequency of 75 Hz. At 115 Hz the rejection is 60 dB, thus allowing for sufficient 3rd harmonic rejection. The filter has a linear phase response in the region of interest. This selection of a 50% duty cycle waveform prior to filtering becomes apparent due to the absence of even order harmonics, thus providing relief for the filter selectivity requirements.

Each channel contains a phase adjustment network. This provides the capability in compensating for differential phase offsets between channels, thus insuring phase equalization of the output waveforms.

In addition to generating the ten frequencies for transmission (for N=10), a center frequency and a clock waveform are also synthesized. The center frequency is an ancillary waveform which is generated in a manner similar to that of an operational channel. The clock waveform (f_m) is derived from the 10th divider chain. See Fig. 3. The clock is tapped into the 10th channel at twice the frequency of transmission ($2f_{10}$). For operating modes other than N = 10, the 10th chain is set to an identical divisor to that of the channel

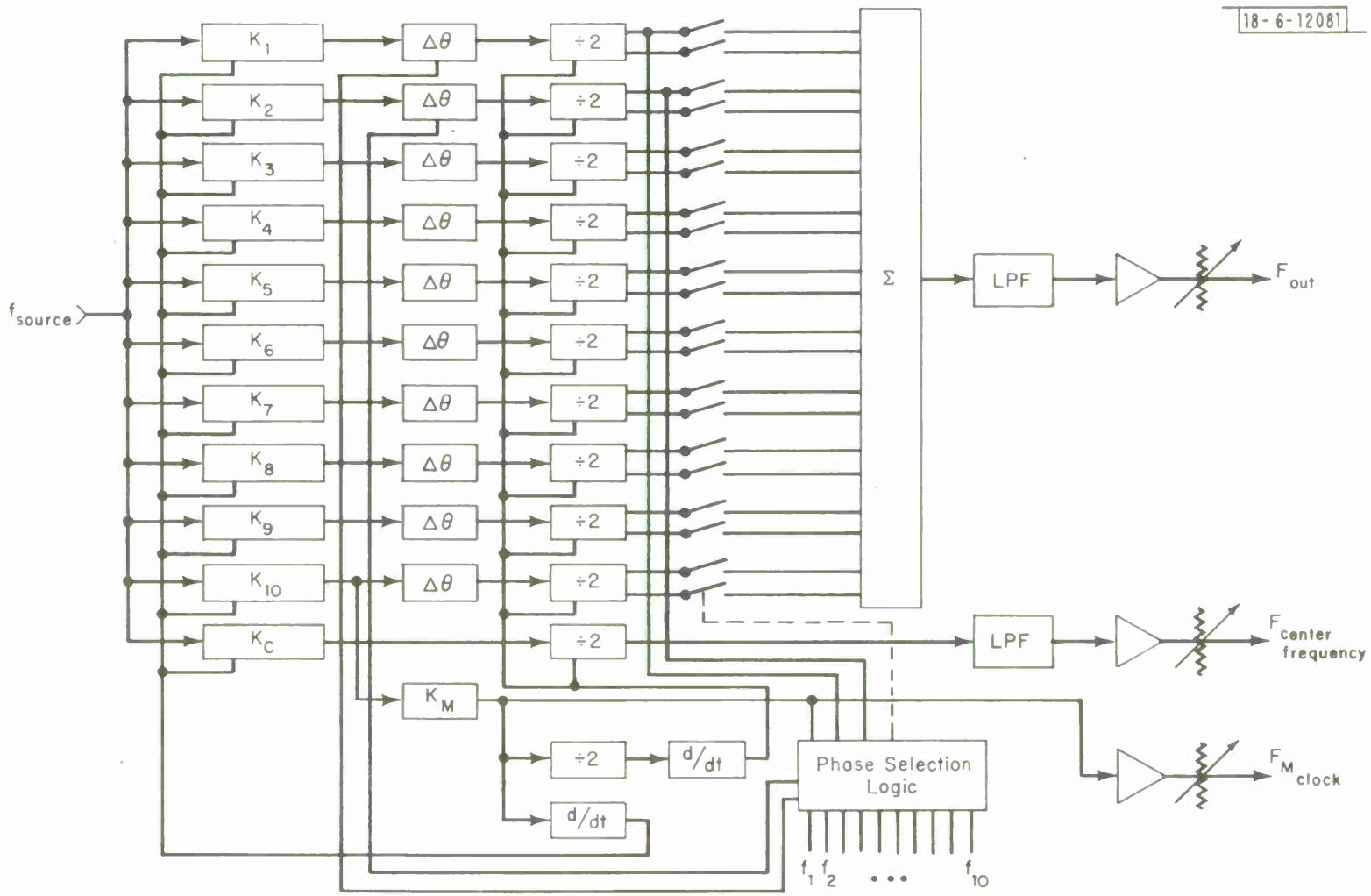


Fig. 2. Modulator block diagram.

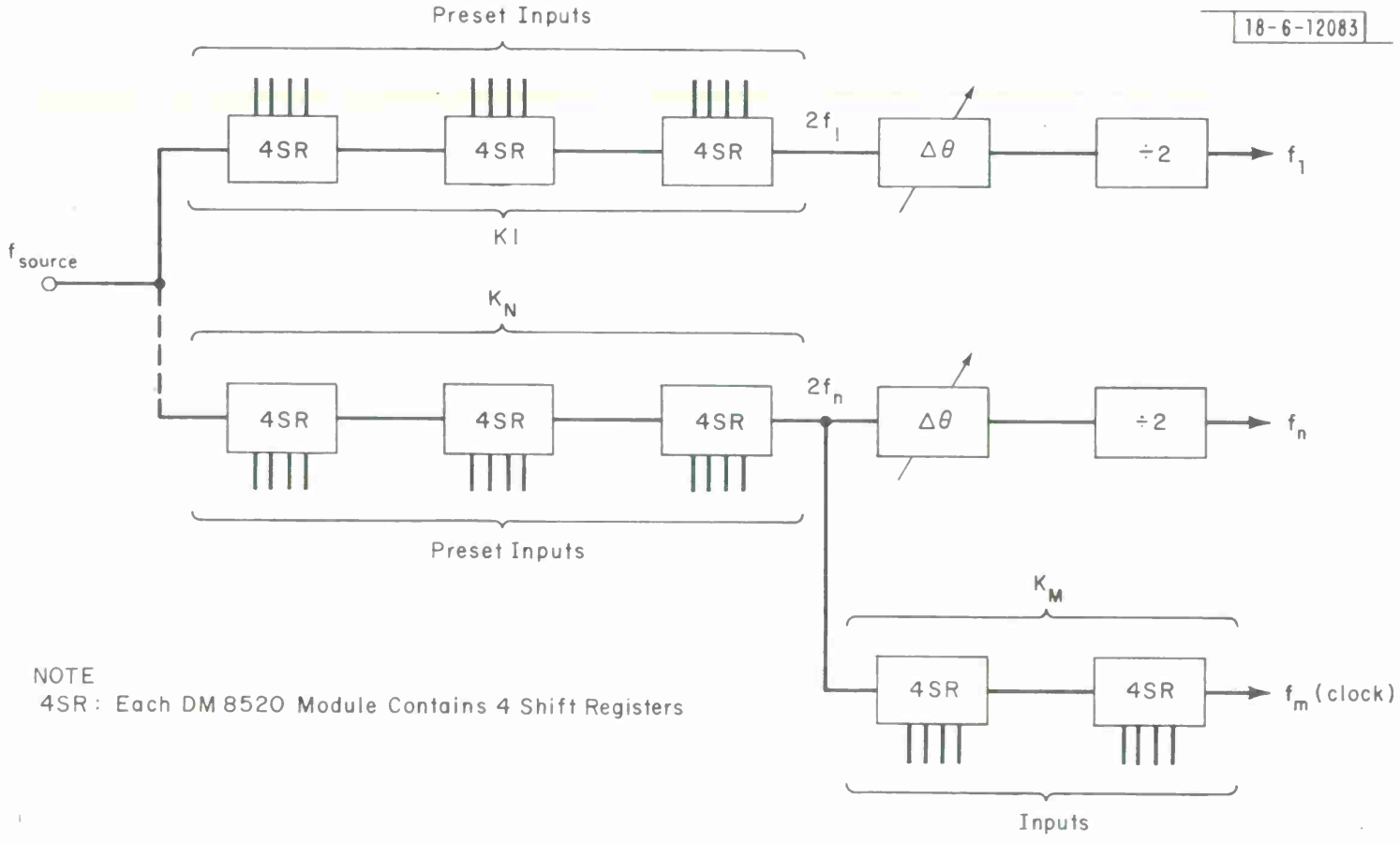


Fig. 3. Frequency divider networks.

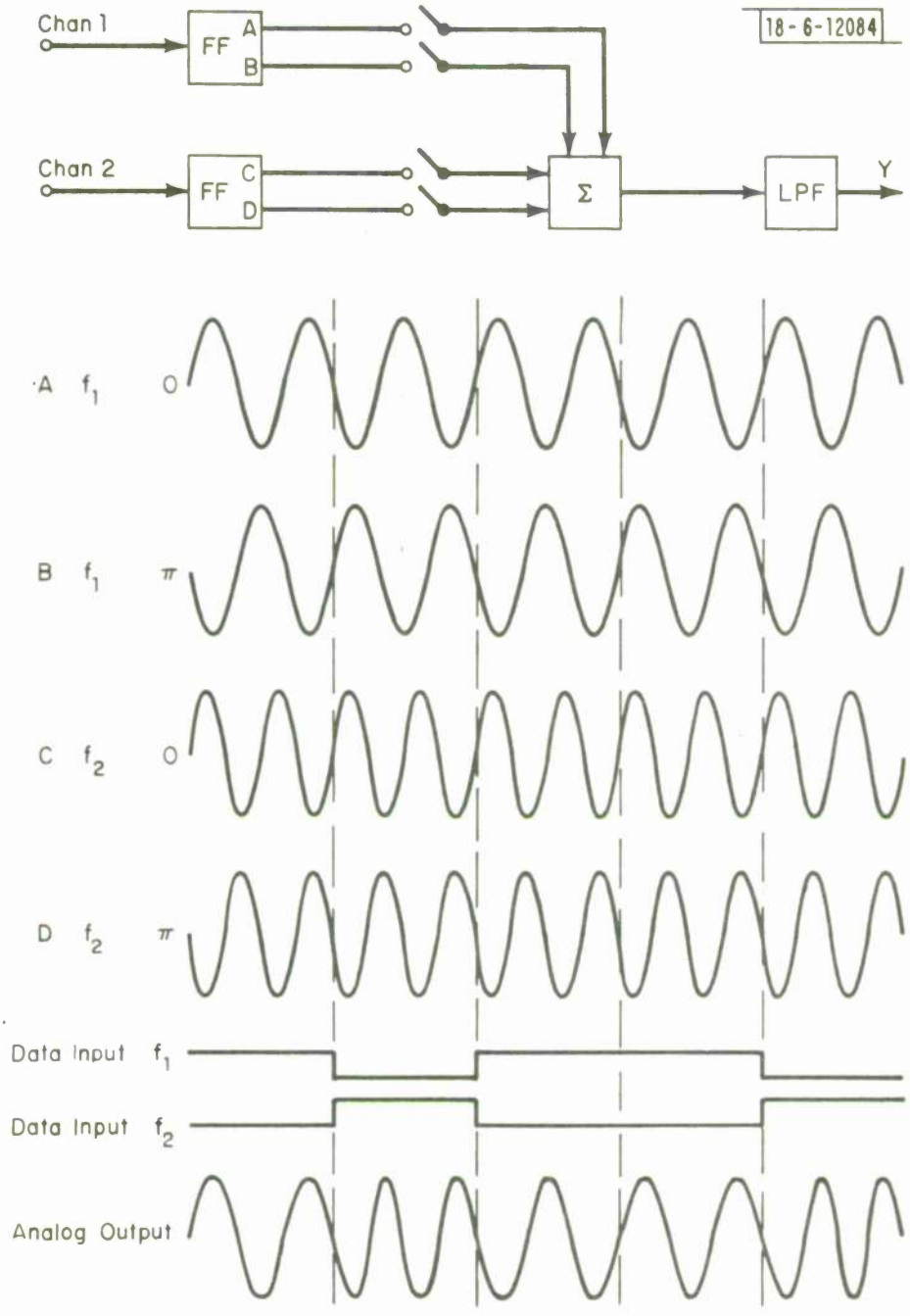


Fig. 4. Transmission waveforms (N = 2).

of the highest transmission frequency; i. e., for N = 6, divisor of the 6th channel is applicable. An additional pair of programmable divider modules is contained in the clock network. This consists of 8 shift register states or a divisor selection ability from 2 to 255. The relationship of the clock frequency and operating frequencies is described in Section V.

The phase selection portion of system is a digital processor which receives the data input at a parallel interface and selects a frequency of transmission in accordance to the data control voltage present. This selected frequency corresponds to the data input on a bit by bit basis, with an initial phase such that phase continuity is maintained between it and the preceding waveform (chip). See Fig. 4.

The phase selection logic also generates a reset pulse which synchronizes all the transmission channels to the clock. Synchronization to the clock waveform is required since the transmission frequencies are generated by an approximation method; i. e., a divisor was selected for minimum frequency offset. However, the "phase run-out" under these conditions would be intolerable without an active synchronization process. This is discussed in greater detail in Section IV.

IV. FREQUENCY SYNTHESIS

The individual transmission sinusoids are generated digitally as shown in Fig. 2. Prior to transmission the fundamental component is selected from f_n by passing the selected chip through a low pass filter. All channels are equalized for phase and gain.

The manner in which the system characteristics are selected for a given operating mode is outlined below. The selectable characteristics are:

N (2, 4, 6, 8 or 10)

K (divisors for each channel, plus the divisors for center frequency channel and clock channel).

The selection of K depends on the bandwidth requirements for a given mode of operation. The following is a representative procedure allowing for the selection of system operating parameters:

a. select the transmission center frequency, f_c (for this discussion 45 Hz is used).

b. for a given bandwidth requirement, W, select the chip duration T, in accordance with $W = 0.595(\frac{1}{T})$. This is for the binary case where $N = 2$.

c. set clock signaling rate, $f_m = \frac{1}{T}$.

d. select K_+ by: $K_+ = \frac{4f_c}{f_m}$.

Since K_+ is constrained to positive odd integers (See Section II), round off K_+ to closest odd integer.

e. compute f_m and T using selected value of K_+.

f. compute separation, $2\Delta f$, of the signaling frequencies by:

$$\Delta f = \frac{f_m}{4}$$

g. set $f_K = f_c + (2K-N-1)\Delta f$ where f_K is Kth signaling frequency of a transmission spectrum.

For example for $N = 4$,

$$f_1 = f_c - 3\Delta f$$

$$f_2 = f_c - \Delta f$$

$$f_3 = f_c + \Delta f$$

$$f_4 = f_c + 3\Delta f$$

h. let $f_{source} = f_1(8000)$; then channel 1 divisor becomes $8000(\frac{1}{2})$ or 4000.

i. set $K_n = f_o(\frac{1}{2f_n})$.

Round off K_n to 4 significant digits*.

Using the preceding method of synthesis,

$$2f_n = \frac{f_{source}}{K_n}$$

$$f_n = \frac{f_{source}}{2K_n}$$

let K'_n = divisor rounded off to 4 significant digits.

$$f'_n = \frac{f_{source}}{2K'_n}$$

$$\frac{f'_n}{f_n} = \frac{K_n}{K'_n} \quad .$$

Since K_n is on the order of 3000, the rounding off process will contribute a maximum error of 0.5 parts per 3000.

This approximation method of synthesis yields a worse case phase error of 2.7^o for frequencies in the region of 45 Hz. This corresponds to a phase offset at the end of a chip interval of $\frac{1}{6000}(45) = 7.5(10)^{-3}$ parts per cycle. This error, however, is removed every $\frac{1}{f_m}$ intervals by resetting the logic of the divider chains with the leading edge of the $\frac{1}{f_m}$ waveform. Since initial phase equalization is to within 1^o, the approximation synthesis

* Because the programmable dividers (linear shift register configuration are limited to 4095, four digit resolution is the limiting factor in this approximation. Since f_1 is the lowest frequency in the transmission spectrum, $K_n \leq 4000$.

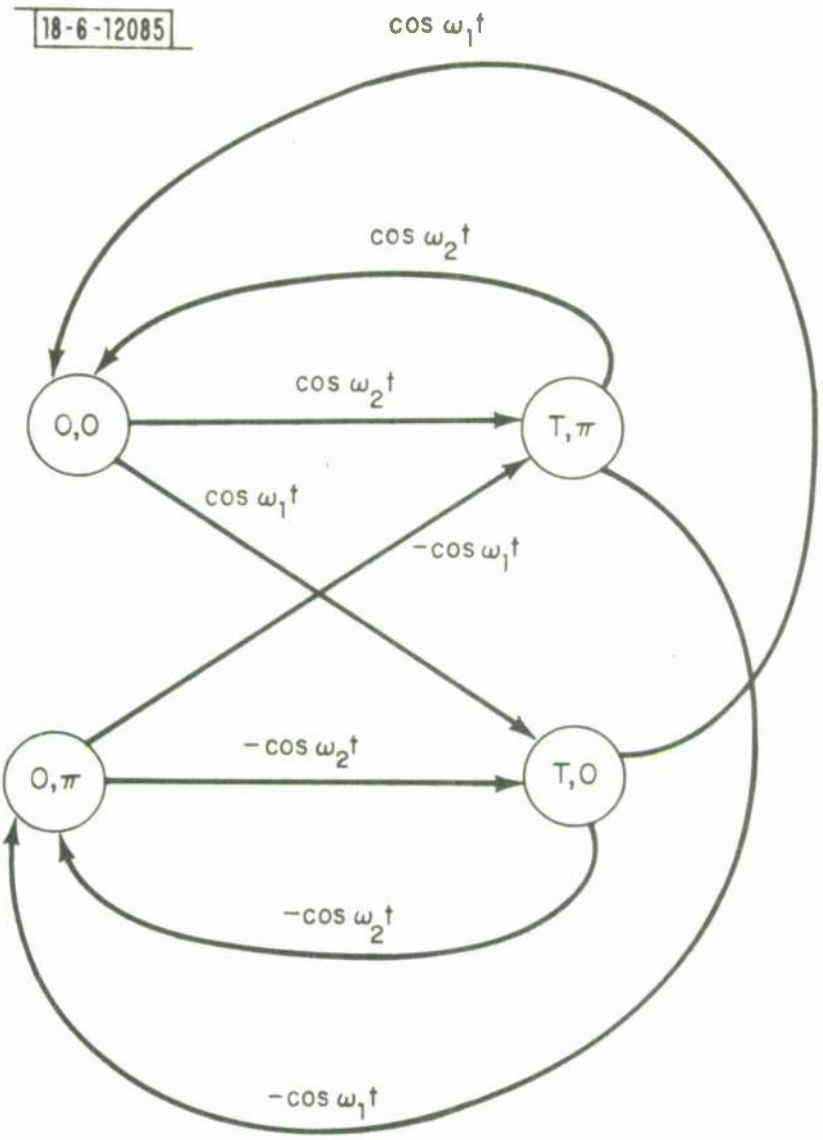


Fig. 5. State diagram (N = 2).

process usually is the major contributor to phase errors in this system.

V. CLOCK PULSE GENERATOR

In this system the clock is generated internally and is derived from the source frequency. The clock, f_m, is available to outside users via a BNC connector. The input data must be synchronous with f_m for proper operation.

As mentioned earlier, the clock pulse is derived from f_{source} by tapping from channel 10 at $2f_{10}$. K_{10} should be set to K_N where K_N is the divisor of the channel of the highest frequency of transmission for a given operating mode. Therefore,

$$f_N = f_c + (2N-N-1)\Delta f$$

$$f_N = \frac{K_+ f_m}{4} + (N-1)\frac{f_m}{4}$$

$$2f_N = 2(K_+ + N-1)\frac{f_m}{4}$$

Thus, the divisor in the clock channel, $K_m = \frac{K_+ + N-1}{2}$.

VI. PHASE SELECTION LOGIC

In order to select the proper phase (0 or π) of a transmitted chip, the state of the preceding chip must be examined. Accordingly, the state (frequency and phase) of the preceding chip is stored with the selection of the next chip being such as described in the state diagram of Fig. 5 which depicts the binary case. Figures 4 and 6 also provide illustrations of the phase continuity of the v(t) output waveform. Notice that both amplitude and phase of the various transmission frequencies have been equalized.

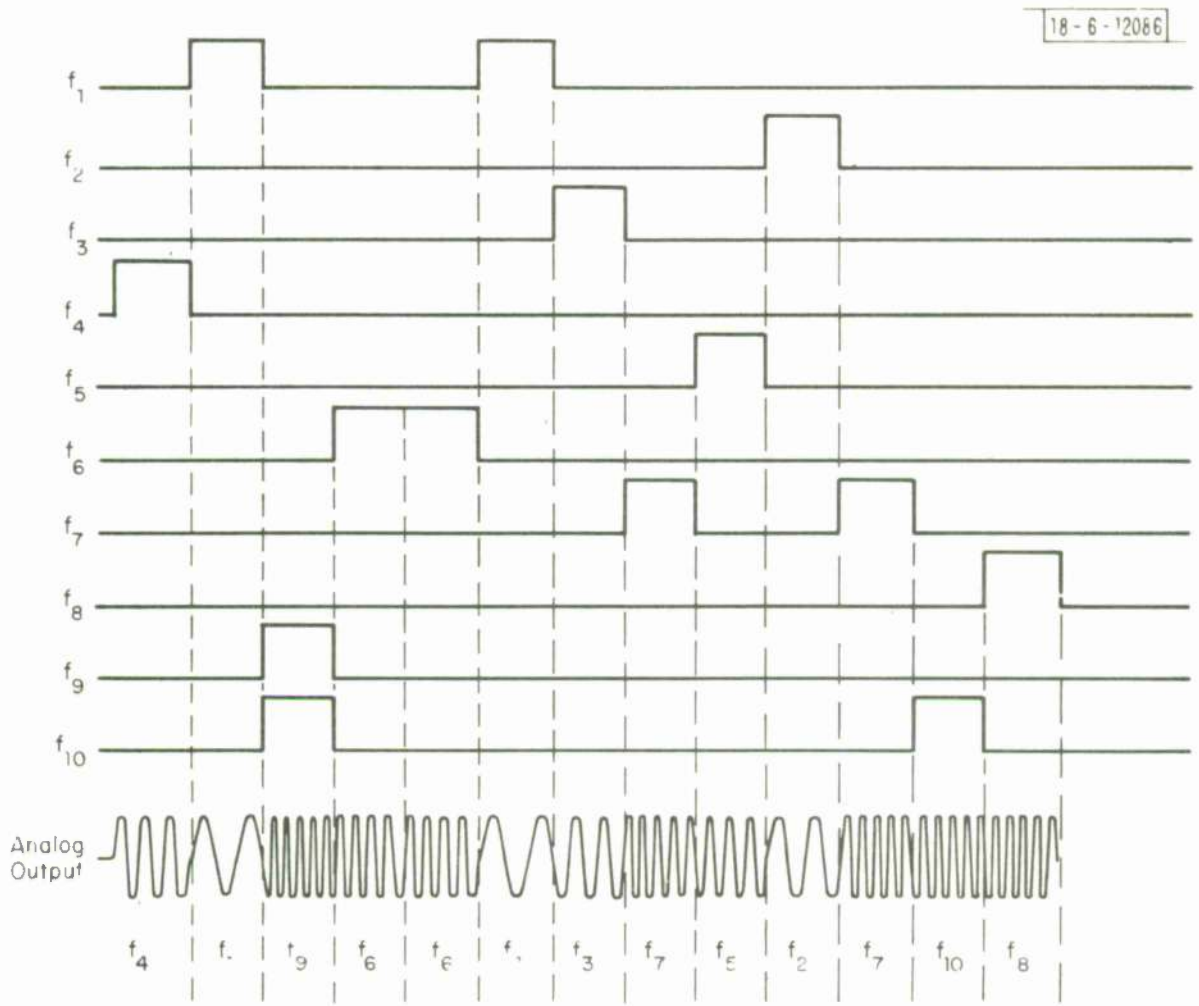


Fig. 6. Transmission waveforms (N = 10).

The relationship between adjacent chips of different frequencies is such that there is a difference in frequency of an integral number of half cycles. As described earlier, the clock pulse, f_m, is derived from f_N. Because of this relationship, the state of a given frequency repeats itself every 2T where T is the chip interval.

VII. PHASE AND AMPLITUDE EQUALIZATION

Prior to operation the modulator should be placed on the standby mode. (The power switch has OFF/STBY/OPER positions available.) In the standby mode each frequency is selectable (via manual switch) on a continuous basis. This allows the operator the opportunity to equalize the amplitude of the twenty signals; i.e., 10 frequencies at 0 and π phases.

Phase is equalized by comparing the phase of each waveform prior to combining with that of the clock. The zero-crossings of each waveform can be readily adjusted to within 20 microseconds of the leading edge of f_m. This results in a phase error of much less than 1^o.

The phase adjustment controls are manual potentiometers with control ranges of 12 milliseconds. The amplitude adjustments are screw-driver controlled to equalize for small offsets*.

VIII. INSTRUMENTATION

The modulator circuitry consists mainly of integrated circuitry. The I.C. packaging panel is a 180 socket capacity dual-in-line panel (Augat Co.). The wire wrap technique uses No. 30 wire with KYNAR insulation. Thumbwheel switches control the programmable inputs to the channel divider

* The phase adjustment controls must be adjusted for every change in operating mode; i.e., N and/or f_m. Amplitude, however, is related to logic levels, since all the waveforms are derived digitally. Therefore, this adjustment should be rarely performed since the logic levels are quite stable.

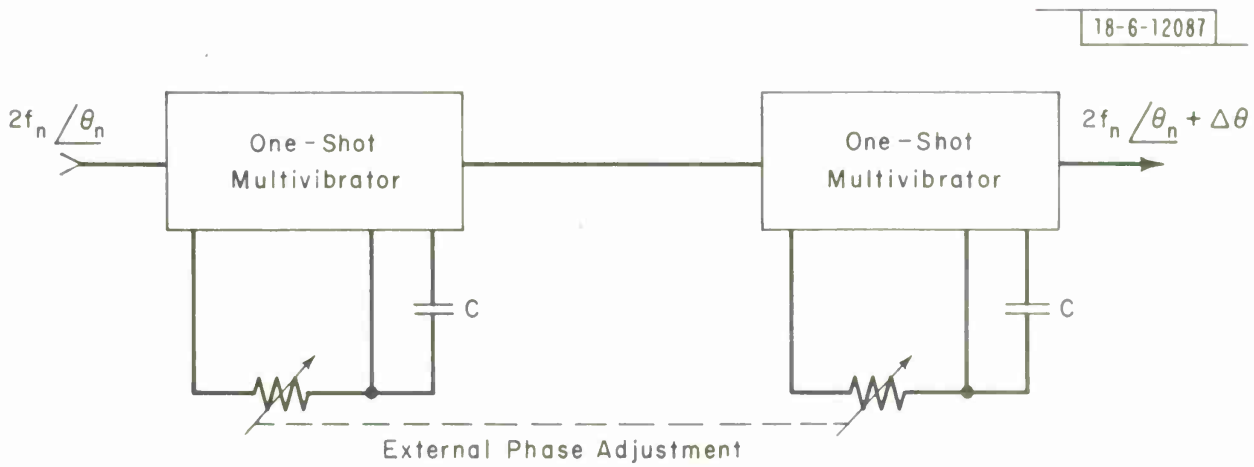


Fig. 7. Phase equalization.

chains. The modulo-N dividers are MSI modules supplied by National Semiconductor Co. (Model DM8520). The remaining digital portions of the system consist of Signetics 8000 series logic.

The phase shifters consist of two cascaded one-shot multivibrators. External capacitors (with low temperature coefficients) and dual-gauge potentiometers control the time constants of the phase shifter. See Fig. 7. These provide from 3 to 15 milliseconds of adjustment.

The analog switches and adder consist of a parallel bank of FET switches followed by an operational amplifier. See Fig. 8.

The unit is self-contained, using its own power supplies. The power dissipation is 75 watts. The frequency source used for preliminary experiments was a Fluke 633A-01 Synthesizer. Although any source with good long term and short term frequency stability characteristics could be used, a synthesizer provides the operator with a readily selectable frequency source. The 633A-01 has a range of 0 to 11 mHz with frequency selection at 0.1 Hz increments. The internal standard has a stability of better than 2 parts per 10^9 per day.

IX. POWER SPECTRA

In order to generate a continuous power spectrum, random keying of the data inputs had to be employed. A data input simulator was designed and instrumented. See Fig. 9. This simulator had the capability of operating in the modes of N = 2, 4, or 8. Some typical power spectra are shown in Figs. 10(a), (b), and (c). The cases of N = 6 and 10 were not evaluated under conditions of random keying. In these cases a repetitive frequency staircase was generated by using a simulator which employed a monotonic keying sequence. The resulting spectra had properties of periodicity consistent with the keying waveforms and signaling frequencies employed.

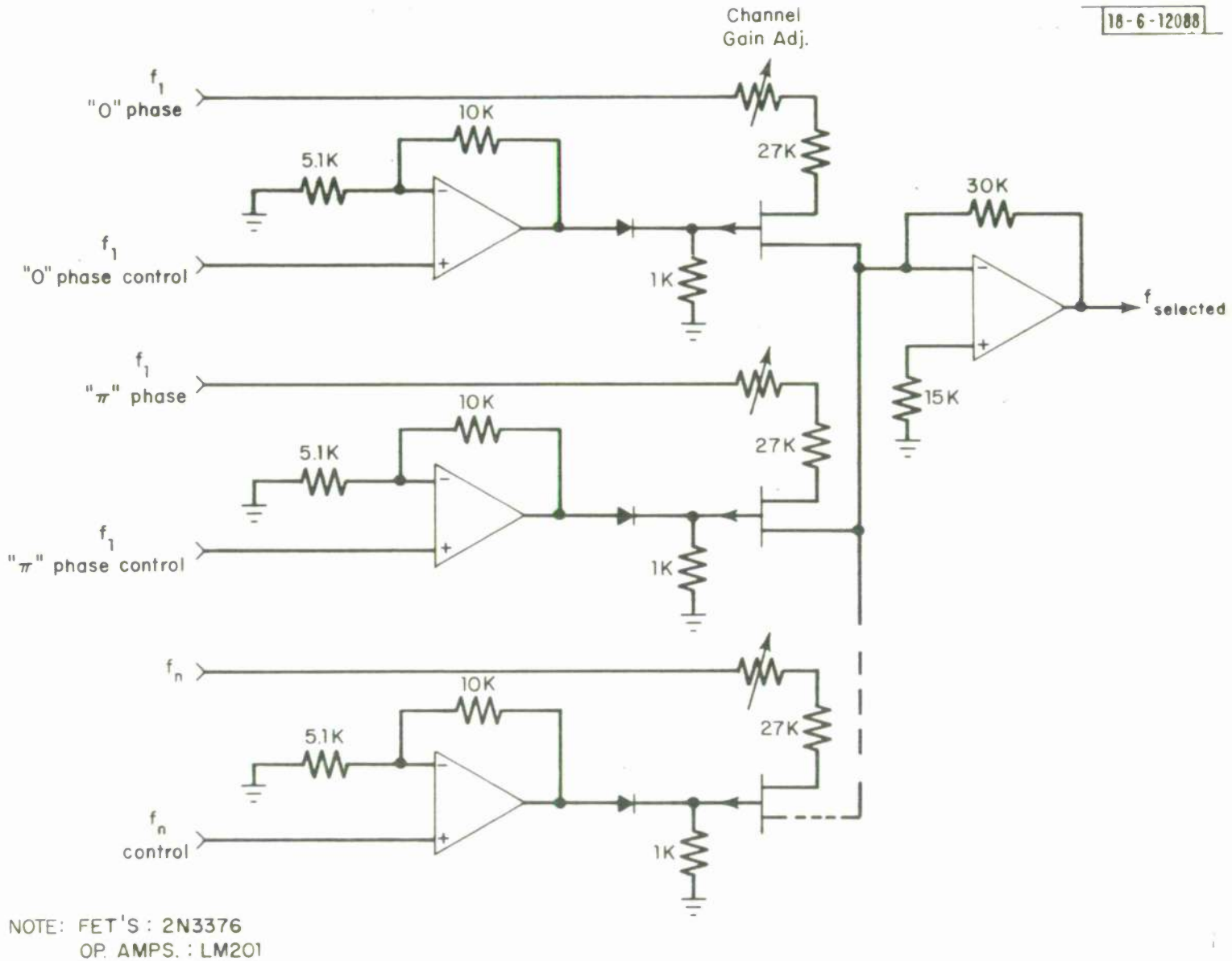


Fig. 8. Analog gate.

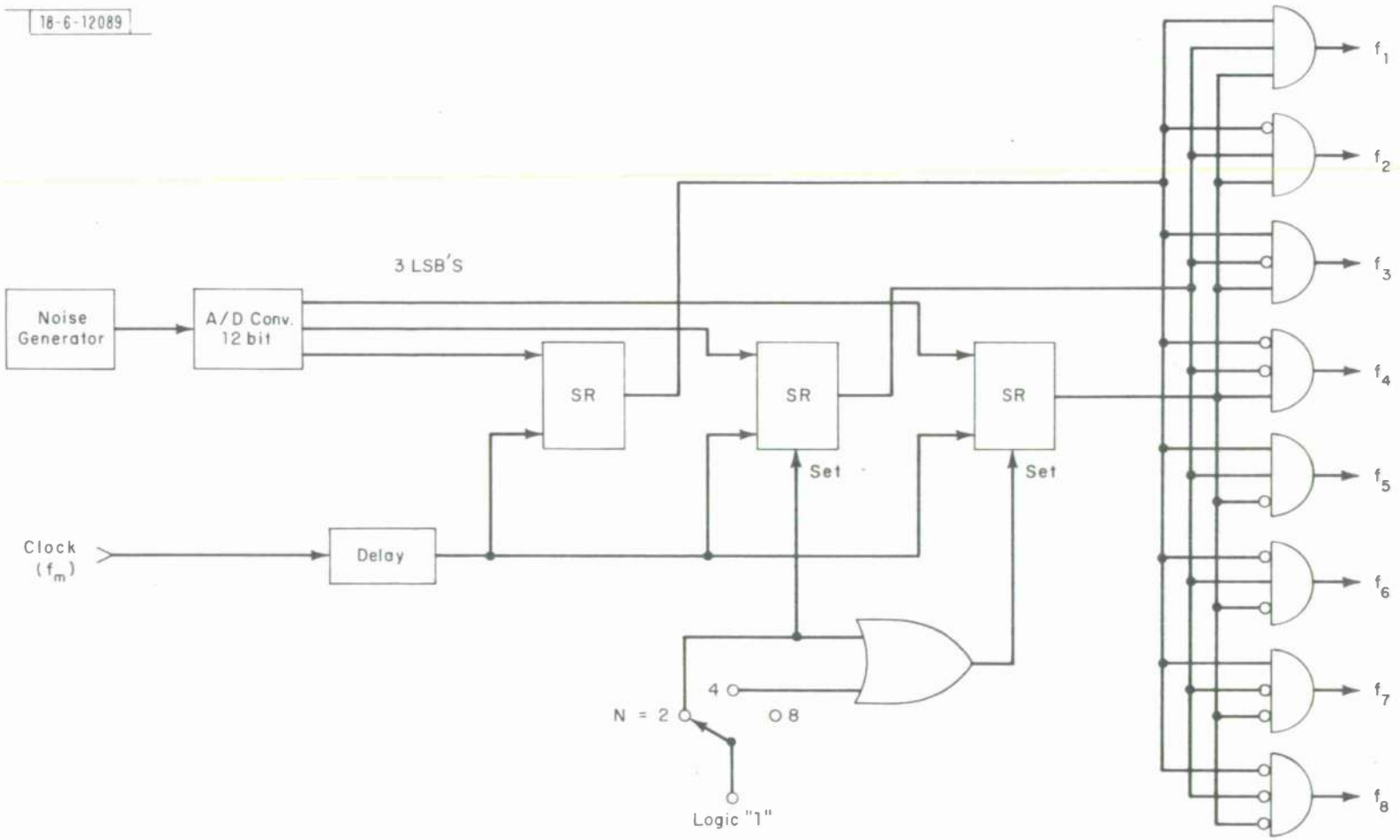


Fig. 9. Random keying generator.

The spectrum analyzer used for these measurements was a Federal Scientific UA-6. The waveforms shown in Figs. 10(a), (b), and (c) are displays of integrated voltage as a function of frequency. Both scales are linear with a spectrum analyzer resolution of 0.2 Hz. The discrete spectral lines on each side of the power spectra are frequency calibration markers.

TABLE I

AVAILABLE OPERATING FREQUENCIES IN 40 TO 50 HZ RANGE

WITH MEAN FREQUENCY OF 45 HZ

N = 2

K_+	Data Rate (f_m)	f_1	f_2
11	16.36	40.91	49.10
13	13.85	41.54	48.46
15	12.00	42.00	48.00
17	10.59	42.35	47.64
19	9.47	42.63	47.37
21	8.57	42.86	47.15
23	7.83	43.04	46.95

N = 4

K_+	Data Rate (f_m)	f_1	f_2	f_3	f_4
31	5.81	40.64	43.56	46.45	49.36
33	5.45	40.91	43.64	46.37	49.10
35	5.14	41.14	43.71	46.28	48.86
37	4.86	41.35	43.78	46.22	48.65
39	4.62	41.54	43.85	46.15	48.46
41	4.39	41.71	43.90	46.10	48.29
43	4.19	41.86	43.95	46.05	48.14
45	4.00	42.00	44.00	46.00	48.00

TABLE I Continued

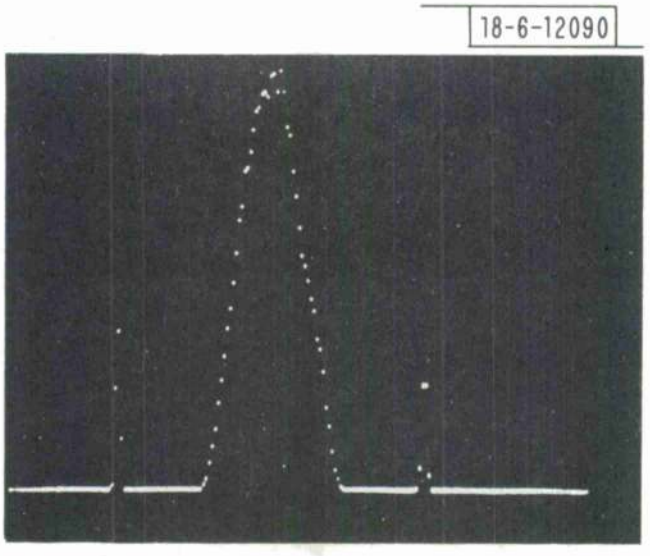
N = 6

K_+	Data Rate (f_m)	f_1	f_2	f_3	f_4	f_5	f_6
45	4.00	40.00	41.99	44.00	46.00	48.00	50.00
47	3.83	40.13	42.13	44.04	45.96	47.87	49.78
49	3.67	40.41	42.24	44.08	45.92	47.75	49.60
51	3.53	40.59	42.36	44.12	45.89	47.65	49.41
53	3.40	40.75	42.45	44.15	45.84	47.54	49.25
55	3.27	40.91	42.55	44.18	45.82	47.46	49.10
57	3.16	41.05	42.63	44.21	45.79	47.36	48.94
59	3.05	41.19	42.71	44.24	45.76	47.29	48.81
61	2.95	41.31	42.79	44.27	45.74	47.21	48.69
63	2.86	41.43	42.85	44.28	45.71	47.14	48.57
65	2.77	41.54	42.92	44.31	45.70	47.08	48.46
67	2.69	41.64	42.98	44.32	45.67	47.01	48.36
69	2.61	41.74	43.04	44.34	45.65	46.95	48.27

TABLE I Continued

N = 8

K_+	Data Rate (f_m)	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8
61	2.95	39.84	41.31	42.78	44.26	45.74	47.21	48.68	50.17
63	2.86	40.00	41.43	42.86	44.28	45.71	47.14	48.57	50.00
65	2.77	40.15	41.53	42.92	44.31	45.69	47.07	48.46	49.85
67	2.69	40.30	41.64	42.98	44.33	45.68	47.01	48.36	49.70
69	2.61	40.43	41.74	43.04	44.35	45.65	46.96	48.26	49.57
71	2.54	40.56	41.83	43.10	44.37	45.63	46.91	48.18	49.44
73	2.46	40.68	41.92	43.16	44.38	45.61	46.84	48.08	49.32
75	2.40	40.80	42.00	43.20	44.40	45.60	46.80	48.00	49.20
77	2.34	40.91	42.08	43.24	44.42	45.58	46.75	47.92	49.10
79	2.28	41.01	42.15	43.30	44.34	45.57	46.71	47.84	48.98
81	2.22	41.11	42.22	43.33	44.44	45.55	46.66	47.77	48.88
83	2.17	41.20	42.29	43.37	44.46	45.54	46.62	47.70	48.79
85	2.12	41.29	42.35	43.41	44.47	45.53	46.59	47.64	48.71
87	2.07	41.38	42.42	43.44	44.48	45.52	46.54	47.59	48.62
89	2.02	41.46	42.47	43.48	44.50	45.51	46.52	47.53	48.53
91	1.98	41.54	42.53	43.51	44.51	45.50	46.49	47.47	48.46



Voltage vs Frequency (linear scales)

N = 2

K_+ = 23

f_c = 45 Hz

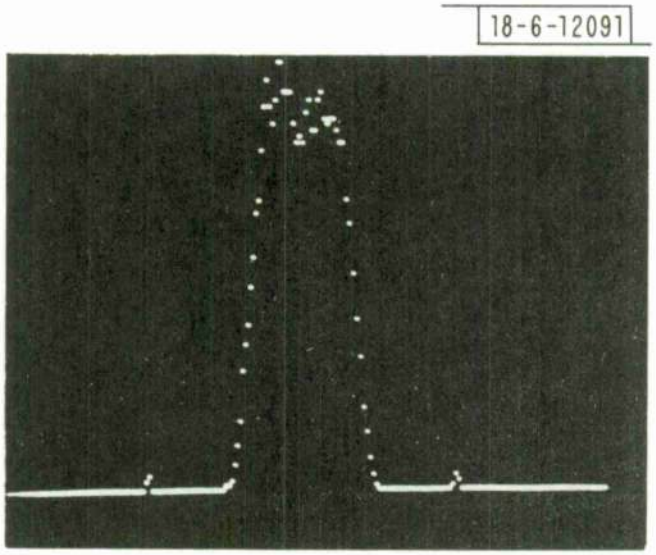
f_m = 7.83 Hz, random keying

Frequency separation = 3.91 Hz

Averaging time = 1280 sec

Calibration signals = 35 and 55 Hz

Fig. 10(a). Voltage spectrum for N = 2.



Voltage vs Frequency (linear scales)

$N = 4$

$K_+ = 45$

$f_c = 45$ Hz

$f_m = 4.00$ Hz, random keying

Frequency separation = 2.00 Hz

Averaging time = 1280 sec

Calibration signals = 35 and 55 Hz

Fig. 10(b). Voltage spectrum for N = 4.

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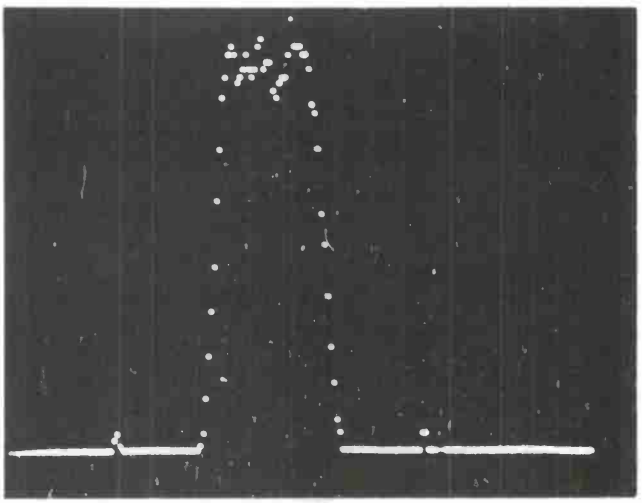

Voltage vs Frequency (linear scales)

N = 8

K_+ = 91

f_c = 45 Hz

f_m = 4.00 Hz

f_m = 1.98 Hz, random keying

Frequency separation = 0.990 Hz

Averaging time = 1280 sec

Calibration signals = 35 and 55 Hz

Fig. 10(c). Voltage spectrum for N = 8.

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13. ABSTRACT

A phase continuous FSK modulator has been instrumented using digital techniques. The system allows for the selection of operating modes using multi-frequency level operation along with variable signaling rates. The principal feature of this modulation technique is its property of yielding a spectrum with a narrower bandwidth than conventional FSK at a given keying rate.

14. KEY WORDS

FSK
modulators
frequency modulation