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A Multi-Mode ULP Receiver Based on an Injection-Locked Oscillator for IoT Applications

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ABSTRACT This paper presents an ultra-low-power receiver based on the injection-locked oscillator (ILO), which is compatible with multiple modulation schemes such as on-off keying (OOK), binary frequency-shift keying (BFSK), and differential binary phase-shift keying (DBPSK). The receiver has been fabricated in 0.18-μm CMOS technology and operates in the ISM band of 2.4 GHz. A simple envelope detection can be used even for the demodulation of BFSK and DBPSK signals due to the conversion capability of the ILO from the frequency and phase to the amplitude. In the proposed receiver, a Q-enhanced single-ended-to-differential amplifier is employed to provide high-gain amplification as well as narrow band-pass filtering, which improves the sensitivity and selectivity of the receiver. In addition, a gain-control loop is formed in the receiver to maintain constant lock range and hence frequency-to-amplitude conversion ratio for the varying power of the BFSK-modulated receiver input signal. The receiver achieves the sensitivity of –87, –85, and –82 dBm for the OOK, BFSK, and DBPSK signals respectively at the data rate of 50 kb/s and the BER lower than 0.1% while consuming the power of 324 μW in total.

INDEX TERMS Ultra-low power, injection-locked oscillator, injection-locking receiver, multi-modulation, frequency-to-amplitude conversion, phase-to-amplitude conversion, wireless sensor node, internet of things, single-ended-to-differential conversion, Q enhancement, envelope detection.

I. INTRODUCTION

As a variety of services and applications based on the internet of things (IoT) have been widely developed, the demands on ultra-low-power wireless techniques for data transmission and reception have grown rapidly. The capability of performing wireless communication with little power consumption is a key factor enabling the operation of wireless sensor nodes for IoT [1]. As the complexity and scale of the IoT system increases and the number of sensor nodes in the network becomes large, connecting the sensor nodes to the power lines makes the installation of the system prohibitively expensive if not impossible. It is therefore preferred to power the sensor nodes by batteries. In such battery-powered sensor nodes, low power consumption is an essential requirement considering that the power consumption of the sensor node determines the replacement or recharging frequency of the battery and directly affects the maintenance cost of the IoT system.

Furthermore, to realize the vision of the hyper-connected world filled with trillions of sensor nodes, researchers are working toward the energy-autonomous operation of the wireless sensor nodes, which are powered by the energy harvested from their ambience. In this scenario, the average power consumption of the overall sensor node must be lower than the average rate of energy harvesting. It poses extreme limitations on the power budget of the wireless sensor node, even if the duty-cycled operation scheme is employed to cut down the amount of the power dissipated on average. Since the wireless transceiver is the most power-hungry block in the typical wireless sensor node, reducing the power consumed for wireless communication is critical.

On the other hand, the choice of modulation scheme has a significant impact on the transceiver design in various aspects such as power consumption, complexity, performance, and

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reliability. For short-range low-power communication, the transceivers based on on-off keying (OOK) have been widely implemented. The OOK modulation scheme allows achieving very low power consumption because of the simple circuit architecture used for the transceiver design. For example, the demodulation function of the receiver can be implemented by using an envelope detector without requiring any high-power-consuming circuit components such as oscillators, mixers, and frequency synthesizers [2]–[4]. However, the OOK receiver based on such a simple structure has low sensitivity and high susceptibility to the interferers compared to the receivers employing other modulation schemes such as frequency-shift keying (FSK) and phase-shift keying (PSK). To overcome the limited sensitivity performance, a high-gain amplifier and an expensive external filter are required to precede the envelope detector [2]. The FSK modulation with a constant envelope, on the other hand, enables the use of an energy-efficient nonlinear power amplifier in the transmitter. However, the receiver requires the precise local oscillator and quadrature signal paths, which results in a complex receiver structure consuming relatively high power.

Recently, to overcome the limitations of the conventional receivers, a variety of new receiver structures for ultra-low-power (ULP) consumption have been introduced (Fig. 1). Fig. 1(a) shows the structure of the uncertain-IF receivers [5]. In this structure, a low-power free-running ring oscillator is used to generate the local oscillator (LO) signal for down-conversion. Due to the inherent uncertainty of the LO signal frequency, the IF frequency is not clearly determined, and the selectivity performance of the receiver is therefore low. Fig. 1(b) shows the low-IF receiver structure, where the receive path itself operates as a part of the frequency-locked loop (FLL) for LO generation [6]. Since the mixers in the receive path perform frequency down-conversion for not only receiver function but also FLL operation, the high-precision LO signal can be generated without using a power-hungry frequency divider. However, the structural complexity is high due to the FLL and quadrature demodulation circuits. Fig. 1(c) shows the receiver structure based on the injection-locked oscillator (ILO) [7], [8]. The ILO plays an essential role of converting the frequency-modulated signal to the amplitude-modulated signal, which enables the energy-efficient implementation of the FSK receiver. The amplitude-modulated signal generated by the ILO is down-converted by the envelope detector as in the conventional low-power OOK receiver. This structure, however, faces significant challenges in that the amplitude of the signal injected to the ILO should be sufficiently large for guaranteeing proper injection-locking operation and kept relatively constant for maintaining consistent frequency-to-amplitude conversion ratio.

In this paper, we propose a low-power receiver design based on ILO, which can support multiple modulation schemes: OOK, binary FSK (BFSK), and differential binary PSK (DBPSK). The proposed receiver enables more robust communication based on FSK and PSK modulation schemes than the simple OOK receiver when necessary, without

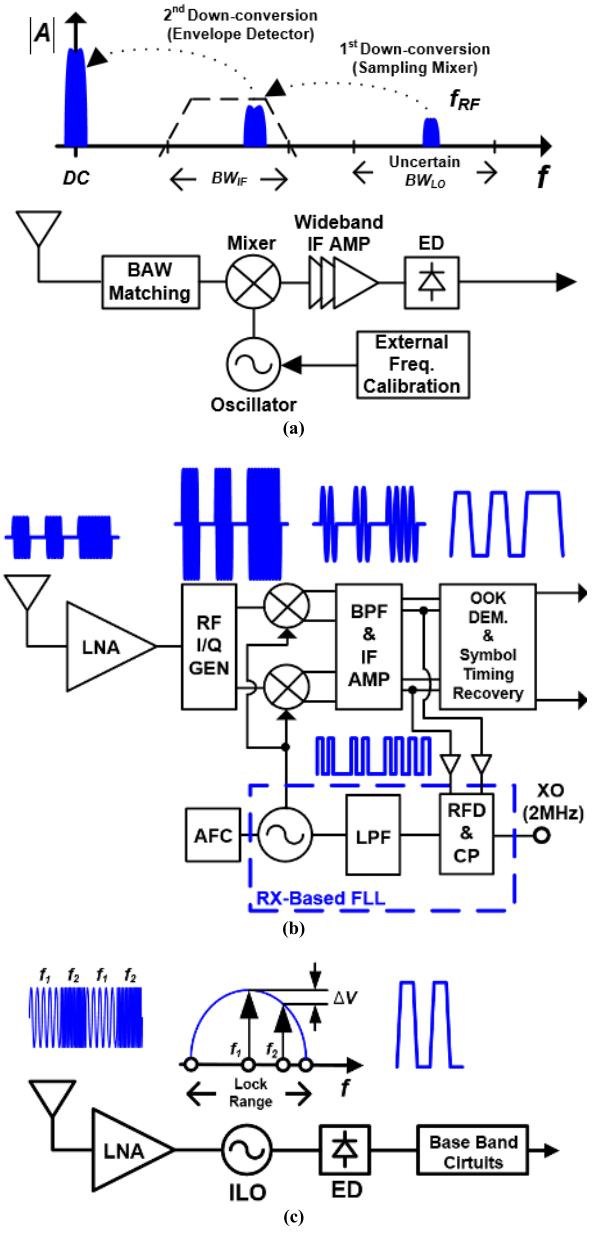


FIGURE 1. ULP receiver architectures: (a) uncertain-IF, (b) low-IF, and (c) injection-locking receivers.

causing any power penalty. Also, in the case where the power reduction of the transmitter is critical, the FSK modulation with a constant envelope can be utilized to allow the use of an energy-efficient nonlinear power amplifier. A Q-enhanced single-ended-to-differential amplifier (SDA) is employed to provide high gain and generate the injection signal with sufficient strength. Moreover, the consistency of the receiver performance is greatly improved by controlling the amplitude of the injection signal in a closed-loop manner. The rest of this paper is organized as follows. Section II describes the overall receiver architecture, and Section III explains the principles of the ILO-based receiver operation performing the frequency-to-amplitude,

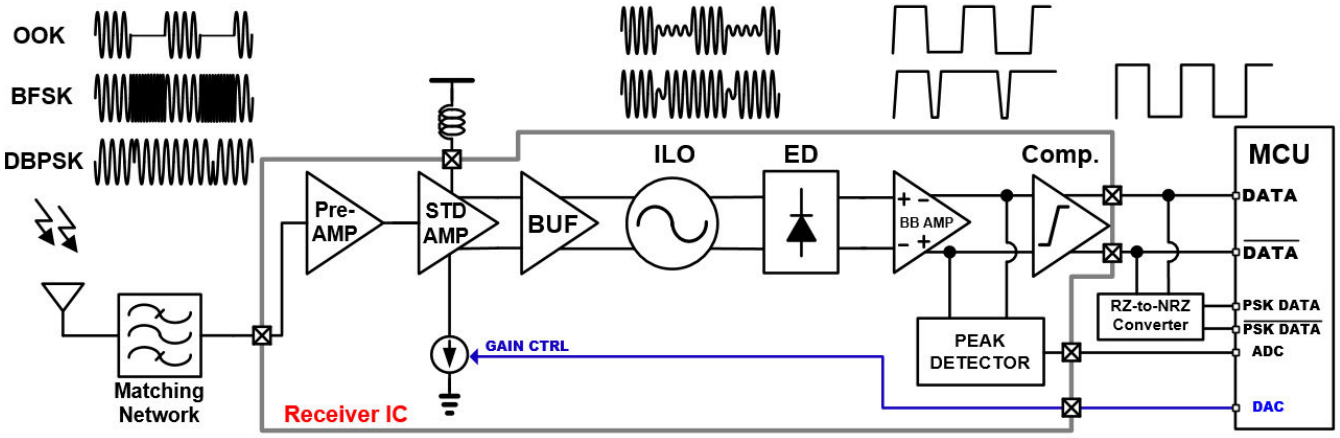


FIGURE 2. Overall architecture of the proposed wireless receiver system.

phase-to-amplitude, and amplitude-to-amplitude conversions. Then, the circuit implementation details of the proposed RF receiver are described in Section IV, and the measurement results of the implemented receiver are presented in Section V. Finally, Section VI draws the conclusion.

II. OVERALL RECEIVER ARCHITECTURE

Fig. 2 is the block diagram showing the overall architecture of the proposed wireless receiver system, consisting of the front-end matching network, RF receiver IC, and microcontroller unit (MCU). In the RF receiver IC, the ILO converts the received OOK/BFSK/DBPSK signal to the amplitude-modulated signal. Based on such ILO operation, an energy-efficient wireless receiver can be realized by employing an envelope detector (ED) for RF-to-baseband frequency down-conversion and demodulation. The external MCU generates a gain control signal for the SDA based on the output amplitude of the baseband amplifier (BB AMP), which is measured by the peak detector. Through this closed-loop control, the magnitude of the RF signal injected to the ILO can be kept fairly constant, and hence a significant change in the frequency-to-amplitude conversion ratio of the ILO can be prohibited when the BFSK signal is received.

The RF signal received by the antenna is fed to the preamplifier (Pre-AMP) through the matching network. The Pre-AMP amplifies the RF signal with moderate gain and provides isolation between the matching network and the SDA input to relieve the requirement of input-impedance matching for the SDA.

The SDA converts the single-ended input signal into an amplified differential signal driving the ILO. The Q-enhancement technique is applied to the SDA so that high gain can be achieved over a narrow frequency band. The high gain property allows obtaining the injection signal with an amplitude larger than the minimum required for locking the ILO even when the received RF signal is very weak, thereby enhancing the sensitivity of the receiver. Since the Q-enhanced SDA acts as a band-pass filter having a narrow passband, the selectivity of the receiver is also improved.

The differential output of the SDA is injected to the ILO, where the OOK/BFSK/DBPSK signal is converted into the amplitude-modulated signal. For the OOK signal, the ILO simply adds the constant amount of signal amplitude as explained in Section III, and thus the amplitude variations of the input signal are preserved at the ILO output. In the case of the BFSK signal, the ILO output has a large amplitude when the frequency of the injection signal (ω_{inj}) is close to the free-running frequency of the ILO (ω_0), while the output amplitude becomes small when ω_{inj} is far from ω_0. For the DBPSK signal, the output amplitude of ILO fluctuates when the phase of the injection signal changes abruptly. The ILO not only translates the OOK/BFSK/DBPSK signal to the amplitude-modulated signal but also improves the receiver sensitivity because the weak RF signal injected to the ILO generates the oscillator output signal having a relatively large swing.

The ILO output at RF is then converted down to the baseband by the ED. The baseband signal is further amplified by the BB AMP, and the BB AMP output is processed by the comparator to produce the final output data. Note that the output data for the DBPSK signal exhibits a return-to-zero (RZ) signal characteristic, as explained in Section III-C, from which the input data can be recovered by converting the RZ data to the non-return-to-zero (NRZ) data.

For reliable BFSK signal reception and demodulation, the frequency-to-amplitude conversion ratio of the ILO should not vary excessively. However, if the lock range of the ILO changes due to the varying magnitude of the injection signal, the frequency-to-amplitude conversion ratio doesn't stay constant, as explained in Section III. In this work, the strength of the ILO injection signal is regulated in a closed-loop manner, so that the ILO can provide a consistent frequency-to-amplitude conversion ratio. The peak detector in the receiver IC measures the amplitude of the BB AMP output, and this amplitude information is sent to the external MCU. Then,

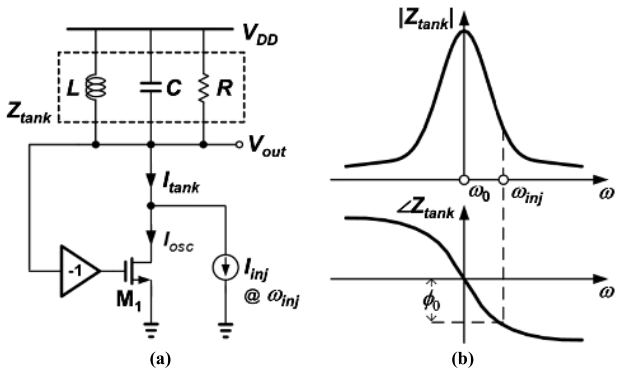


FIGURE 3. (a) Conceptual diagram of ILO, and (b) freuquency response of LC tank.

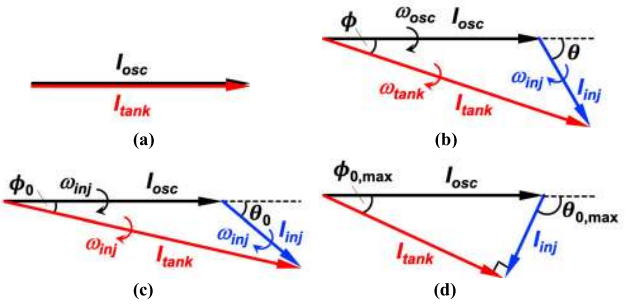


FIGURE 4. Phasor diagrams of ILO currents when the ILO (a) runs freely, (b) experiences locking transition, (c) is locked, and (d) operates at the edge of its lock range.

the digital-to-analog converter (DAC) embedded in the MCU generates the control signal to adjust the gain of the SDA, thus maintaining the strength of the ILO injection signal relatively constant.

III. OPERATION PRINCIPLES OF ILO-BASED RECEIVER

A. BASIC ILO OPERATION

Fig. 3(a) shows the conceptual diagram of the ILO. When there is no injection signal applied, the oscillator runs freely at ω_0, which is the resonance frequency of the LC tank. At ω_0, the Z_{tank} contributes no phase shift, as illustrated in Fig. 3(b), while the inverting buffer and M_1 create a total phase shift of 360°. In the free-running condition, the magnitude and phase of I_{tank} are the same as those of I_{osc}, as shown in Fig. 4(a).

Now assume that the injection current I_{inj} having the frequency of ω_{inj} is applied to the ILO. Since the I_{tank} should be the vector sum of I_{osc} and I_{inj}, the relationship among I_{osc}, I_{inj}, and I_{tank} can be described by the phasor diagram as in Fig. 4(b). Before locking, the phasors, I_{osc}, I_{inj}, and I_{tank} rotates clockwise with different angular velocities, ω_{osc}, ω_{inj}, and ω_{tank}, respectively. Hence, the angle θ between I_{osc} and I_{inj}, as well as the angle ϕ between I_{osc} and I_{tank}, varies over time.

After this transition process, if I_{inj} is not too small and ω_{inj} is not too far from ω_0 to achieve injection-locking, the angle between the I_{osc} and I_{tank} becomes ϕ_0, as shown in Fig. 4(c), and this phase difference is compensated by the phase shift of Z_{tank}, as described in Fig. 3(b). It makes the total phase shift around the feedback loop become 360°, and thus the ILO locked to the injection signal. Once injection-locked, the phasors I_{osc}, I_{inj}, and I_{tank} rotate with the same angular velocity of ω_{inj}, keeping ϕ and θ constant at ϕ_0 and θ_0, respectively [9]. From Fig. 4(c), the following relationships can be derived:

$$|I_{tank}| = \sqrt{|I_{osc}|^2 + |I_{inj}|^2 + 2\,|I_{osc}|\,|I_{inj}|\cos\theta_0}, \tag{1}$$

and

$$\begin{aligned}\sin\phi_0 &= \frac{|I_{inj}|}{|I_{tank}|}\sin\theta_0 \\ &= \frac{|I_{inj}|\sin\theta_0}{\sqrt{|I_{osc}|^2 + |I_{inj}|^2 + 2\,|I_{osc}|\,|I_{inj}|\cos\theta_0}}.\end{aligned} \tag{2}$$

As the frequency of injection signal (ω_{inj}) deviates farther from the self-resonance frequency of the ILO (ω_0), the phase shift introduced by Z_{tank} (ϕ_0) grows, as found in Fig. 3(b), and the angle between I_{osc} and I_{tank}, which is depicted in Fig. 4(c), becomes larger. If ω_{inj} keeps departing from ω_0 and finally reaches the edge of the lock range ω_L, ϕ_0 comes to have its maximum possible value $\phi_{0,\max}$ [10]:

$$\sin\phi_{0,\max} = \frac{|I_{inj}|}{|I_{osc}|} \tag{3}$$

when

$$\cos\theta_0 = \cos\theta_{0,\max} = -\frac{|I_{inj}|}{|I_{osc}|}. \tag{4}$$

The phasor diagram under this condition is illustrated in Fig. 4(d), where the I_{inj} and I_{tank} form a 90° angle. From Fig. 4(d), we can also find that

$$\tan\phi_{0,\max} = \frac{|I_{inj}|}{|I_{tank}|} = \frac{|I_{inj}|}{\sqrt{|I_{osc}|^2 - |I_{inj}|^2}}. \tag{5}$$

Since the phase shift, ϕ_0 of Z_{tank} at the frequencies close to ω_0 is described by [10]

$$\tan\phi_0 \approx \frac{2Q}{\omega_0}(\omega_0 - \omega_{inj}), \tag{6}$$

the ω_L can be expressed as

$$\omega_L = |\omega_0 - \omega_{inj}|_{\max} = \frac{\omega_0}{2Q}\cdot\frac{|I_{inj}|}{\sqrt{|I_{osc}|^2 - |I_{inj}|^2}}. \tag{7}$$

Note that ω_L is a function of Q (= quality factor of the LC tank), ω_0, $|I_{osc}|$, and $|I_{inj}|$. Since the values of Q, ω_0, and $|I_{osc}|$ are given by design, these values experience only a little change during operation, which is caused by the variations in the supply voltage and ambient temperature. In contrast, $|I_{inj}|$ can vary significantly and results in large variations of ω_L, as the amplitude of the received input signal changes. The lock range ω_L increases as the injection signal I_{inj} becomes stronger.

Using the operation characteristics of the ILO investigated in this sub-section, an energy-efficient ILO-based receiver

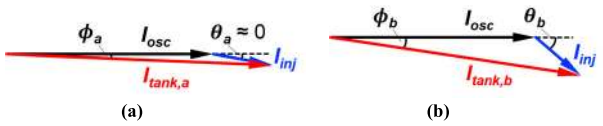


FIGURE 5. Phasor diagrams of ILO currents for the FSK-modulated injection signal when: (a) $\omega_{inj} = \omega_a \approx \omega_0$ and (b) $\omega_{inj} = \omega_b = \omega_a + \Delta\omega$.

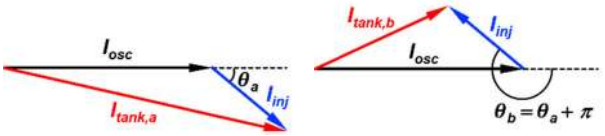


FIGURE 6. Phasor diagrams of ILO currents for the PSK-modulated injection signal when: (a) $\theta_{inj} = \theta_0$ and (b) $\theta_{inj} = \theta_0 + \pi$.

can be implemented, which translates the signal modulated with various modulation schemes such as OOK, BFSK, and DBPSK into a simple amplitude-modulated signal. In the following sub-sections, the principles of such conversions performed by the ILO-based receiver are analyzed and discussed.

B. CONVERSION OF BFSK SIGNAL

Assume that the injection frequency ω_a representing the data bit of '1' is set close to the self-resonance frequency ω_0 and hence $\theta_a \approx 0$ as depicted in Fig. 5(a). Then, from (1), the $|I_{tank,a}|$ can be approximated as

$$\left|I_{tank,a}\right| \approx \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2\,|I_{osc}|\,\left|I_{inj}\right|} = |I_{osc}| + \left|I_{inj}\right|. \tag{8}$$

The output voltage amplitude of the ILO corresponding to '1' ($= |V_{out,a}|$) is produced by the multiplication of $|I_{tank,a}|$ and $|Z_{tank}(\omega_a)|$ ($\approx |Z_{tank}(\omega_0)|$). Since $|I_{tank,a}|$ and $|Z_{tank}(\omega_a)|$ are close to the maximum possible values of $|I_{tank}|$ and $|Z_{tank}|$ respectively, $V_{out,a}$ presents nearly the largest output swing.

On the other hand, if the injection frequency $\omega_b = \omega_a + \Delta\omega$ used to indicate the data bit of '0' is set far from ω_0 but within the lock range, as shown in Fig. 5(b), the $|I_{tank,b}|$ is given by

$$\left|I_{tank,b}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2\,|I_{osc}|\,\left|I_{inj}\right|\cos\theta_b}. \tag{9}$$

The output voltage amplitude of the ILO corresponding to '0' ($= |V_{out,b}|$) is derived by multiplying $|I_{tank,b}|$ with $|Z_{tank}(\omega_b)|$ ($< |Z_{tank}(\omega_0)|$). Since $|I_{tank,b}|$ and $|Z_{tank}(\omega_b)|$ are smaller than $|I_{tank,a}|$ and $|Z_{tank}(\omega_a)|$ respectively, $|V_{out,b}|$ is also smaller than $|V_{out,a}|$. How large amplitude difference between $V_{out,a}$ and $V_{out,b}$ is obtained for the frequency deviation of $\Delta\omega = |\omega_b - \omega_a|$ determines the frequency-to-amplitude conversion ratio.

Note that once the injection frequency ω_b for the data bit of '0' is determined, the corresponding phase shift ϕ_b is fixed as described in Fig. 3(b). It can be found in Fig. 5(b) that, for the same ϕ_b, if $|I_{inj}|$ increases, θ_b decreases, and hence $\cos\theta_b$ approaches 1. In other words, the difference between $|I_{tank,a}|$ and $|I_{tank,b}|$ becomes smaller, and thus the frequency-to-amplitude conversion ratio decreases as $|I_{inj}|$ increases. It demonstrates the need for prohibiting any significant variations in the magnitude of I_{inj} to obtain a consistent demodulation performance over a wide range of received RF signal strength.

To achieve a good sensitivity, the receiver should be designed to operate even with a very weak RF input signal, which leads to a very small amplitude of I_{inj}. Since ω_L is narrow for small $|I_{inj}|$ as predicted by (7), the ω_a and ω_b cannot be separated too far from each other. The ILO-based receiver is therefore designed to generate a distinguishable amplitude change for such a small frequency difference when $|I_{inj}|$ is small. However, if a strong RF signal is received and hence the amplitude of I_{inj} increases, the ω_L becomes wide, and the frequency-to-amplitude conversion ratio reduces significantly, resulting in too small amplitude change at the ILO output to be discriminated properly. To avoid this problem, it is important to control the magnitude of I_{inj} to stay relatively constant.

C. CONVERSION OF DBPSK SIGNAL

The conversion process from the DBPSK-modulated signal to the amplitude-modulated signal by the ILO is depicted in Fig. 6. Since I_{tank} is the vector sum of I_{osc} and I_{inj}, and V_{out} is the multiplication of I_{tank} and Z_{tank}, when there is a phase change of π in I_{inj}, the amplitude of V_{out} changes accordingly [11].

When the ILO is in the injection-locked state and I_{inj} forms the angle of θ_a with respect to the I_{osc} to represent the data bit of '1', $|I_{tank,a}|$ is given by

$$\left|I_{tank,a}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2\,|I_{osc}|\,\left|I_{inj}\right|\cos\theta_a}, \tag{10}$$

as described in Fig. 6(a).

If the angle between I_{inj} and I_{osc} changes to $\theta_b = \theta_a + \pi$ which corresponds to the data bit of '0', the ILO is perturbed from its injection-locked state and the magnitude of I_{tank} experiences an instantaneous change to $|I_{tank,b}|$, which is expressed as

$$\begin{aligned}\left|I_{tank,b}\right| &= \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2\,|I_{osc}|\,\left|I_{inj}\right|\cos(\theta_a + \pi)} \\ &= \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 - 2\,|I_{osc}|\,\left|I_{inj}\right|\cos\theta_a},\end{aligned} \tag{11}$$

as depicted in Fig. 6(b). After this transient change, as the frequency of the injection signal does not change, the ILO returns to the injection-locked state, as shown in Fig. 6(a) and the magnitude of I_{tank} settles back to $|I_{tank,a}|$. In other words, the output amplitude of ILO fluctuates when the phase of the injection signal changes abruptly.

As a result, the phase change in the injection signal is translated to the transient variation of the output amplitude, and this amplitude variation can be captured by the following ED circuit, obviating the need for power-hungry circuit blocks such as the frequency synthesizer and mixer. Note that the output of the ED behaves like an RZ signal, which requires a conversion to the NRZ signal for input data recovery [11].

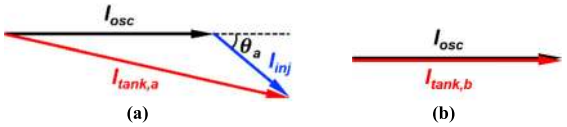


FIGURE 7. Phasor diagrams of ILO currents for the OOK-modulated injection signal when: (a) I_{inj} is on and (b) I_{inj} is off.

D. CONVERSION OF OOK SIGNAL

Fig. 7 shows how the amplitude variations of the OOK-modulated input signal are preserved at the ILO output. When I_{inj} is on to present the data bit of '1', the I_{inj} is added to the I_{osc} to produce I_{tank}, and hence the amplitude of I_{tank} ($= |I_{tank,a}|$) becomes larger than that of I_{osc}:

$$\left|I_{tank,a}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2\,|I_{osc}|\,\left|I_{inj}\right|\cos\theta_a}. \quad (12)$$

On the other hand, if I_{inj} is off to present the data bit of '0', the amplitude of I_{tank} ($= |I_{tank,b}|$) becomes the same as that of I_{osc}:

$$\left|I_{tank,b}\right| = |I_{osc}|\,. \quad (13)$$

Multiplied by Z_{tank}, the I_{tank} generates the amplitude-modulated V_{out} signal.

In conclusion, the OOK input signal is also processed by the ILO to generate the amplitude-modulated signal at the output, as in the cases of BFSK and DBPSK input signal. Based on this conversion process of the ILO, an energy-efficient receiver IC can be constructed. The implementation details of the receiver circuits are described in the next section.

IV. CIRCUIT IMPLEMENTATION

A. RF FRONT-END

The Pre-AMP and SDA amplify the received RF signal to obtain the signal with an amplitude larger than the minimum required to lock the following ILO. The Pre-AMP is based on the conventional cascode common-source structure with inductive degeneration and tuned load circuit [12]. Off-chip inductors and capacitors are used to construct the input matching network. Due to the good isolation characteristic of the cascode structure, a stable input matching performance is obtained without being affected by variations of the impedance at the output. The voltage gain of the Pre-AMP is given by

$$G_{Pre-AMP} = \frac{R_L}{2L_S\omega_0}, \quad (14)$$

where L_S is the degeneration inductance, and ω_0 and R_L are the resonance frequency and parallel equivalent resistance of the load tank circuit, respectively.

The second amplifier stage following the Pre-AMP is designed to not only provide a high voltage gain but also convert the single-ended input signal to the differential output signal, which leads to the Q-enhanced SDA structure. It is well known that the differential signaling has an inherent immunity against the common-mode noise and disturbances,

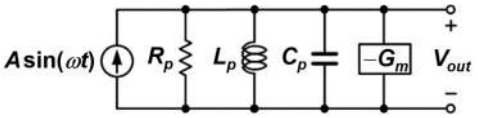


FIGURE 8. Schematic diagram of the parallel resonant circuit with a negative conductance element.

and the differential injection significantly reduces the minimum amplitude needed for the injection-locking of the LC oscillator compared to the single-ended injection. The SDA design employs a Q-enhancement technique and a parallel resonant circuit structure.

The operation principle of the Q-enhanced amplification can be explained by using the equivalent circuit model shown in Fig. 8. This circuit operates in two different modes [13]. When $|-G_m| < 1/R_p$, the amount of energy put into the circuit by active devices is not enough to overcome the tank loss and build up the oscillation. The circuit, therefore, operates as a Q-enhanced amplifier. Conversely, if $|-G_m| > 1/R_p$, the circuit operates in the oscillation mode.

The quality factor Q of the parallel resonant circuit in Fig. 8 is given by [14]

$$Q = \omega_0 \frac{\text{energy stored}}{\text{average power dissipated}} = \frac{\omega_0}{BW} = \frac{R_{p,eff}}{\sqrt{L_p/C_p}}, \quad (15)$$

where BW is the 3-dB bandwidth of the parallel resonant circuit and $R_{p,eff}$ is calculated as

$$R_{p,eff} = \frac{1}{1/R_p + (-G_m)}. \quad (16)$$

When the circuit in Fig. 8 operates in the amplifier mode, a high Q leads to a high voltage gain and a narrow amplification bandwidth, which improves the selectivity of the receiver.

From (15) and (16), it is found that the Q varies as the value of $|-G_m|$ changes. When the $|-G_m|$ is much smaller than $1/R_p$, the circuit operates in the amplification mode, and the Q of the circuit is low. As the $|-G_m|$ increases, the Q increases, approaching infinity when $|-G_m|$ reaches the value of $1/R_p$. If the $|-G_m|$ continues to increase beyond $1/R_p$, the circuit enters the oscillation mode. Based on this characteristic, it is possible to implement a Q-enhanced amplifier with high gain and narrow bandwidth by operating the parallel resonant circuit as an amplifier and setting its $|-G_m|$ value close to $1/R_p$ [15], [16].

The core circuit of the proposed Q-enhanced SDA is based on the aforementioned parallel resonant circuit structure and its simplified schematic diagram is shown in Fig. 9(a). This circuit oscillates when the voltage at the drain node is 180° out of phase with respect to the voltage at the gate node, and the negative conductance generated by the MOS transistor is larger than $1/R_1$. If we set the negative conductance value to be slightly smaller than $1/R_1$ and take the differential outputs from the gate and drain nodes, this circuit operates as a Q-enhanced SDA. The input signal is applied to the drain node in the form of current.

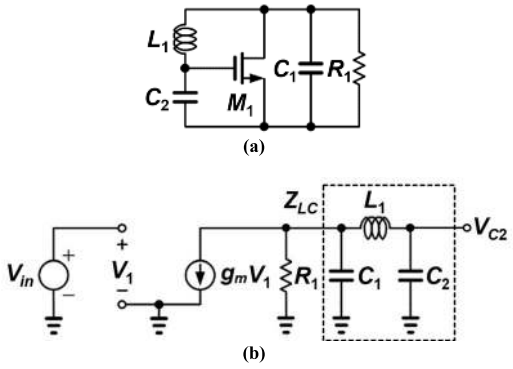


FIGURE 9. (a) Simplified schematic diagram of the Q-enhanced SDA core circuit, and (b) its small-signal equivalent circuit for loop gain analysis.

To investigate the operation of the circuit shown in Fig. 9(a), the feedback loop of this circuit can be cut at the gate node of the MOS transistor to analyze the loop gain characteristic. By using the small-signal equivalent circuit given in Fig. 9(b), the loop gain can be calculated as

$$T(\omega) = \frac{V_{C2}}{V_{in}} = -g_m \times \frac{R_1 \cdot Z_{LC}}{R_1 + Z_{LC}} \times F_v, \tag{17}$$

where Z_{LC} is the total equivalent impedance of the circuit network composed of L_1, C_1, and C_2, and F_v is the voltage division factor caused by the series-connected L_1 and C_2.

The Z_{LC} is given by

$$Z_{LC} = \frac{\frac{1}{j\omega C_1}\left(j\omega L_1 + \frac{1}{j\omega C_2}\right)}{j\omega L_1 + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}}, \tag{18}$$

and F_v is expressed as

$$F_v = \frac{\frac{1}{j\omega C_2}}{j\omega L_1 + \frac{1}{j\omega C_2}} = \frac{1}{1 - \frac{\omega^2}{\omega_{inv}^2}}, \tag{19}$$

where

$$\omega_{inv} = \frac{1}{\sqrt{L_1 C_2}}. \tag{20}$$

Note that F_v introduces a phase inversion at the frequencies higher than ω_{inv}, as depicted in Fig. 10(a). Substituting (18) and (19) into (17), the loop gain is derived as

$$T(\omega) = \frac{-g_m}{j\omega(C_1+C_2)\{1-\omega^2 L_1(C_1||C_2)\} + (1-\omega^2 L_1 C_2)/R_1}. \tag{21}$$

If this circuit oscillates, the oscillation frequency is given by

$$\omega_0 = \frac{1}{\sqrt{L_1(C_1||C_2)}}. \tag{22}$$

At this oscillation frequency, the magnitude of the loop gain is calculated as

$$|T(\omega_0)| = g_m R_1 \frac{C_1}{C_2}, \tag{23}$$

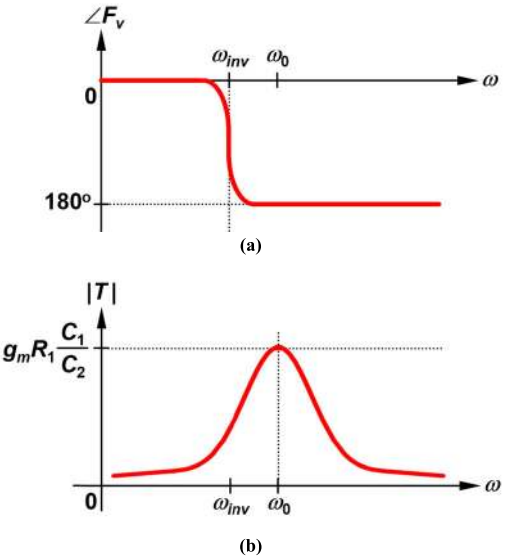
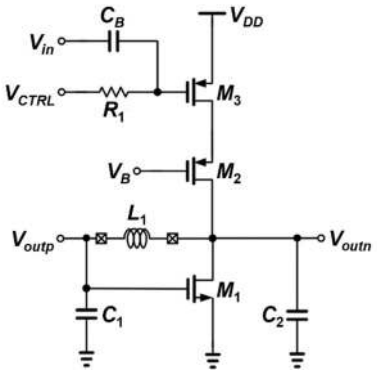


FIGURE 10. (a) Phase vs. frequency characteristic of the voltage division factor F_V, and (b) magnitude vs. frequency characteristic of the loop gain T.



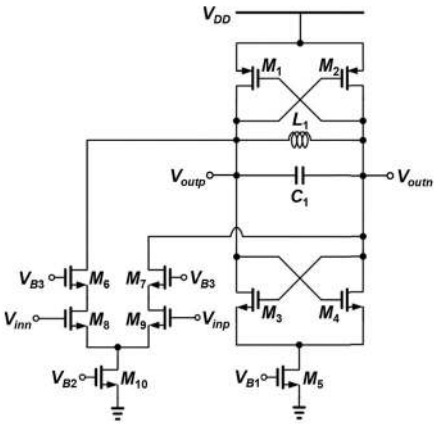
M_1	6 μm / 0.18 μm
M_2	4.5 μm / 0.18 μm
M_3	15 μm / 0.18 μm
L_1	6 nH
C_1, C_2	351 fF
R_1	320 kΩ
C_B	1.79 pF

FIGURE 11. Schematic diagram of the proposed Q-enhanced SDA.

which needs to be greater than 1 for the oscillation to occur. The magnitude of the loop gain shows the frequency characteristic, as presented in Fig. 10(b).

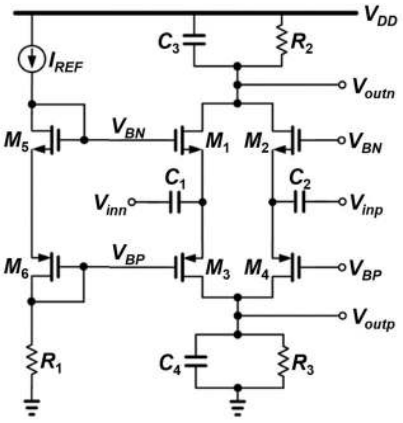
From (20) and (22), we can find that ω_0 is higher than ω_{inv}. Therefore, the feedback network causes a phase shift of 180° at ω_0, which is added to the phase inversion generated by the MOS transistor, leading to a total phase shift of 360° along the loop. If the transconductance value is controlled in such a way that the magnitude of the loop gain stays slightly lower than 1, the circuit can be operated as a Q-enhanced amplifier. Moreover, if the output voltages are taken from the gate and drain nodes of the MOS transistor while the input current is applied to the drain terminal, the circuit can also be used to convert the single-ended input to the differential output.

The complete circuit diagram of the proposed Q-enhanced SDA is shown in Fig. 11. M_3 converts the input voltage V_{in} to the corresponding input current, which is fed to the drain node of M_1 through M_2. M_2 is used as a cascode element to provide isolation between the input and output terminals. The voltage gain of this Q-enhanced SDA can be controlled



M_1, M_2	70 µm / 0.18 µm
M_3, M_4	50 µm / 0.18 µm
M_5	0.5 µm / 1 µm
M_6, M_7	1.5 µm / 0.18 µm
M_8, M_9	5 µm / 0.18 µm
M_{10}	2 µm / 1 µm
L_1	8.24 nH
C_1	40 fF

FIGURE 12. Schematic diagram of the ILO.



M_1, M_2	10 µm / 0.18 µm
M_3, M_4	20 µm / 0.18 µm
M_5	10 µm / 0.18 µm
M_6	20 µm / 0.18 µm
C_1, C_2	1.79 pF
C_3, C_4	100 fF
R_1	120 kΩ
R_2, R_3	120 kΩ

FIGURE 13. Schematic diagram of the fully differential ED.

by adjusting the gate bias voltage V_{CTRL} of M_3. The V_{CTRL} determines the bias current flowing through M_1 and hence its transconductance, which in turn affects the Q–enhancement factor of the parallel resonant circuit formed by M_1, L_1, C_1, and C_2. If the inherent Q of the inductor L_1 is high, a large gain can be obtained with flowing small bias current. In other words, by using a high-Q inductor, the power consumption of the Q-enhance SDA can be reduced. In this work, an off-chip inductor component having a high Q is used.

The center frequency and amplification gain of the SDA need to be tuned to accommodate the manufacturing process tolerances. We employ a tuning method similar to the one used in [15]. For frequency tuning, the V_{CTRL} is initially controlled to flow large enough bias current to oscillate the circuit. In the oscillation mode, the center frequency is tuned to the target value by controlling the capacitor banks C_1 and C_2. Once the frequency tuning is completed, the V_{CTRL} is adjusted again to enter the amplification mode and tune the amplification gain to the wanted value.

Fig. 12 presents the schematic diagram of the ILO used in our design. The ILO consists of a current injection circuit (M_{6-10}) and an oscillator core circuit (M_{1-5}, L_1, and C_1). In this topology, the complementary cross-connected MOS transistor pairs ($M_{1,2}$ for the PMOS pair and $M_{3,4}$ for the NMOS pair) provide negative resistance. The current injection circuit plays a role of converting the differential injection voltage to the differential injection current that is fed to the oscillator core circuit. In the oscillator core, a capacitor bank is employed so that the free-running frequency of the ILO can be tuned to the desired value.

The schematic diagram of the fully differential ED is shown in Fig. 13 [17]. The nonlinear I-V characteristics of the NMOS transistor $M_{3,4}$ and the PMOS transistors $M_{1,2}$ are used to down-convert the RF signal at the input to the baseband signal at the output. The common-gate topology is used, i.e., the input is applied to the source nodes of the transistors, and the output is taken from the drain nodes of the transistors. The low-pass filters, formed by $C_{3,4}$ and $R_{2,3}$ are placed to filter out high-frequency components produced by the nonlinear transfer function of the transistors. At the input nodes, the AC-coupling capacitors $C_{1,2}$ are employed to construct the high-pass filters when combined with the input resistances of the NMOS and PMOS transistors $M_{1,3}$ and $M_{2,4}$, respectively. The biasing circuit consists of stacked transistors $M_{5,6}$, I_{REF}, and R_1, where M_5 comprises the current mirrors with $M_{1,2}$ and M_6 constitutes the current mirrors with $M_{3,4}$. The core transistors M_{1-4} are biased in the weak-inversion region. The amplitude of the differential output voltage is given by

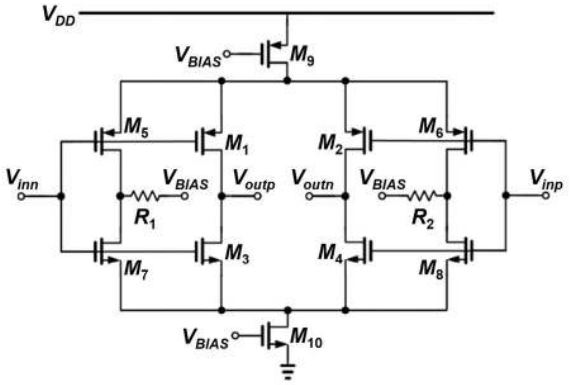
$$|V_{out}| = |V_{outp} - V_{outn}| = \frac{|I_Q| \times R_{2,3} \times |V_{in}|^2}{4V_T^2} \quad (24)$$

where V_T is the thermal voltage and $|V_{in}|$ is the amplitude of the differential input voltage, $|V_{inp} - V_{inn}|$. The I_Q is the quiescent current of the core transistors operating in weak inversion.

B. ANALOG BASEBAND

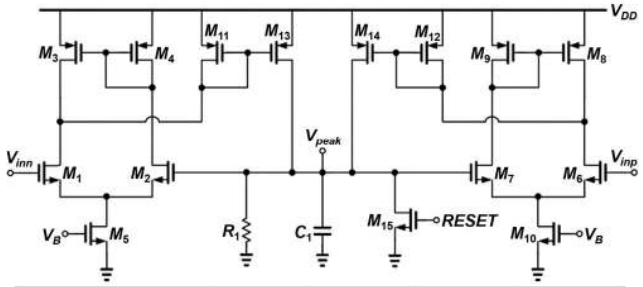
After the down-conversion by the fully differential ED, the signal resides in the baseband, which is processed by the analog baseband circuits consisting of a BB AMP, a comparator, and a peak detector. For baseband amplification, the conventional 2-stage fully differential operational amplifier is used. Compared to its single-ended counterpart, this balanced operational amplifier provides a larger effective output voltage swing and is less susceptible to common-mode noise and disturbances. Also, the even-order nonlinearities are canceled to the first order at its differential output. The voltage gain of the implemented BB AMP is 25 dB, and its operation bandwidth is from 300 Hz to 1 MHz.

The schematic diagram of the fully differential comparator is shown in Fig. 14, which employs the self-biasing structure [18]. The resistors $R_{1,2}$ are used to extract the common-mode output voltage from the replica-biasing circuit composed of M_{5-8}, which is fed to the gate terminals of $M_{9,10}$ to control the bias current of the overall comparator circuit. This self-biasing scheme creates a negative feedback loop that stabilizes the operating point of the circuit. Note



M_1, M_2, M_5, M_6	4 μm / 1 μm	M_3, M_4, M_7, M_8	2 μm / 1 μm	M_9	20 μm / 1 μm
M_{10}	5 μm / 1 μm	R_1, R_2	Pseudo - resistor	-	-

FIGURE 14. Schematic diagram of the fully differential comparator.



M_1, M_2, M_6, M_7	10 μm / 1 μm	M_3, M_4, M_8, M_9	6 μm / 5 μm	M_{11}, M_{12}, M_{13}, M_{14}	6 μm / 5 μm
M_5, M_{10}	4 μm / 8 μm	R_1	500 kΩ	C_1	1.79 pF

FIGURE 15. Schematic diagram of the positive peak detector.

that the $M_{9,10}$ operate in the linear region, and therefore the output swing of the comparator can be close to the difference between the two supply rails. Thanks to the fully differential structure of the compactor, the explicit reference voltage for comparison doesn't need to be generated.

As shown in Fig. 15, a positive peak detector is implemented using differential amplifiers (M_{1-10}), current mirrors (M_{11-14}), and a low-pass filtering load (R_1, C_1, and M_{15}). If the V_{in} is larger than V_{peak}, the excess current flows through $M_{11,12}$ and is copied to $M_{13,14}$, charging the C_1, which holds the peak value. The R_1 provides a small amount of discharging current, and the M_{15} is used for resetting C_1. The droop rate of the peak detector can be controlled by adjusting the values of C_1 and R_1.

V. MEASUREMENT RESULTS

The proposed ILO-based OOK/BFSK/DBPSK receiver has been fabricated with 0.18-μm CMOS process technology, and the chip micrograph is shown in Fig. 16. The total chip area, including the bonding pads, is 1.7 mm × 1.9 mm. The receiver is implemented using three inductors. Two of them are the on-chip inductors used for the Pre-AMP and ILO, and

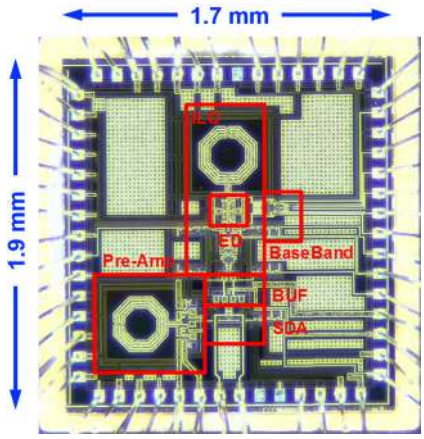


FIGURE 16. Chip micrograph of the fabricated receiver IC.

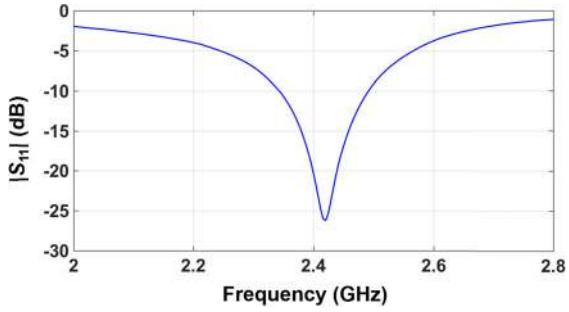


FIGURE 17. Impedance matching characterisitc of the recever.

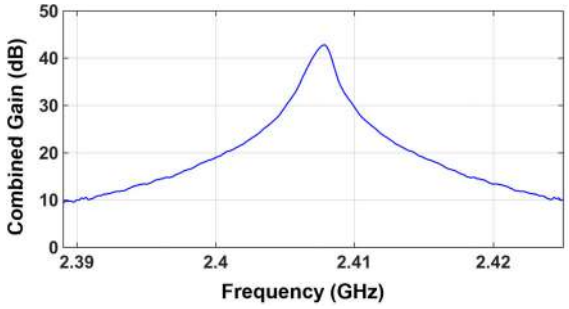


FIGURE 18. Combined gain of the Pre-AMP and Q-enhanced SDA.

the other is the off-chip inductor with high Q used for the SDA.

The input impedance matching characteristic of the receiver is shown in Fig. 17, while the combined gain of the Pre-AMP and SDA is plotted in Fig. 18 as a function of frequency. The magnitude of S_{11} is lower than –10 dB over the frequency range from 2.36 GHz to 2.49 GHz, which covers the ISM band. The Pre-AMP and Q-enhanced SDA provides a high voltage gain up to 43 dB with narrow bandwidth, which improves the sensitivity as well as the selectivity of the proposed receiver.

Fig. 19 shows the measured output waveforms of the ILO generated for the RF input signals with different modulation schemes. The baseband data of the input signal with a data rate of 50 kb/s is shown in Fig. 19(a). Based on this baseband data, –90-dBm RF input signals are gener-

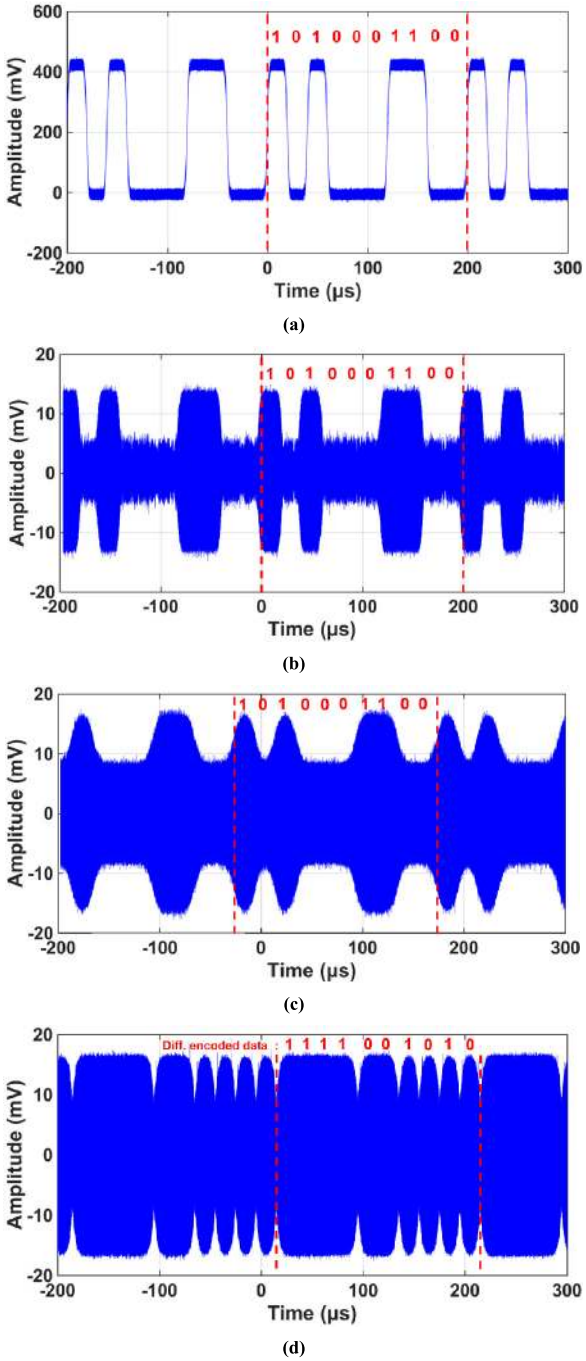


FIGURE 19. (a) Baseband data of the receiver input and the corresponding ILO output waveforms for the receiver input modulated by (b) OOK, (c) BFSK, and (d) DBPSK schemes.

ated with OOK, BFSK, and DBPSK modulation schemes. Fig. 19(b) presents the output waveform of the ILO when the OOK-modulated input signal is applied to the receiver. As explained in Section III-D, the amplitude variations of the OOK-modulated input signal are preserved at the ILO output, and thus the amplitude of the ILO output signal varies according to the input baseband data. Fig. 19(c) shows the output waveform of the ILO when the receiver input is the BFSK signal modulated between 2.404 GHz and 2.406 GHz

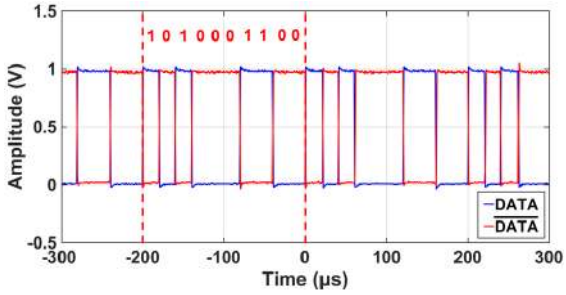


FIGURE 20. Demodulated output data of the receiver.

with the frequency deviation of 2 MHz. The frequency-to-amplitude conversion characteristic of the ILO generates the variations in the amplitude of the ILO output signal corresponding to the input baseband data. The ILO output waveform for the DBPSK-modulated input signal is shown in Fig. 19(d). When the phase of the input signal changes, the ILO is perturbed from its injection-locked state, resulting in the instantaneous change of the ILO output amplitude. After the transient amplitude fluctuation, the ILO turns back to the injection-locked state, and its original output amplitude is recovered. It is found that the ILO output waveform presents an RZ signal characteristic as explained in Section III-C, and therefore the input baseband data can be recovered by converting the RZ signal to the NRZ data. From the results shown in Fig. 19, it is verified that the OOK/BFSK/DBPSK-modulated input signal can be converted to the amplitude-modulated output signal by the ILO operation, which enables the energy-efficient ED-based receiver structure.

As illustrated in Fig. 2, the ILO output is fed to the ED to generate the baseband signal capturing the variations in the amplitude envelope of the ILO output, and the ED output is amplified by the BB AMP. The amplified baseband signal is processed by the comparator to produce the output bit stream. Note that the output of the ED is AC-coupled to the input of the BB AMP. When the receiver input signal is OOK- or BFSK-modulated, the comparator output can directly be used as the demodulated output data. In the case of the DBPSK-modulated input signal, the comparator output needs to go through the conversion process from the RZ data to the NRZ data to produce the demodulated output. Fig. 20 presents the demodulated output of the receiver, which is consistent with the input baseband data shown in Fig. 19(a). This result verifies that the proposed receiver can process the modulated RF input signal properly to generate the correct and accurate output data.

When the RF input signal is BFSK-modulated, as shown in Fig. 2 and discussed in Section III-B, the peak detector is used to regulate the strength of the ILO injection signal so that the frequency-to-amplitude conversion performance of the ILO can be maintained reliably. The peak detector provides the amplitude information of the baseband signal to the MCU through the analog-to-digital converter (ADC) interface of the MCU, and the MCU generates an appropriate DC voltage (V_{CTRL} in Fig. 11) through its DAC output to control the SDA

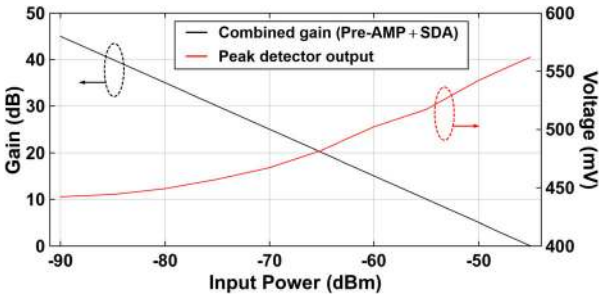


FIGURE 21. SDA gain control characteristic as a function of the receiver input power.

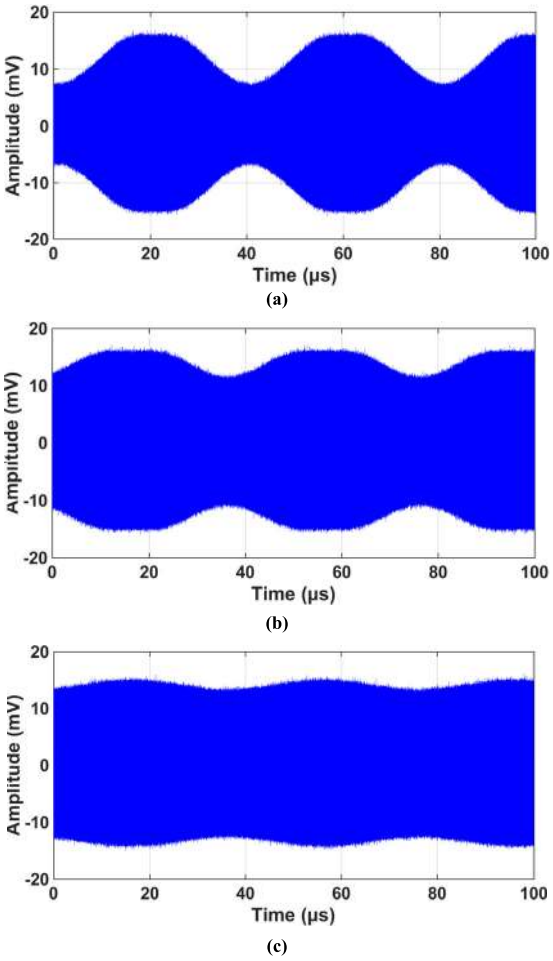


FIGURE 22. ILO output waveforms measured for the BFSK-modulated receiver input signal with different power levels: (a) –70 dBm, (b) –66 dBm, and (c) –64 dBm, when the SDA gain control loop is disabled.

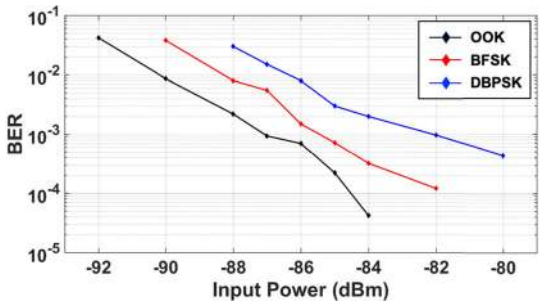


FIGURE 23. BER performance of the proposed receiver measured with the data rate of 50 kb/s as a function of the input power.

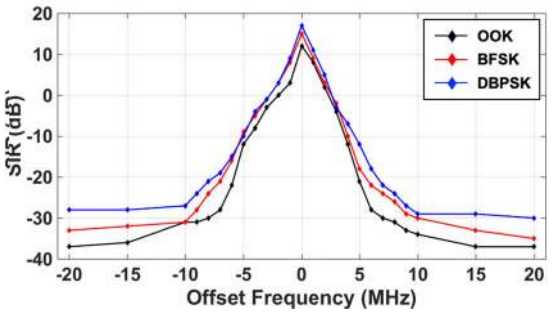


FIGURE 24. SIR performance of the proposed receiver measured with the data rate of 50 kb/s and the 6-dB higher input power than the sensitivity limit.

TABLE 1. Power breakdown of the receiver.

Pre-Amplifier	75 μA
SDA	33 μA
Buffer	80 μA
ILO	130 μA
ED	2 μA
BB AMP	2 μA
Comparator	1 μA
Peak Detector	1 μA
Total Power	324 μW

gain, forming the closed regulation loop. In the proposed receiver, the amplitude of the ILO injection signal is kept constant at –45 dBm to obtain the lock range of about 2 MHz consistently, leading to an optimal frequency-to-amplitude conversion ratio. As shown in Fig. 21, when the receiver input power changes from –90 dBm to –45 dBm, the peak detector generates the corresponding output voltage varying from 440 mV to 560 mV, and this information is processed by the external MCU to control the SDA gain from 45 dB to 0 dB. As a result, the ILO injection strength is regulated to –45 dBm for the wide range of the receiver input power.

Fig. 22 shows the ILO output waveform for different levels of the receiver input power when the closed-loop SDA gain control function is disabled, and the combined gain of the Pre-AMP and SDA is fixed at 25 dB. As shown in Fig. 22(a), if the RF input signal is FSK-modulated with the frequency deviation of 2 MHz and its power level is –70 dBm, the ILO output exhibits a sufficiently large amplitude variation of 8 mV. However, as the power of the input signal increases, the frequency-to-amplitude conversion ratio degrades greatly, as shown in Fig. 22(b) and (c). This result demonstrates the importance of regulating the power of the ILO injection signal through the closed-loop gain control.

TABLE 2. Performance summary and comparison with previous works.

	ISSCC '08 [5]	ISSCC '15 [6]	SOVC '14 [15]	JSSC '11 [8]	SOVC '17 [19]		JSSC '18 [20]	This work
Technology (nm)	90	65	130	180	65		40	180
Supply Voltage (V)	0.5	0.6	0.7	0.7	0.6		0.65	1
Architecture	Uncertain IF	Low IF	Envelope Detection	Injection Locking	Sliding IF		Super Regeneration	Injection Locking
Frequency (MHz)	2000	2400	915	920	2400		900	2400
Modulation	OOK	OOK	BFSK	BFSK	BFSK		OOK	OOK/BFSK/ DBPSK
Data Rate (kb/s)	100	1000	500	5000	25	50	1000	50
Sensitivity (dBm)	-72	-83	-90	-73	-102	-101	-86	-87
Power consumption (μW)	52	227	500	420	466		320	324

Fig. 23 plots the bit-error-rate (BER) test results performed at the data rate of 50 kb/s with varying the receiver input power. It is found that the proposed receiver achieves the sensitivity of –87, –85, and –82 dBm when the input is modulated with OOK, BFSK, and DBPSK schemes respectively for the data rate of 50 kb/s and BER of 10^{-3}. The signal-to-interference ratio (SIR) performance measured for the interferer near the 2.4-GHz ISM band is presented in Fig. 24. For this SIR measurement, the data rate is set to 50 kb/s, and the input signal power is adjusted to be 6-dB higher than the sensitivity limit of the receiver. The measurement is repeated for different modulation schemes. The SIR measurement result indicates the power level of the interferer that the receiver can withstand. Typically, the ILO-based receiver is vulnerable to the blocker because the ILO can be locked erroneously to the interferer. However, as shown in Fig. 24, the proposed receiver can mitigate this issue significantly by employing the Q-enhanced SDA with the narrow-band amplification characteristic. The measurement results verify that the receiver can distinguish the input signal from the accompanying interferer, exhibiting good selectivity performance.

The power breakdown of the receiver is shown in Table 1. The total power consumption is 324 μW when operated with the supply voltage of 1 V. The most of power is consumed by the Pre-AMP, SDA, buffer, and ILO, while the consumption by the ED, BB AMP, comparator, and peak detector is nearly negligible. Table 2 summarizes the key performances of the proposed receiver and compares them with those of other recent low-power receivers. The receiver presented in this work exhibits competitive performances when compared with other designs. Especially, the proposed receiver can operate with multiple modulation schemes and improves the previous injection-locking-based receiver [8] in that the strength of the injection signal to the ILO is controlled in a closed-loop manner, guaranteeing consistently good performances over a wide range of the receiver input power. Note that the presented receiver IC has been fabricated using a 180-nm technology and operates at 2.4 GHz with 1-V supply voltage, while the other designs in comparison were fabricated in more advanced process technologies except [8], operates at lower frequencies except [6] and [19], and powered by lower supply voltages.

VI. CONCLUSION

An energy-efficient multi-mode receiver that operates in the 2.4-GHz ISM band is presented for use in the wireless sensor node under various IoT application scenarios. The ILO is at the core of the receiver structure, and its inherent injection-locking characteristic is exploited to convert the amplitude, frequency, and phase variations of the OOK, BFSK, and DBPSK input signals respectively to the amplitude fluctuations at the ILO output. After this conversion process, a simple envelope detection follows to extract the amplitude variations of the ILO output envelope as well as to down-convert the signal to the baseband. Consequently, the use of the mixer and the frequency synthesizer can be excluded to minimize the power consumption.

Importantly, the proposed receiver implements the closed-loop control of the ILO injection signal power, unlike the previous ILO-based FSK receiver. The control loop operates by adjusting the Q-enhanced SDA gain according to the baseband signal power monitored by the peak detector. Without this loop, as the receiver input power increases, the ILO lock range becomes wider, and the frequency-to-amplitude conversion performance degrades, leading to the demodulation failure eventually.

In the RF front-end, the Pre-AMP and Q-enhanced SDA are employed to provide a sufficiently large differential injection signal to the ILO even when the RF input power is low, which improves the receiver sensitivity significantly.

In addition, the receiver selectivity is also improved due to the narrow-band amplification characteristic of the Q-enhanced SDA.

When fabricated in 0.18-μm CMOS technology, the proposed receiver achieves the sensitivity of –87, –85, and –82 dBm for the OOK, BFSK, and DBPSK signals respectively at the data rate of 50 kb/s and the BER lower than 0.1% while consuming 324 μW from the 1-V supply.

REFERENCES

[1] A. Burdett, "Ultra-Low-Power wireless systems: Energy-efficient radios for the Internet of Things," *IEEE Solid State Circuits Mag.*, vol. 7, no. 2, pp. 18–28, Jun. 2015.
[2] N. Pletcher, S. Gambini, and J. Rabaey, "A 65 μW, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 539–542.
[3] D. C. Daly and A. P. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, May 2007.
[4] X. Huang, S. Rampu, X. Wang, G. Dolmans, and H. de Groot, "A 2.4 GHz/915 MHz 51μW wake-up receiver with offset and noise suppression," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 222–223.
[5] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 μW wake-up receiver with–72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.
[6] J.-S. Lee, J.-M. Kim, J.-S. Lee, S.-K. Han, and S.-G. Lee, "A 227pJ/b–83dBm 2.4GHz multi-channel OOK receiver adopting receiver-based FLL," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 234–235.
[7] M. Zgaren and M. Sawan, "A low-power Dual-Injection-Locked RF receiver with FSK-to-OOK conversion for biomedical implants," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 11, pp. 2748–2758, Nov. 2015.
[8] J. Bae, L. Yan, and H.-J. Yoo, "A low energy injection-locked FSK transceiver with Frequency-to-Amplitude conversion for body sensor applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 928–937, Apr. 2011.
[9] R. Adler, "A study of locking phenomena in oscillators," *Proc. IRE*, vol. 34, no. 6, pp. 351–357, Jun. 1946.
[10] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.
[11] Y.-L. Tsai, J.-Y. Chen, B.-C. Wang, T.-Y. Yeh, and T.-H. Lin, "A 400MHz 10Mbps D-BPSK receiver with a reference-less dynamic phase-to-amplitude demodulation technique," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014.
[12] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.
[13] J. Ayers, K. Mayaram, and T. S. Fiez, "An ultralow-power receiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1759–1769, Sep. 2010.
[14] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.
[15] R. Ni, K. Mayaram, and T. S. Fiez, "A 915MHz, 6Mb/s, 80pJ/b BFSK receiver with–76dBm sensitivity for high data rate wireless sensor networks," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[16] J. Bae, N. Cho, and H.-J. Yoo, "A 490uW fully MICS compatible FSK transceiver for implantable devices," in *Proc. Symp. VLSI Circuits*, Jun. 2009, pp. 36–37.
[17] B. van Liempd, M. Vidojkovic, M. Lont, C. Zhou, P. Harpe, D. Milosevic, and G. Dolmans, "A 3 W fully-differential RF envelope detector for ultra-low power receiver," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, vol. 2012, pp. 1496–1499.
[18] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb. 1991.
[19] H.-G. Seok, O.-Y. Jung, A. Dissanayake, and S.-G. Lee, "A 2.4GHz,–102dBm-sensitivity, 25kb/s, 0.466mW interference resistant BFSK multi-channel sliding-IF ULP receiver," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C70–C71.
[20] V. Dabbagh Rezaei and K. Entesari, "A fully on-chip 80-pJ/b OOK super-regenerative receiver with sensitivity-data rate tradeoff capability," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1443–1456, May 2018.

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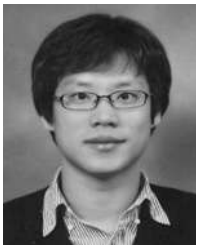

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