A Multichannel Pipeline Analog-to-Digital Converter for an Integrated 3-D Ultrasound Imaging System

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***Abstract*—An 8-channel 10-bit pipeline analog-to-digital converter, designed for use in an integrated three-dimensional ultrasound imaging system, has been implemented in a 0.25-μm CMOS technology. Two parallel multiplexing sample-and-hold stages are employed to multiplex a total of eight adjacent ultrasound channels, each sampled at 20 MHz. The sampled and multiplexed signals are fed into two parallel time-interleaved pipeline paths, each operating at 80 MHz. The two parallel pipelines are subsequently multiplexed into a single pipeline operating at 160 MHz to conserve area and reduce complexity. An experimental prototype of the proposed architecture occupies less than 4 mm^2 of active silicon area and shows a peak signal-to-noise-plus-distortion ratio more than 54 dB for a 2.1-MHz input signal, while dissipating only 20 mW of analog power per input channel from a 2.5-V supply.**

***Index Terms*—Analog-to-digital converter (ADC), mixed-signal integrated circuits, multichannel, multiplexing, pipeline analog-to-digital conversion, switched-capacitor circuits, ultrasound imaging.**

I. Introduction

REAL-TIME three-dimensional (3-D) ultrasound imaging for medical and underwater applications is an area of expanding research interest [1]. The realization of real-time 3-D ultrasound imagers is based on the use of phased two-dimensional (2-D) transducer arrays with individually addressable elements, together with signal conditioning, control, and high-speed data acquisition circuitry. The integration of the ultrasound transducer array with supporting electronics offers advantages such as improved sensitivity, reduced power dissipation and compact design, which expands the space of possible applications. Capacitive micromachined ultrasonic transducers enable the realization of 3-D ultrasound imaging arrays because they offer a practical means of implementing 2-D ultrasonic transducer arrays using silicon integrated circuit technology while providing both wide bandwidth and high sensitivity, as well as the potential for integration with supporting circuitry [2]–[4].

The integration of analog-to-digital (A/D) conversion as an integral part of an ultrasonic imaging array decreases the sensitivity of the system to analog circuit imperfections and eliminates the need for an unmanageable number of interconnects between the transducer array and the signal processing unit. On the other hand, the constraints on the power dissipation and area of the A/D interface are complicated by the need to process many channels in parallel.

In recent years, switched-capacitor pipeline A/D converters (ADCs) have emerged as an attractive approach for the implementation of Nyquist-rate, medium-to-high-resolution A/D conversion in wide-band applications [5]. Pipeline converters offer significant power and area advantages compared to flash and multistep architectures, at the cost of latency. In particular, pipeline stages can be scaled to reduce the overall power and area of the converter [7], [8]. Moreover, as illustrated by this work, later stages in the pipeline can be multiplexed to further conserve area.

This paper describes the architecture and circuit implementation for a multichannel pipeline ADC for use in an integrated 3-D ultrasound imaging probe. An experimental prototype integrated in a 0.25-μm CMOS technology is capable of digitizing eight parallel channels, each with an effective signal bandwidth as wide as 10 MHz, with 10 bits of resolution. The prototype circuit occupies less than 4 mm^2 of active silicon area and dissipates a total of 330 mW from a 2.5-V supply. Section II gives a brief introduction to multichannel pipeline A/D conversion as well as the techniques to reduce the complexity of the system. The proposed architecture and circuit implementations are described in Section III. Section IV summarizes the measured performance of the prototype.

II. Multichannel Pipeline A/D Conversion

In a multichannel system with a large number of input signals, such as an ultrasound imaging array, the use of a dedicated pipeline ADC for each channel can become prohibitively costly in terms of area and power. The following subsections describe the use of multiplexing in switched-capacitor pipeline ADCs to overcome this limitation.

A. Input Multiplexing

A potentially significant source of error in a high-resolution pipeline ADC implemented using switched-capacitor circuits is the thermal noise associated with the switched-capacitor networks, referred to as kT/C noise. For a given supply voltage, the overall resolution required of the converter constrains the total input-referred kT/C noise and, consequently, the size of the sampling capacitors of the pipeline stages. kT/C noise thus governs the area and power dissipation of a high-resolution switched-capacitor converter. However, this noise does not depend on the conversion rate or the sampling frequency, which suggests that for a multichannel system it should be efficient to

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share the stages of the pipeline among multiple inputs in order to reduce the overall area of the converter.

In general, for applications of pipeline converters where the quantization noise is comparable to the kT/C noise, area can be conserved simply by increasing the number of multiplexed input signals. However, the limit on conversion rate imposed by technology considerations constrains the number of input signals that can be multiplexed through the converter. The use of an architecture that maximizes the conversion rate of the pipeline converter is therefore essential.

B. Parallel Pipeline Multiplexing

Since the accuracy required for each stage in a pipeline ADC decreases further down in the pipeline, the area and power dissipation of the stages can be scaled [7], [8]. Another possibility for exploiting the decreasing accuracy required is to conserve area by sharing later stages in the pipeline.

In a pipeline converter, the output of each stage needs only settle to within the accuracy required of the remaining stages of the pipeline. The relaxed settling requirement enables operation of the later stages at higher conversion rates than the first stage. In particular, once the constraint on settling time requirement for a stage becomes less than half of that for the first stage, the remaining stages in the pipeline can be clocked at twice the conversion rate of the first stage. Thus, each of two parallel paths in a multichannel pipeline ADC can be multiplexed into a single pipeline converter operating at twice the sampling frequency of the preceding parallel paths. Since the later stages in a pipeline often cannot be scaled owing to parasitics, matching, and offset considerations, multiplexing provides for an additional reduction in area by sharing resources among multiple channels.

III. Architecture and Circuit Implementation

The proposed pipeline multiplexing has been employed in the design of a CMOS switched-capacitor 10-bit pipeline ADC for an ultrasonic imaging array readout application. Fig. 1 shows the architecture for digitizing the signals on eight 10-MHz ultrasound channels. The outputs from four adjacent channels are multiplexed through front-end multiplexing sample-and-hold (MSAH) circuits into two parallel 80-MHz pipeline paths comprising the first section of the converter. Since the design for 10-bit resolution is limited by kT/C noise, the area can be reduced by increasing the number of channels multiplexed into each conversion path. To maximize the number of multiplexed input channels through each path, a 1.5-bit-per-stage architecture is employed in the pipeline converters since it offers both the highest conversion rate and smallest area in comparison with architectures based on the use of higher resolution stages [9].

Since the resolution required for the later stages in the pipeline is relaxed, the two parallel paths of the converter are merged into a single path operating at twice the sampling frequency of the first section of the converter. This multiplexing is accomplished after the first five stages in the pipeline which resolve the most significant bits of the conversion. A single pipeline converter comprising four stages clocked at 160 MHz is then used to resolve the least significant bits for both parallel

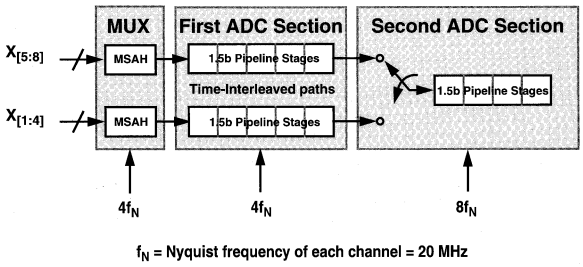

Fig. 1. Eight-channel 10-bit multiplexing parallel pipeline ADC.

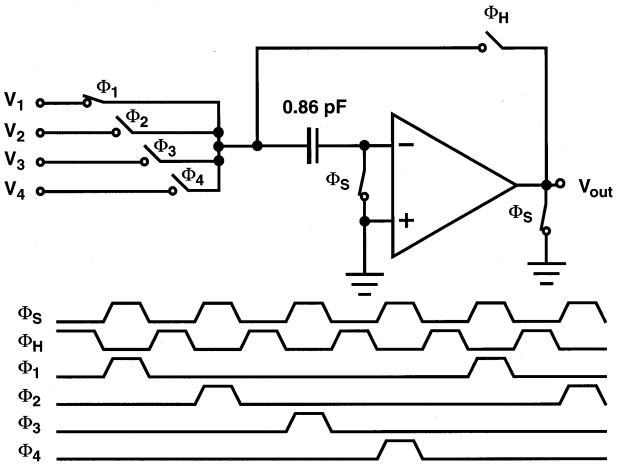

Fig. 2. Single-ended front-end multiplexing sample-and-hold simplified circuit and timing diagram.

paths. The two parallel paths in the first section of the converter are operated in a time-interleaved fashion to enable their subsequent multiplexing.

Mismatches among the parallel pipelines in the proposed architecture do not have the same effect as mismatches in time-interleaved converters [10] because each independent input signal experiences only a single path during the conversion. Path mismatches introduce channel-to-channel gain and offset variations, which can be corrected using post-conversion digital processing.

A. Front-End MSAH Amplifier

To ensure aperture-independent sampling, especially for high frequency input signals, a front-end MSAH amplifier is used to first sample four ultrasound signals that are then multiplexed to the first pipeline stage in the hold mode. Fig. 2 is a schematic of a single-ended version of the front-end MSAH circuit; the actual implementation is fully differential. Four input signals are sampled in sequence, as shown in the timing diagram, with an overall sampling frequency of 80 MHz, thus providing Nyquist-rate sampling for each of the 10-MHz bandwidth analog input channels. Each MSAH stage employs unity-gain feedback and is implemented as a differential circuit in order to suppress the effects of both supply noise and disturbances in the substrate.

The inputs from the ultrasound channels are sampled onto 0.86-pF sampling capacitors at the end of the tracking phase. To improve the linearity of the sampling operation, and to minimize clock feedthrough, the sampling switches

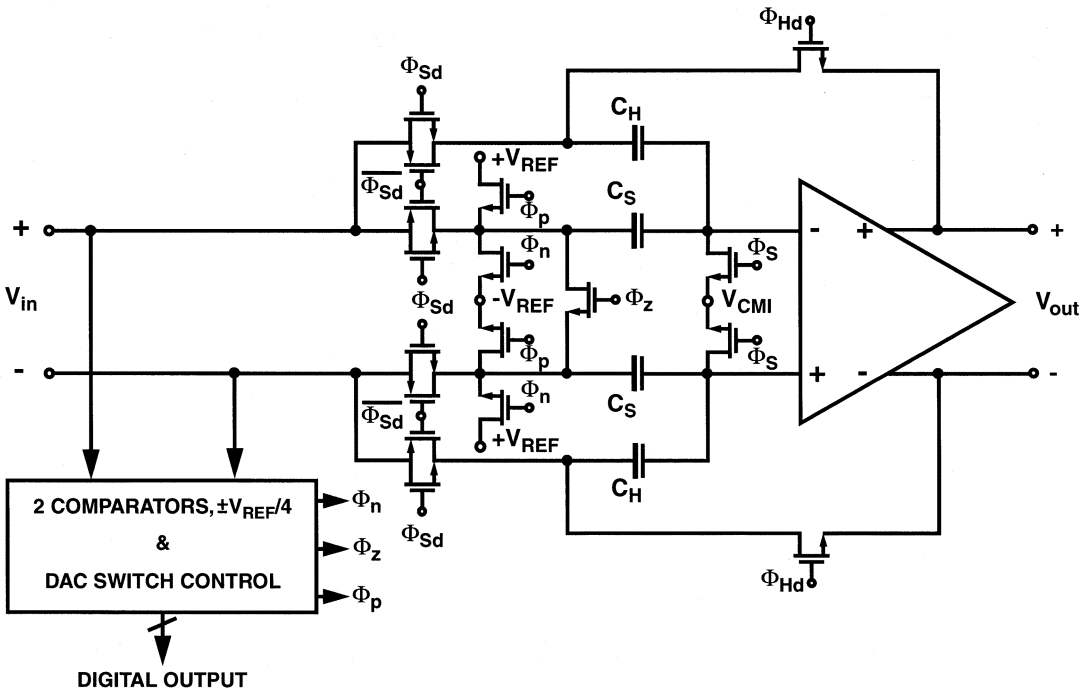

Fig. 3. Pipeline stage circuit schematic.

are implemented using CMOS transmission gates. The use of bottom-plate sampling minimizes the circuit's sensitivity to signal dependent charge injection, and the differential topology cancels, to first order, the remaining signal-independent switch charge injection.

B. Parallel Pipeline Stages

The pipeline stages are implemented as differential circuits with the holding capacitors also utilized as sampling capacitors during the tracking phase as shown in Fig. 3. Using the hold capacitors in the sampling phase allows a reduction in the size of the sampling capacitors and, therefore, increases the feedback factor. The larger feedback factor increases the closed-loop bandwidth of the interstage amplifier and also reduces the total output capacitance of the stage. The size of both sampling and hold capacitors is 0.43 pF.

To provide a large bandwidth with minimal power dissipation, the operational amplifiers in the pipeline stages are realized using the telescopic cascode topology shown in Fig. 4, [11]. Since in submicron technologies it is difficult to obtain both large gain and reasonable output swing, gain-boosting of the cascode devices is used to achieve a dc gain of more than 80 dB [12]. This ensures enough gain to suppress amplifier gain nonlinearity to the degree needed to achieve the required 10-bit accuracy. The same operational amplifier topology is employed in all pipeline stages, as well as the front-end MSAH circuits. Switched-capacitor common-mode feedback is used to bias the fully differential gain-boosted operational amplifiers. The gain-boosting amplifiers are also telescopic cascode circuits with capacitive common-mode feedback.

Since digital error correction is employed to correct for offsets in the comparators used to quantize the input to a pipeline stage, simple low-power dynamic comparators with a very low

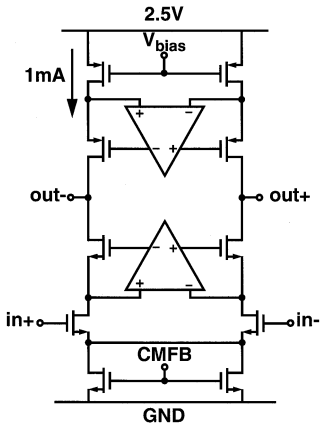

Fig. 4. Gain-boosted telescopic cascode amplifier.

input capacitance can be used [7]. Gain error, which is primarily the result of capacitor mismatch, can be adequately suppressed by a careful design and layout to meet the 10-bit accuracy requirement.

C. Multiplexing Pipeline Stages

Fig. 5 illustrates how the two 80-MHz parallel pipeline paths are merged into a single pipeline operating at 160 MHz. As shown in the timing diagram, multiplexing is only possible when the two parallel pipeline paths operate in a time-interleaved manner. Also, the clocks Φ_{11} and Φ_{12} fall after the falling edge of the multiplexing clock, Φ_{21}.

Owing to the relaxed noise constraints in the later stages of the pipeline, the capacitor sizes in the multiplexed pipeline are reduced by a factor of two. The capacitor scaling not only reduces the area of the converter but also decreases the load

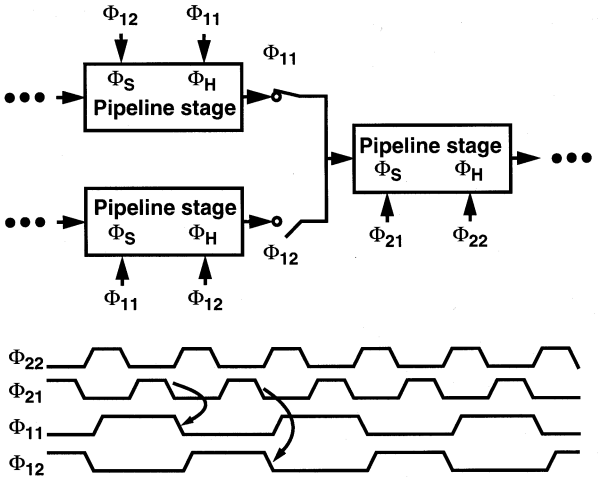

Fig. 5. Pipeline stage multiplexing and clock timing diagram.

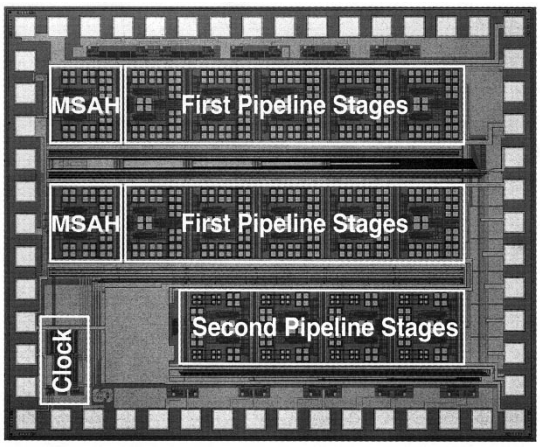

Fig. 6. Die photo.

capacitances presented to preceding stages in the pipeline, thereby improving their settling responses.

The overall ADC is controlled with two-phase nonoverlapping clocks $\Phi_{11}, \Phi_{12}, \Phi_{21}$, and Φ_{22} and their delayed replicas; the delayed replicas are used to minimize signal-dependent charge injection. The rising edges of each clock phase and its delayed version are aligned to maximize the time for settling of the interstage amplifiers in the hold mode.

IV. Measurements

An experimental prototype has been fabricated in a 0.25-μm, five-metal CMOS technology. The circuit occupies 2.2×1.7 mm^2 of active silicon area while the sampling and holding capacitors are constructed using stacks formed with metal layers 2 through 5. A die photo of the pad-limited chip is shown in Fig. 6.

A differential low-swing clock signal operating at 320 MHz is brought on chip and amplified to full-rail levels. Two divide-by-two frequency dividers then generate the 50% duty-cycle 160- and 80-MHz clock signals. The converter was tested with fully differential sinusoidal inputs provided to the chip by means of external baluns. The multiplexed digital output data were acquired with a logic analyzer for further digital processing, including digital error correction, and the performance was assessed using fast Fourier transform and code density techniques [14].

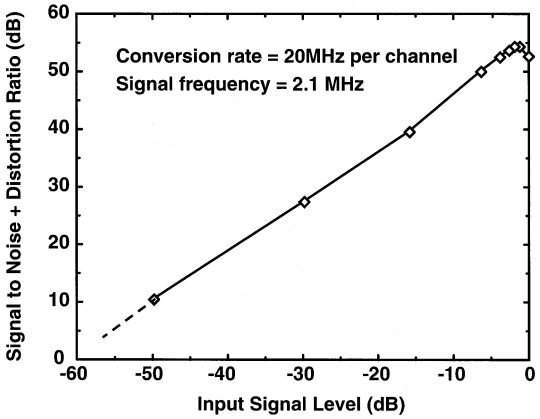

Fig. 7. SNDR versus input signal level.

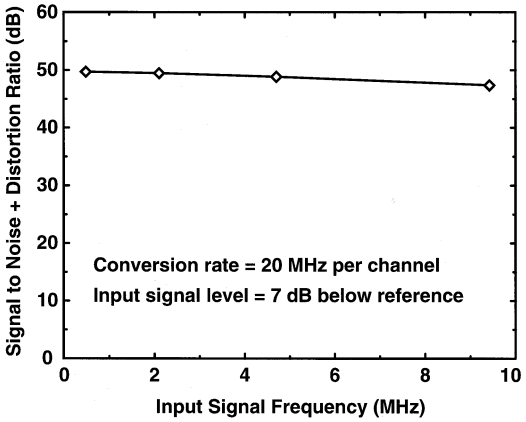

Fig. 8. SNDR versus input signal frequency.

TABLE I
Measured ADC Performance

Supply voltage	2.5 V
Number of input channels	8
Sampling rate per channel	20 MHz
Peak SNDR(@2.1MHz)	54.3 dB
Peak SNR(@2.1MHz)	56.8 dB
Peak absolute DNL(@2.1MHz)	0.25
Peak absolute INL(@2.1MHz)	0.88
Crosstalk	-70 dB
Power Dissipation	
Digital including output drivers	170 mW
Analog per channel	20 mW
Total	330 mW
Active die area	3.74 mm^2
Technology	CMOS 0.25µm

The measured signal-to-noise-plus-distortion ratio (SNDR) versus input level is shown in Fig. 7 for a single input channel. The measured peak SNDR is greater than 54 dB for a 2.1-MHz input signal, where 0 dB corresponds to a sinusoidal input with a peak-to-peak amplitude of 1 V. Fig. 8 shows the SNDR as a function of input frequency for an input signal level of -7 dB. The crosstalk between channels has been measured to be better than -70 dB when 2.1- and a 5-MHz input signals are applied to two adjacent channels, both with an input level of -6 dB.

The measured performance of the experimental prototype is summarized in Table I.

V. Conclusion

A multichannel pipeline ADC has been designed for use in an integrated 3-D ultrasound imaging probe. Multiplexing is employed to reduce the area of the overall data acquisition system. In general, multiplexing is beneficial in terms of conserving area when the performance of a pipeline ADC is limited by the error sources that are independent of the conversion rate. Although the architecture proposed herein was designed for ultrasound imaging applications, the converter can be utilized to implement A/D interface for other multichannel systems. Moreover, the multiplexing technique can be employed in other types of multistage ADCs, such as cascaded sigma–delta modulators.

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