

A Multilevel Bottom-up Optimization Methodology for the Automated Synthesis of RF Systems

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Abstract— In recent years there has been a growing interest in electronic design automation methodologies for the optimization-based design of radiofrequency circuits and systems. While for simple circuits several successful methodologies have been proposed, these very same methodologies exhibit significant deficiencies when the complexity of the circuit is increased. The majority of the published methodologies that can tackle radiofrequency systems are either based on high-level system specification tools or use models to estimate the system performances. Hence, such approaches do not usually provide the desired accuracy for RF systems. In this work, a methodology based on hierarchical multilevel bottom-up design approaches is presented, where multi-objective optimization algorithms are used to design an entire radiofrequency system from the passive component level up to the system level. Furthermore, each level of the hierarchy is simulated with the highest accuracy possible: electromagnetic simulation accuracy at device-level and electrical simulations at circuit/system-level.

Index Terms— bottom-up design methodology; radio-frequency; automated design; multi-objective optimization; surrogate modeling

I. INTRODUCTION

RADIO FREQUENCY (RF) circuits are considered to be a bottleneck in automated system synthesis [1]. In RF, circuit/system design is highly intuitive, rather than systematic and structured as in e.g., digital circuits. Also, RF design relies heavily upon the designer know-how. Furthermore, RF circuits

usually need very time-consuming simulations, such as electromagnetic (EM) simulations, in order to accurately model passive devices such as inductors and transformers, which are key elements in RF design.

Since the world is evolving towards 5G wireless communications and the Internet of Things (IoT) becomes a trending topic in today's electronics, RF systems are becoming more complex, with higher integration needs and harder-to-obtain specifications. Today's setback is that designers' productivity rate is insufficient to cope with the advances in integrated circuit specifications, therefore leading to a design gap. In order to overcome this design gap, new design methodologies have to be developed that can help the designer improve his/her productivity.

During the past fifteen years, several optimization-based methodologies have been reported for the automatic design of RF circuits [2]–[19]. Most of them address the synthesis of basic building blocks, e.g., power amplifiers or low noise amplifiers [2]–[14], in some cases considering parasitic effects and process variations. Moreover, and because of the high cost of EM simulations, passive devices, like inductors and transformers, are, instead, usually evaluated with analytical (i.e., fast) but inaccurate models, something that could lead to a fatal impact in how accurately circuit performances end up being evaluated [11]. Other works do address RF system-level synthesis but, however, relying on high-level description tools or approximated models for performance evaluation and, therefore, lack sufficient accuracy [15]–[19].

In consequence, in order to tackle complex RF circuits and solve the accuracy issues mentioned above, this work presents a design methodology that follows a divide-and-conquer strategy, which is based on hierarchical circuit partitioning and bottom-up (BU) composition of lower-level blocks. Furthermore, each level of the hierarchy is simulated with the highest accuracy possible: EM accuracy at the device level (using an efficient state-of-the-art machine learning technique [20]), and electrical simulations at the circuit/system level, using smart simulation techniques that do not degrade the efficiency of the entire synthesis. In [12], this BU design methodology was successfully applied between the passive and

Manuscript submitted in July 25, 2018. Revised December, 4, 2018. Accepted December, 28, 2018. This work was supported in part by the P12-TIC-1481 Project (funded by Junta de Andalucía) and in part by the TEC2013-45638-C3-3-R and TEC2016-75151-C3-3-R Project (funded by the Spanish Ministry of Science, Innovation and Universities and ERDF). F. Passos acknowledges the same ministry for supporting his research activity through the grant BES-2014-068216.

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the circuit level to design a low noise amplifier. However, to the best of the authors' knowledge, the work presented here is the first automated BU methodology to reach a system level design (e.g., RF front-end receiver) with highly accurate performance evaluation from the device up to the system level.

A second contribution of this paper is that it demonstrates the reusability of inductor and circuit information by using the same performance models for different system level specifications. Finally, a last contribution is the detailed comparison with other partitioning strategies for the same specifications, simulation tools and optimization techniques.

The rest of this paper is organized as follows. Section II details previous efforts made on RF system synthesis, i.e., circuits with higher complexity than the building blocks in [2]-[14]. Section III presents the proposed methodology. Section IV provides the experimental results coming from the application of the proposed methodology to the design of a typical RF system. The proposed methodology is further validated in Section V, by comparing it against other partitioning strategies. Finally, in Section VI, conclusions are drawn.

II. PREVIOUS WORKS ON RF SYSTEM SYNTHESIS

From the early 2000's up to the last few years, most efforts aimed at RF system-level design were focused on high-level system specification tools, architecture comparison tools and RF budget analyzers [15]-[17]. Such tools were commonly used to select the desired system architecture based on the needed system performances. Afterwards, the performances were distributed among the circuits constituting the system, using either optimization processes based on behavioral models [15],[16] or analytical equations [17]. As power consumption minimization is essential for optimal system design, in some cases a power consumption estimation model was used [15],[17]. The main disadvantage of such tools is their inability to consider all circuit nonlinearities. Since they are based on simple behavioral models or equations, it may be difficult to guarantee that the specifications imposed by the tools will be eventually achieved at the device level. Therefore, when designing lower-level circuits, the designer may face some difficulties reaching the desired performances, and, thus, re-design cycles are unavoidable. Eventually, since the high-level specifications do not entirely match the device-level simulations, the designer can choose to over-design the RF system in order to reduce the re-design cycles. However, this would ultimately lead to sub-optimal designs (e.g., circuits with higher power consumption than strictly required).

Some other approaches have tried to reach the lower circuit sizing level. In [18], the circuit specifications provided by the tool in [16] are used to size a low-noise amplifier (LNA) and a mixer. The circuit performances are estimated using first-order analytical equations, that do not take into account all non-idealities. Furthermore, ideal models are used for the passive components. Therefore, these components have to be synthesized after the circuit design, and there is no guarantee that the value required for the passive is achievable in the adopted technology. As reported in [18], some components had

to be iteratively tuned by more than 50% from its initial value in order to meet the circuit specifications.

Another attractive approach starts from a manual coarse design [19]; then, models linking LNA and mixer performances (estimated using electrical simulation) to the circuit variables are generated using sparse regression techniques. An optimization algorithm is then used to generate Pareto fronts of the optimal performance trade-offs of each circuit block and a polynomial fitting is used to obtain equations relating the performances of the Pareto front. Optimization at the system level is performed using the Pareto front equations of the blocks to constrain the search space. However, the developed models are local, only covering 20% of the design space around the initial coarse design and, therefore, the circuit optimization is not expected to yield globally optimal results, being instead more focused on local optimization around the initial design. Furthermore, as in [5], the performance models are built using ideal passive components (with the designer having to ultimately synthesize these components) and only NF, gain and IIP₃ are considered for the performance of the blocks, leaving out important performances such as power consumption.

In some other cases, optimized RF blocks were connected together to obtain an RF frontend but no real system optimization was performed [9],[10]. What is more, in most cases the models for the passive components are of the analytical nature whose typical inherent inaccuracies can make the synthesis process unsuccessful [11] thus calling for new re-design iterations.

Therefore, it is possible to conclude that:

- There is a lack of tools and methods to estimate system performances with the utmost accuracy at all levels, from the device level up to the system level, and to overcome the accuracy problems of performance/behavioral models, analytical equations, etc., reducing or avoiding in this way re-design iterations.
- There is a lack of tools and methods to perform device/circuit/system optimization in order to find globally optimal designs, therefore enabling the minimization of performances such as power consumption and area.
- There is a lack of tools and methods to fully synthesize RF systems and provide the sizing of all components.

Thus, to address these deficiencies, this paper describes an accurate and efficient methodology to design RF systems.

III. PROPOSED MULTILEVEL BOTTOM-UP DESIGN METHODOLOGY FOR SYSTEM SYNTHESIS

The proposed methodology avoids re-design iteration issues by using BU design approaches (subsections A and B) and uses accurate models for passive components, in order to attain the utmost accuracy at each level of the system design (subsection C).

A. Multilevel BU Circuit Design

The design of an RF circuit can be considered as an optimization problem, mathematically formulated as:

$$\begin{aligned} & \text{minimize } f(x); & f(x) \in R^m \\ & \text{subject to } g(x) \leq 0; & g(x) \in R^k \\ & x \in \Omega \end{aligned} \quad (1)$$

where $f(x)$ is a vector with m objective functions, $g(x)$ is a vector with k constraints and x is a vector with n design variables on the search space Ω . When designing a circuit, where only one performance is minimized or maximized ($m=1$) the problem can be solved with a single-objective optimization algorithm. When trade-offs between two or more objectives are to be explored ($m>1$), then a multi-objective optimization algorithm can be used.

In the multi-objective case, a solution a is said to constrain-dominate solution b if and only if a has a smaller constraint violation than b , or, if all constraints are met, $f_i(a) \leq f_i(b)$, for every $i \in \{1, \dots, m\}$ and $f_j(a) < f_j(b)$ for at least an index $j \in \{1, \dots, m\}$. A point $y \in \Omega$ is Pareto-optimal if it is not dominated by any other point in Ω . The set of all Pareto-optimal points in the search space is known as the Pareto set and the corresponding points in the objective space is the Pareto-optimal front (POF).

In BU design methodologies, the complete system is decomposed into two or more hierarchical levels; then, the design starts at the lowest level and composes the results up the hierarchy until reaching the system level. In this type of design methodologies, multi-objective optimization algorithms are commonly used so the information passed to the upper level is not a single design solution but rather a POF representing the best trade-offs available for a given circuit topology (e.g., phase noise vs. power consumption in a voltage-controlled oscillator (VCO)). This approach ensures that the designs considered at all levels are feasible and that no re-design cycles are required.

This type of BU methodology has been successfully applied in two-level hierarchical design, as in [21]. More recently, these BU methodologies have been exploited in RF circuit design by splitting the design of the circuit and the device levels [12]. In this work, a BU methodology is developed for the entire system-circuit-device hierarchy, as shown in Fig. 1, for the design of an RF front-end.

Since we are interested in obtaining POFs in order to compose a system up the hierarchy, the Non-dominated Sorting Genetic Algorithm (NSGA-II) is used [22]. NSGA-II is a multi-objective optimization algorithm based on the evolution of a set

of solutions (i.e., individuals) along a certain number of iterations (i.e., generations). The combination of Pareto dominance with the maximization of the minimal crowding distances aims at promoting convergence and diversity of the solutions. The RF circuit design methodologies considered in this paper do not exploit any particular characteristic of NSGA-II and, therefore, this algorithm could be substituted by any other multi-objective optimization algorithm.

Apart from avoiding re-design cycles, there are several other motivations for using BU design methodologies:

1) Optimal Circuit Trade-Offs

In BU design methodologies, each low-level device/circuit design space is reduced to only optimal solutions, representing the best trade-offs for the selected objectives and the device/circuit topology (i.e., the POF). This means that when designing a given higher-level block that contains a low-level device/circuit, the optimization algorithm is only performing a design space exploration in an already optimized design space (the device/circuit POFs previously obtained). This fact improves, considerably, the efficiency of the entire optimization as well as the convergence of the optimizations, because the algorithm no longer has to search in unusable/sub-optimal design areas.

2) Hierarchical Reusability of Lower-Level Blocks

Another motivation for using BU design methodologies is that it facilitates the hierarchical reusability of lower-level blocks. Since in BU design methodologies the lower-level blocks are designed first, the obtained POFs can be stored and used afterwards in the composition of any other system or the same system with different specifications. For example, this means that for the front-end depicted in Fig. 1, the inductor topologies and each individual circuit (LNA, VCO and mixer), have to be optimized only once. Afterwards, the front-end can be optimized for another communication standard without having to perform any additional low-level optimization. Again, this highly improves the efficiency of the methodology.

3) Low-Level Topology Selection

It is also possible to consider several device and circuit topologies for each optimization. Thus, all levels of the BU hierarchy can be implemented with different topologies and, therefore, while performing the system synthesis, the optimization algorithm can combine not only different circuit designs but also different circuit topologies (all selected from pre-generated POFs) [21].

The above-mentioned features provide the basis for an efficient and highly dynamic optimization-based multilevel BU methodology which can tackle highly complex systems.

B. Composing the System up the Hierarchy

While composing the system up the hierarchy, the lower-level POFs have to be explored because they represent part of the search space in the higher-level optimizations. Therefore, an important issue in BU design methodologies is how to search through these low-level POFs when optimizing higher-level blocks. This issue is important because searching these low-level POFs poses a problem to the optimization algorithms.

Evolutionary algorithms use mutation operators for local

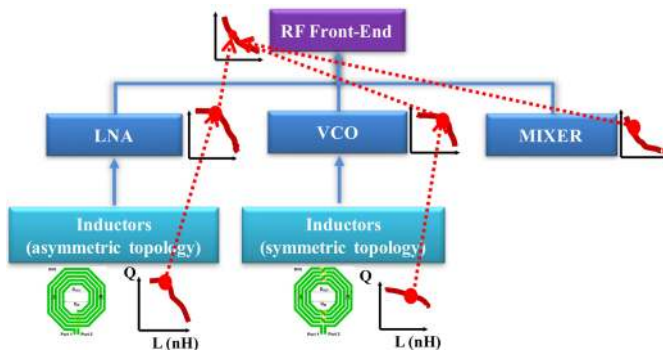


Fig. 1. BU design methodology for the specific case of an RF front-end

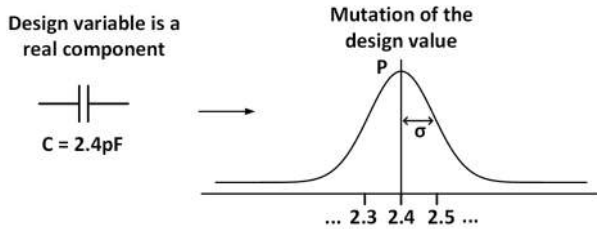


Fig. 2. Illustrating the mutation operation for regular design variables.

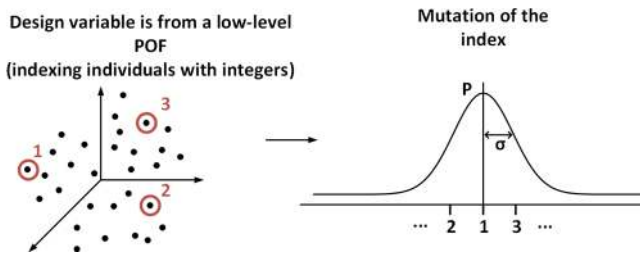


Fig. 3. Illustrating the mutation operation for indexed variables.

search in the design space, where a slight movement in the design space represents a small change in component parameter e.g., transistor width, capacitance value, resistance value, etc. A small component variation (e.g., capacitor value changes from 2.4pF to e.g., 2.5pF, as illustrated in Fig. 2), is usually associated to a small variation in the objective and constraint values of the circuit these components are part of.

When considering low-level POFs in a high-level optimization, and in order to allow the optimization algorithm to search the low-level POFs, the simplest solution is to assign an integer value to each individual of the low-level POF and use this integer (so-called index value) as a design variable during the optimization. The range of this new design variable, the index variable, would be the number of individuals in the low-level POF. The problem, however, is that this index variable does not have any information on the performances of the low-level individual, and therefore, individuals with index 1, 2 or 3, may be in completely different areas of the design space (see Fig. 3). Hence, while performing mutation around individual 1, the algorithm can jump to individual 3, which is in a completely different area of the design space and may cause a large variation in the objectives and/or constraints of the system this low-level circuit is part of. As a consequence, the mutation operation is transformed into a completely random variation, that can hamper the convergence of the optimization.

In order to solve this problem, and realizing that a POF generated for N design objectives is a hypersurface of dimension $N-1$, a set of $N-1$ coordinates can be used to represent the POF. Therefore, instead of assigning only one index to the individuals in low-level POFs, the individuals of each POF can be sorted by their performances and mapped into a matrix with $N-1$ dimensions. This operation can be seen in Fig. 4, where a set of 2 coordinates is given to each individual of a 3-D POF. By doing so, each individual of a low-level POF can be represented by a set of coordinates instead of a single index variable. Thus, the designs in each POF are organized by

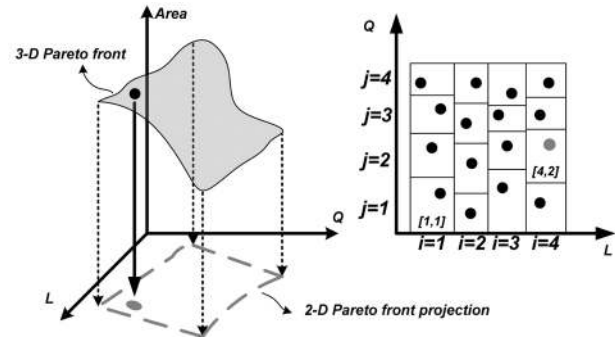


Fig. 4. Illustrating the mapping of each inductor into a two-coordinate matrix.

its performances in such a way that the mutation operator can be efficiently used. The matrix coordinates are then used as design variables in the upper level optimization [23].

C. Accurate Inductor Modeling

One of the most important subjects in the design of RF circuits/systems is how accurate the device models are. While for transistors, resistors and capacitances, the foundry usually provides sufficiently accurate models, inductors are still a bottleneck due to their distributed effects and parasitics. Traditionally, designers use EM simulations in order to estimate inductor performances, as in [7]. However, including EM simulations in optimization-based approaches, where thousands of EM simulations have to be performed, leads to impractical optimization times. Some approaches, on the other hand, use analytical models, as in [3]. Still, although efficient, these models tend to be highly inaccurate and therefore cause huge shifts in the circuit performances as shown in [11]. Therefore, new modeling strategies, based on machine learning and surrogate models, have been developed in the last few years that are both extremely accurate and efficient, and therefore more suited to be used with optimization-based approaches [24]. Surrogate modeling is an engineering method used when the performances of interest of a complex system cannot be easily measured or, as in this case, when the alternatives are too time consuming (e.g., EM simulations) or too inaccurate (e.g., analytical models). Surrogate models are able to acquire the behavior of a system from a limited number of smartly chosen data points. After learning the system behavior, the model is able to predict how the system will respond to any given input, and predict its output. Surrogate models have been used in the literature, for instance, to model circuit performances [25] or device variability [26]. The work presented here uses an extremely accurate surrogate model that has less than 1% error when compared with EM simulations [20]. Furthermore, the model can describe the inductors through its S-parameters for an accurate frequency behavior description, which can be used in any commercial electrical simulator (e.g., SpectreRF, EldoRF, HspiceRF). In this work, this model is used in order to

accurately and efficiently design and optimize inductors.

IV. EXPERIMENTAL RESULTS

The methodology presented in Section III can be applied to any RF system, technology process and communication standard. In this Section, experimental results are shown for a low-IF RF front-end receiver in a 0.35- μm CMOS technology for the ISM band. The selection of the technology process in these experiments was motivated by the availability of foundry data for EM simulation. In Fig. 5, an RF receiver is depicted. For the experimental results in this paper, the RF front-end composed of an LNA, a VCO and a mixer is considered.

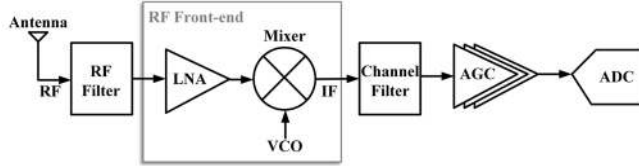


Fig. 5. Complete RF receiver signal chain with focus on the RF front-end (LNA, VCO and Mixer).

As shown in Fig. 1, the methodology is based on hierarchical partitioning and composition, from the device level up to the system level. By ensuring that each low-level device/circuit design performs well for the entire 2.4-2.5GHz ISM band we ensure that any receiver working in this band can be designed (e.g., Bluetooth, Bluetooth Low Energy, ZigBee, Wi-Fi/WLAN, etc.).

A. Device-Level Synthesis

The first step of the methodology is to optimize the devices that correspond to the lowest hierarchical level of the system. In this work, the two inductor topologies illustrated in Fig. 6 are considered: an octagonal asymmetric topology and an octagonal symmetric topology. The search space for the inductors is presented in Table I (for both topologies, where N is the number of turns of the inductor, D_{in} is the inner diameter and W is the turn width.). The minimum inner diameter and turn width, as well as the grid size, are imposed by the design rules of the technology process. Upper limits are reasonably high values, well beyond what is commonly found and is of interest for cost reasons. The same occurs for the number of turns: higher numbers are never used, especially for relatively high frequencies. These inductors are designed by using surrogate models that present less than 1% error when compared to EM

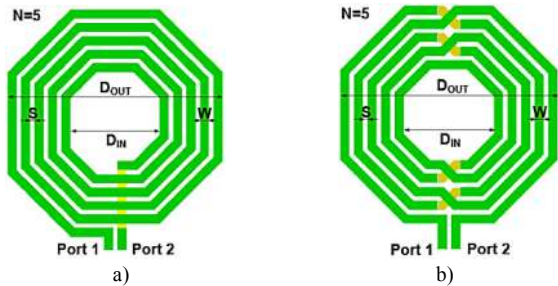


Fig. 6. a) Octagonal asymmetric topology used in the LNA and b) octagonal symmetric topology used in the VCO.

TABLE I
DESIGN VARIABLES FOR THE INDUCTORS.

N			D_{in} (μm)			W (μm)		
Min	Max	Grid	Min	Max	Grid	Min	Max	Grid
1	8	1	10	300	0.05	5	25	0.05

simulations, which is an extremely accurate estimation that will introduce an also extremely negligible deviation when simulating the circuit performances.

Two optimizations, one for each topology, were carried out with three design objectives: maximization of the quality factor, Q , maximization of inductance, L , and minimization of the area. Both optimizations were performed with 1000 individuals and 80 generations and several constraints were imposed to guarantee the proper behavior of inductors at the entire frequency band. These constraints are:

$$\begin{cases} \text{area} < 400\mu\text{m} \times 400\mu\text{m} \\ \left| \frac{L_{@WF} - L_{@WF+0.05\text{GHz}}}{L_{@WF}} \right| < 0.01 \\ \left| \frac{L_{@WF} - L_{@WF-0.05\text{GHz}}}{L_{@WF}} \right| < 0.01 \\ \left| \frac{L_{@WF} - L_{\text{at } 0.1\text{GHz}}}{L_{@WF}} \right| < 0.05 \\ Q_{@WF+0.05\text{GHz}} - Q_{@WF} > 0 \end{cases} \quad (2)$$

where $L_{@WF}$ and $Q_{@WF}$ are the inductance and quality factor at the working frequency (WF), which, in this case, is the center of the ISM band (2.45GHz) [20]. The inductance and quality factor at any frequency can be easily obtained from the S-parameters [27]. The second and third constraint in (2) guarantee that the inductance is very flat around the WF. In addition, the fourth constraint guarantees that the inductance is sufficiently flat from low frequencies up to the WF (preventing in this way a significant inductance valley that typically appears in integrated inductors). The last constraint in (2) guarantees that the maximum of the quality factor is beyond the working frequency and, therefore, that the inductor self-resonance frequency (SRF) will still be at higher frequencies. The obtained POFs are shown in Fig. 7 and Fig. 8.

The individuals of these POFs represent fully-sized inductors

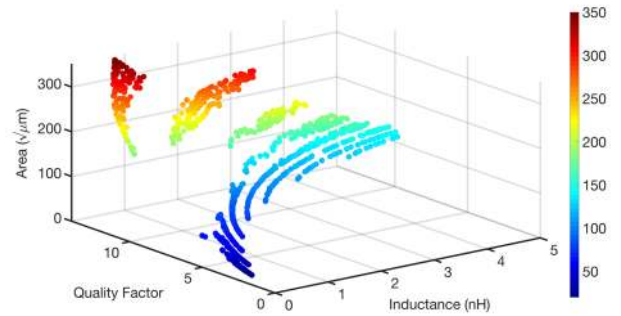


Fig. 7. POF of the inductor octagonal asymmetric topology. The color bar represents the area objective.

TABLE II
SPECIFICATIONS FOR THE LNA, VCO, MIXER OPTIMIZATIONS.

LNA Performance	LNA Specifications	VCO Performance	VCO Specifications	Mixer Performance	Mixer Specifications
S_{11} @ 2.45; 2.5; 2.55 GHz	< -12 dB	f_{osc}	> 2.45 GHz	CG @ 10 MHz	> 5 dB
S_{22} @ 2.45; 2.5; 2.55 GHz	< -12 dB	f_{osc}	< 2.55 GHz	CG @ 40 MHz	> 5 dB
S_{21} @ 2.45; 2.5; 2.55 GHz	Maximize (> 7 dB)*	PN @ 1MHz offset	Minimize (< -110 dBc/Hz)*	P_{DC}	Minimize (< 20 mW)*
k	> 1	P_{DC}	Minimize (< 20 mW)*	NF @ 10 MHz	< 20 dB
NF @ 2.45; 2.5; 2.55 GHz	Minimize	P_{OUT}	Maximize (> -2 dBm)*	NF @ 40 MHz	Minimize (< 20 dB)*
P_{DC}	Minimize (< 20 mW)*			IIP ₃	Maximize (> -15 dBm)*
IIP ₃	> -15 dBm			Port-to-Port Isolation	> 30 dB
Area (μm^2)	Minimize	Area (μm^2)	Minimize	Area (μm^2)	Minimize

*Although this performance is given as an objective a constraint is also imposed.

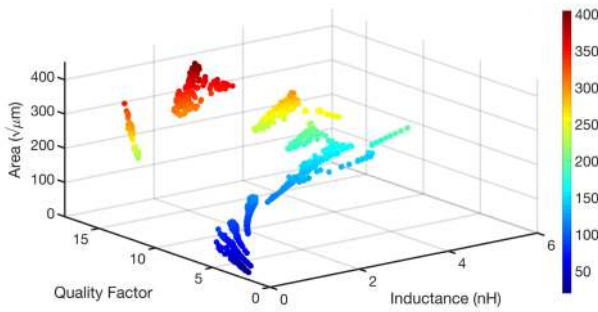


Fig. 8. POF of the inductor octagonal symmetric topology. The color bar represents the area objective.

whose performances (L, Q and Area) correspond to the best trade-offs for the selected technology and working frequency. This means that, for a given L value, inductors with the smallest possible area and highest Q values in this technology will be available in the POF. After the inductor optimization is performed, the inductor POFs are mapped into matrices, as described in Section III.B, and used as inductor search space in the following circuit optimizations.

B. Circuit-Level Synthesis

The second step in the methodology is to optimize the circuit-level blocks that compose the system. Therefore, in this subsection, the optimization of the three individual circuits (LNA, VCO and mixer) used in the RF front-end are illustrated. In our methodology, all circuits are simulated using SpectreRF (although the methodology is completely independent from the

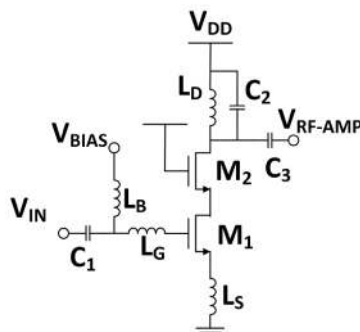


Fig. 9. Schematic of the LNA.

TABLE III
DESIGN VARIABLES FOR THE LNA OPTIMIZATION.

Variables	Min	Max	Step
$W_{1,2}$ (μm)	30	600	10
$l_{1,2}$	Fixed @ 0.35 μm		
V_{bias} (V)	0.001	1.5	0.001
Inductors	Selected from POF in Fig. 7		
$C_{1,2,3}$ (pF)	0.4	4	0.4

electrical simulator), providing therefore the utmost accuracy at each level of the hierarchy. As power and area will be optimization objectives at the receiver level, it is essential that they are also optimized at the circuit level for all RF blocks.

Regarding the LNA design, the circuit is intended to operate at any frequency of the ISM band (2.4-2.5GHz), with a supply voltage of $V_{DD}=2.5\text{V}$. The LNA topology considered is a source-degenerated LNA shown in Fig. 9. The LNA has several important performance parameters that need to be considered during the design process: noise figure NF, gain S_{21} , power consumption P_{DC} , third-order intercept point IIP₃, input matching coefficient S_{11} , output matching coefficient S_{22} , Rollet stability factor k (if smaller than 1, the LNA is potentially unstable) and the area occupation (extremely important as it is directly related to the manufacturing cost in IC technologies).

According to Friis's equations [28], for the design of an RF cascaded system, the NF of the LNA is the main contributor to the NF of the receiver; therefore, it should be minimized. In most of the reported optimization-based approaches, the calculation of the IIP₃ is usually avoided due to the needed power sweep, which is time consuming and degrades the efficiency of the optimization. In this work, a highly efficient technique is used in order to calculate the IIP₃, where no power sweep is needed [12]. The LNA optimization was performed with 800 individuals, 300 generations and had four objectives: maximization of S_{21} and minimization of area, NF and P_{DC} . The specifications are shown in Table II. Notice that in some cases, constraints have also been imposed on optimization objectives (e.g., lower constraint for gain or upper constraint for power). Although this is not strictly necessary, it helps the optimizer to avoid exploring search regions we are clearly not interested in. The search space is defined in Table III and the result of the optimization is shown in Fig. 10. Notice that, for this graphical representation, the 3-D plot is used for three objectives (S_{21} , NF

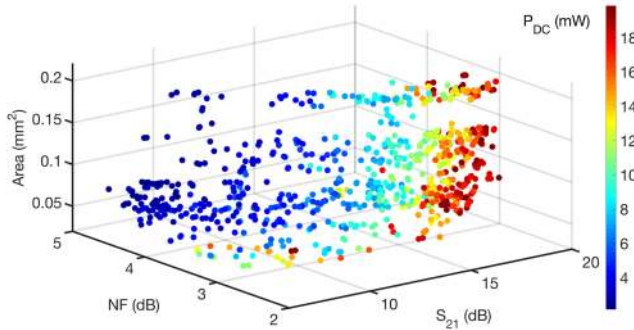


Fig. 10. Obtained LNA POF. The color bar represents the power consumption, the fourth objective in the optimization.

and area), while a color bar is used for the fourth objective (P_{DC}).

With this LNA POF, the designer is in possession of the best trade-offs available for the selected performances, which means that for a given value of S_{21} , the LNA with lowest NF, P_{DC} and area is available in the POF. After the circuit optimization, the POF has to be mapped into a matrix for higher level optimizations. Since this POF has 4 objectives, it has to be mapped into a matrix using three indexes.

The next circuit considered for optimization is the VCO. This circuit is intended to oscillate at a frequency of 2.5GHz with a supply voltage of $V_{DD}=2.5V$. From the several VCO topologies available, in this work, a cross-coupled double-differential VCO, depicted in Fig. 11, has been considered. The most important VCO performances are: oscillation frequency (f_{osc}), phase noise (PN), power consumption (P_{DC}), output swing (P_{OUT}), which is an important performance parameter especially when the VCO is connected to a mixer, and, finally, the area occupation.

The VCO optimization was carried out with 300 individuals, 100 generations and four objectives: maximization of P_{OUT} and minimization of PN, P_{DC} and area. The specifications are shown in Table II, the design variables are listed in Table IV and the optimization results are plotted in Fig. 12. As in the previous example, the resulting POF has the best trade-offs for the chosen performances, which means that, for a given value of P_{DC} , the VCO with lowest PN, area and highest P_{OUT} is available

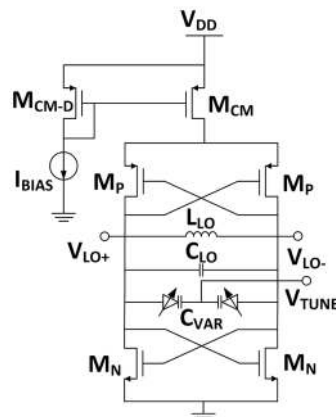


Fig. 11. Schematic of the VCO.

TABLE IV
DESIGN VARIABLES FOR THE VCO OPTIMIZATION.

Variables	Min	Max	Step
$w_n (\mu m)$	10	200	10
$w_{p,CM-D,CM} (\mu m)$	10	150	10
$I_{n,p,CM-D,CM}$	Fixed @ 0.35 μm		
$I_{bp} (mA)$	0.1	5	0.1
$w_{Cvar} (\mu m)$	Fixed @ 6.6 μm		
$I_{Cvar} (\mu m)$	Fixed @ 0.65 μm		
Inductors	Selected from the POF in Fig. 8		
Row _{Cvar} , Col _{Cvar} ⁽¹⁾	4	12	1
C (pF)	0.4	4	0.4

⁽¹⁾ Row_{Cvar} is the number of fingers per row and Col_{Cvar} is the multiplicity of the varactors.

in the POF. Since four objectives were considered, the VCO POF is also mapped using three indexes.

The last circuit block considered for optimization is the down-conversion mixer, which converts the RF frequency (coming from the LNA) into a lower intermediate frequency (IF). The Gilbert cell mixer topology shown in Fig. 13 has been used. The mixer optimization is performed setting an ideal RF signal at 2.46GHz and an ideal local oscillator (LO) signal at 2.5GHz. The mixer operates with a supply voltage $V_{DD}=2.5V$. The most important performance parameters for the mixer are: conversion gain (CG), P_{DC} , IIP_3 , which is extremely important in mixers because it usually dominates the IIP_3 of the entire cascaded RF system [28], Port-to-Port isolation, which is a measure of how well the ports (RF, LO and IF) are separated

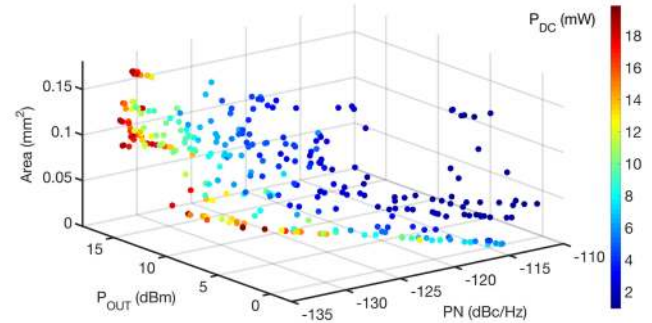


Fig. 12. Obtained VCO POF. The color bar represents the power consumption, the fourth objective in the optimization.

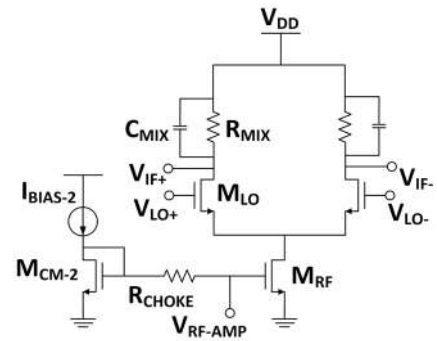


Fig. 13. Schematic of the mixer.

TABLE V
DESIGN VARIABLES FOR THE MIXER OPTIMIZATION.

Variables	Min	Max	Step
$W_{LO,RF,CM-2}$ (μm)	10	200	10
$L_{LO,RF,CM-2}$	Fixed @ 0.35 μm		
I_{BIAS-2} (mA)	0.1	1.5	0.1
R_{CHOKE} (Ω)	10	24,000	10
R_{MIX} (Ω)	10	18,000	10
C_{MIX} (pF)	0.3	3	0.3

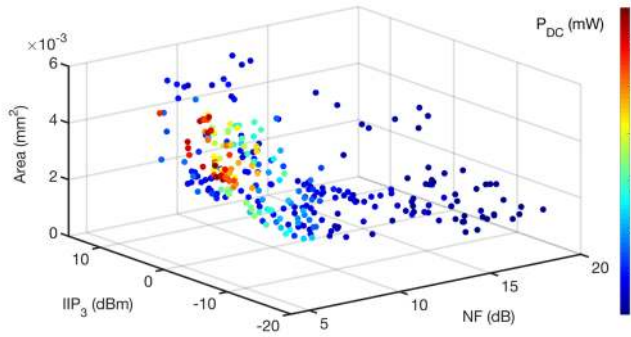


Fig. 14. Obtained POF of the Gilbert cell mixer. The color bar represents the power consumption, the fourth objective in the optimization.

from each other in terms of unwanted signal coupling (typically, an isolation of 30dB is in most cases considered “high isolation”), NF, which is not a very critical performance in mixers because in cascaded systems it is divided by the LNA gain [28], and, finally, the area occupation.

The mixer optimization was performed with 300 individuals, 100 generations and four objectives: maximization of IIP_3 and minimization of P_{DC} , NF and area. The desired specifications are shown in Table II, the design variables are listed in Table V and the results of the optimization are depicted in Fig. 14. In the mixer, CG and NF constraints in Table II were imposed at two different IF frequencies in order to guarantee that the constraints are met for an IF band from 10 to 40MHz. Since four objectives were considered, the mixer POF is also mapped using three indexes.

C. Receiver Front-end Synthesis

After obtaining the POF for each individual circuit (LNA, VCO and mixer), the next optimization is performed at the third hierarchical level in order to compose the individual blocks that together empower the best front-ends for a given communication standard. Due to the hierarchical POF reusability that the methodology enables, the previous optimizations (passives and circuits) only have to be performed once for a given frequency band. Afterwards, the POFs can be stored and reused for any given communication standard that operates in the same frequency band. In the following, the receiver synthesis is illustrated for two different standards: Bluetooth and Wi-Fi.

1) Bluetooth Receiver Synthesis

It was shown in [29] that the specifications for the Bluetooth standard (IEEE 802.15.1) yield $NF < 8.79dB$ and

TABLE VI
DESIRED SPECIFICATIONS FOR THE RECEIVER FRONT-END OPTIMIZATIONS.

Front-end Performance	Bluetooth standard	Wi-Fi standard
CG @ down-frequency	> 12 dB	> 12 dB
CG @ up-frequency	> 12 dB	> 12 dB
P_{DC}	Minimize < 40 mW	Minimize < 40 mW
NF @ down-frequency	< 8.79 dB	< 5.64 dB
NF @ up-frequency	< 8.79 dB	< 5.64 dB
IIP_3	> -10.35 dBm	> -20.3 dBm
Area (μm^2)	Minimize	Minimize

$IIP_3 > -10.35dBm$. Furthermore, assuming that the receiver is designed for an IoT application, the receiver area and P_{DC} need to be kept at a minimum. The constraints and objectives for the receiver synthesis are shown in Table VI. The optimization was performed with 160 individuals and 60 generations.

Similar to the mixer optimization, the receiver CG and NF constraints were ensured at two different IF frequencies in order to guarantee that the constraints are met for the IF band. However, while for the mixer optimization an ideal LO of 2.50GHz was used, now, for the receiver, a real VCO is used, which may oscillate between 2.45-2.55GHz (as imposed in the VCO constraints). Therefore, the up- and down-frequency will vary depending on which VCO is used in the receiver (the desired IF is then selected by tuning the VCO using V_{TUNE} shown in Fig. 11). The result of the optimization can be seen in Fig. 15. Each red dot in Fig. 15 represents a fully-sized RF receiver front-end, compliant with the Bluetooth standard with its performances obtained with accurate EM simulation of the inductors and electrical simulation accuracy at higher levels.

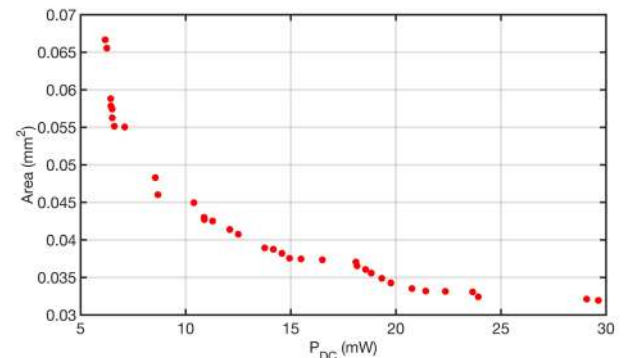


Fig. 15. POF of the front-ends compliant with the Bluetooth standard.

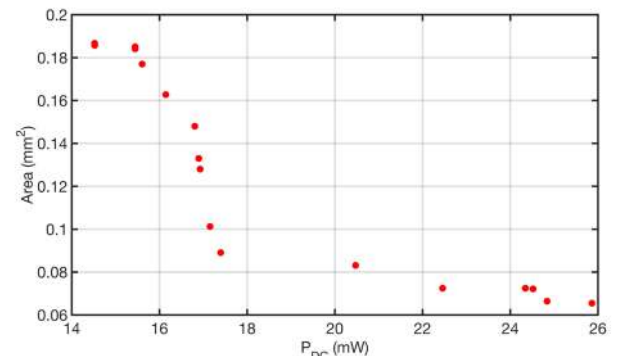


Fig. 16. POF of the front-ends compliant with the Wi-Fi standard

TABLE VII
CONSTRAINTS FOR THE DIFFERENT OPTIMIZATION STRATEGIES. ILLUSTRATING THE NUMBER OF DESIGN VARIABLES AND CONSTRAINTS.

Performance	BU		CIR		IND	
	Bluetooth	Wi-Fi	Bluetooth	Wi-Fi	Bluetooth	Wi-Fi
S_{11} (dB)	x ^a	x	<-12	<-12	<-12	<-12
CG (dB)	>12	>12	>12	>12	>12	>12
NF (dB)	<8.79	<5.64	<8.79	<5.64	<8.79	<5.64
IIP ₃ (dBm)	>-10.35	>-20.30	>-10.35	>-20.30	>-10.35	>-20.30
f_{osc} (VCO) (GHz)	x	x	>2.45	>2.45	>2.45	>2.45
f_{osc} (VCO) (GHz)	x	x	<2.55	<2.55	<2.55	<2.55
Port-to-port isolation (dB)	x	x	>30dB	>30dB	>30dB	>30dB
Inductor Constraints	x	x	x	x	yes ^b	yes
P_{DC} (mW)	<40	<40	<40	<40	<40	<40
P_{DC}	Minimize	Minimize	Minimize	Minimize	Minimize	Minimize
Area	Minimize	Minimize	Minimize	Minimize	Minimize	Minimize
Optimization settings						
Total number of design variables	9 ^c	9	33	33 ^d	38 ^e	38
Total number of constraints	6	6	15	15	40	40

^aThe constraints marked with an x were already imposed at device/circuit level and do not need to be imposed at the circuit/system level.

^bThe inductor constraints are the ones imposed in order to ensure that the inductors are in the flat-BW zone, as explained in Section IV.A.

^cThe design variables of the BU strategy are the indexes of the matrix mapping for each circuit.

^dAll design variables of the LNA, VCO and mixer are considered. The inductors are passed as indexes from the matrix mapping.

^eAll the design variables of the LNA, VCO and mixer, plus the geometrical parameters of inductors are considered.

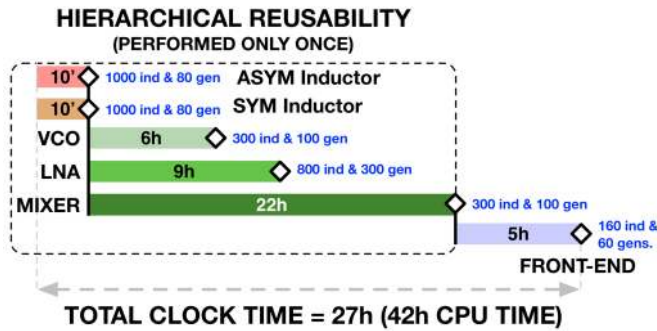


Fig. 17. Timeline of the entire proposed design methodology for the design of RF systems.

2) Wi-Fi Receiver Synthesis

It was shown in [29] that the required performances for the Wi-Fi standard (IEEE 802.11b) are $NF < 5.64$ dB and $IIP_3 > -20.3$ dBm. The constraints and objectives of the receiver synthesis are shown in Table VI and the result from an optimization process with 160 individuals and 60 generations is presented in Fig. 16.

By comparing Fig. 15 and Fig. 16, it is possible to observe that the Bluetooth POF achieves designs with lower area and power consumption, which is due to the more relaxed NF specification of the Bluetooth standard.

The total design time for the entire methodology can be seen in Fig. 17. As mentioned before, one of the very important advantages of the proposed approach is its hierarchical reusability. This feature allows the designers to reuse, over and over, the lower level POFs in order to optimize the front-end for different standards. Therefore, if a POF for another standard is desired, the designer only needs to perform the system-level optimization without the need for re-optimizing each individual circuit. After that, in a few hours, several fully-sized RF front-ends (or any other system, since the methodology can be applied to other blocks) are ready for its physical implementation.

V. COMPARISON TO OTHER PARTITIONING STRATEGIES

In order to assess the advantages of the proposed methodology, this section reports several comparisons to other alternative partitioning strategies.

A. Device-Level Hierarchical Optimization

In this sub-section, a device-level optimization methodology is applied. This optimization is considered at the device-level, without any type of hierarchical partitioning. Therefore, all circuits and passives are sized during the optimization. This optimization, denoted as IND, is the most straightforward. Thus, the search space includes all the design variables shown in Table I for the inductors, and in Tables III to V for the circuits. During the optimization, surrogate models of the S-parameters are used to evaluate the performances of both the asymmetric and symmetric inductors considered during the sizing process [11]. Accurate performances of the complete front-end are simulated with an electrical simulator.

Several factors can be considered for comparison of the different methodologies: accuracy, quality of the results and efficiency. In this work, all methodologies use the same evaluation techniques and therefore the accuracy is the same. Therefore, the comparison will be centered around efficiency and quality of the final results. Since the BU strategy presented in Section III and the IND strategy have different number of design variables and design constraints, as shown in Table VII, a CPU criterion will be used in order to compare both strategies. It was shown in Fig. 17 that the BU strategy needed around 42 hours of CPU time to get the 2D POF of the front-end, including the time needed to optimize all the passives, circuits and system. Therefore, for the IND strategy, the optimization was allowed to run with the same number of individuals of the system-level optimization of the BU approach and for a large number of generations. The POF obtained at several generations and corresponding CPU times is compared to the BU approach in Fig. 18 for the Bluetooth standard and in Fig.

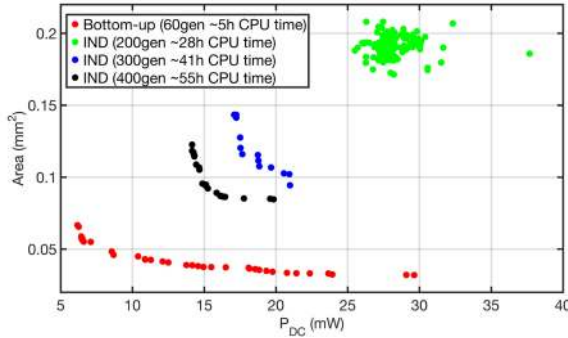


Fig. 18. Comparison between the POFs obtained with the BU and IND strategies for the Bluetooth standard.

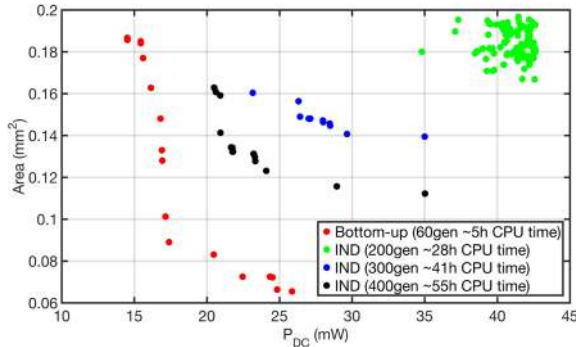


Fig. 19. Comparison between the POFs obtained with the BU and IND strategies for the Wi-Fi standard.

19 for the Wi-Fi standard.

The CPU time for the entire BU strategy is 42 hours. However, due to the low-level hierarchical reusability, the optimization of the passives and circuits only has to be performed once. Therefore, the actual system synthesis takes only 5 hours of CPU time. In both Fig. 18 and Fig. 19, the BU POF is represented with red dots, while the green dots, represent the population of solutions of the IND approach at generation 200, where the consumed CPU time was around 28 hours. At this generation, a cloud of points, rather than an actual POF (for both Bluetooth and Wi-Fi) is obtained. Therefore, the optimization was allowed to evolve further for 400 generations (black dots in Fig. 18 and Fig. 19), extending to a total CPU time of 55 hours. Despite this high CPU time figure, the IND strategy cannot achieve the same results as the BU strategy since the POFs obtained for both standards are completely dominated by the POFs obtained using the BU strategy. Therefore, this comparison clearly endorses the usage of BU strategies over IND strategies for RF circuit design.

From the optimization times shown in Fig. 18 and Fig. 19 it may be perceived that there is a lack of proportionality between the BU and IND CPU optimization times. The BU strategy performs 9,600 electrical simulations of the front-end (160 individuals along 60 generations), and the IND strategy performs 64,000 simulations (160 individuals along 400 generations). In the IND strategy, roughly 7 times the number of simulations are performed but the optimization time is more than 7 times that of the BU strategy. This is due to several reasons:

- In the IND strategy, the inductors are designed during the optimization. Since surrogate models are being used, the S-parameter files have to be created at each generation, whereas in the BU strategy, these files are created a priori only for the inductors of the POF.

- The IND strategy has to perform more simulations at each generation in order to comply with all front-end constraints. In order to evaluate the front-end input matching, an S-parameter analysis must be performed, and, in order to consider the port-to-port isolation, a periodic transfer function analysis must be performed too. In the BU strategy, these analyses are performed during the simulation of the LNA and the mixer, relieving, therefore, the front-end optimizations from these simulations.

- The time needed for the periodic steady-state analysis highly depends on the individual design being simulated, because the analysis needs to converge to a steady-state. Whereas in the BU strategy every single LNA, VCO and mixer designs are fully functional, in the IND strategy, especially during the initial stages of the optimization, there may be many designs that take longer to converge.

From the obtained Bluetooth and Wi-Fi POFs, and the previous given drawbacks of the IND strategy, it may be concluded that the BU strategy is more efficient and achieves much better results than the IND strategy.

B. Circuit-Level Hierarchical Optimization

The IND strategy has the drawback of having to design the inductors in an online style (i.e., during the optimization), thus considerably increasing the number of design variables and constraints imposed. Therefore, it may be possible that the optimization algorithm struggles to converge to optimal solutions. In order to study the effect of such online inductor design in the entire front-end optimization, a circuit-level hierarchical optimization, denoted as CIR, is performed, where the circuits composing the front-end (LNA, VCO and mixer) are sized at the same optimization. However, the inductors are designed previously and passed as a POF.

Again, since a fair comparison between BU and CIR strategies is difficult, the optimization was run with the same number of individuals but for a longer CPU time in order to inspect the convergence of the optimization. The results of the optimization can be seen in Fig. 20 for the Bluetooth standard and in Fig. 21 for the Wi-Fi standard.

The front-end POF obtained with the BU strategy is illustrated with red dots in both Fig. 20 and Fig. 21. Green dots are used to depict the CIR POF at generation 200, reached after 25 hours of CPU time. It can be seen that the obtained POF is still far away from the one obtained with the BU strategy. The optimization was run up to 50 hours of CPU time, where the obtained POF is shown with black dots in Fig. 20 and Fig. 21. It is possible to observe that by just using the inductor POF, the obtained results are widely improved (e.g., see green dots in Fig. 18 and Fig. 20).

By comparing the BU and the CIR results for the Bluetooth standard it is reasonable to conclude that, despite the longer CPU time of the CIR approach (50 hours), the obtained POF is completely dominated by the POF obtained with the BU

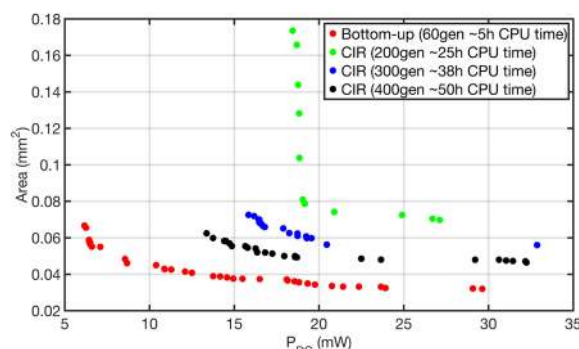


Fig. 20. Comparison between the POFs obtained with the BU and CIR strategies for the Bluetooth standard.

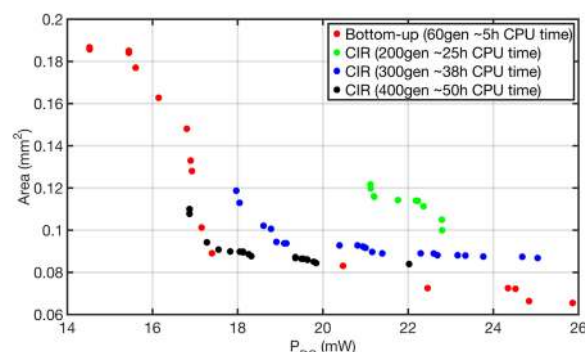


Fig. 21. Comparison between the POFs obtained with the BU and CIR strategies for the Wi-Fi standard.

strategy. For the Wi-Fi standard, shown in Fig. 21, the CIR optimization with 400 generations slightly overlaps the BU POF; however, the BU POF is much wider and achieves lower power consumptions and lower areas.

VI. CONCLUSIONS

In this work, a multilevel BU circuit design methodology was described and applied to the design of an RF system composed of an LNA, a VCO and a mixer. By using such multilevel BU strategy, different circuits can be assembled to design an RF system. Furthermore, each level of the hierarchy is simulated with the utmost accuracy possible: EM accuracy at device-level and electrical simulations at circuit/system-level. Also, the methodology developed in this work, promotes the hierarchical reusability of low-level POFs. Moreover, the methodology proved to be highly efficient and presented superior results when compared to other alternative partitioning and synthesis strategies. To the best of the authors' knowledge, the design of an RF system, using a multilevel BU approach, has been demonstrated for the first time in this work.

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