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A Multilevel Fault-Tolerant Power Converter for a Switched Reluctance Machine Drive

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ABSTRACT Reliability in the electrical drives is becoming an important issue in many applications. In this context, the reliability associated to the switched reluctance machine (*SRM*) is also an important area of research. One of the major problems, that strongly affect its operation, are drive power semiconductors faults. Typical power converter topologies used in *SRM* drives cannot handle faults in their power semiconductors. So, this paper presents a power converter topology that provides fault-tolerant capabilities to the drive under a switch fault. This power converter will be used considering that a change in the direction of the current that flows in the *SRM* windings does not affect the behavior of the machine. Besides that, the proposed power converter will allow to generate multilevel phase voltages in order to apply different voltage levels as function of the *SRM* speed. A laboratory power converter was developed to test the SRM drive in normal and faulty conditions. From the obtained results it was possible to verify the fault-tolerant capability of the drive under switch faults in different devices and failure modes. It was also possible to confirm the multilevel operation of the drive.

INDEX TERMS Switched reluctance motor (SRM), multilevel power converter, fault tolerance, bidirectional current excitation.

I. INTRODUCTION

The Switched Reluctance Machine (*SRM*) is a very well-known electrical machine, but, when compared with other electrical machines, not so used in common applications. The reason for this is mainly related with some disadvantages that are associated to this machine, like the need of a power converter, the existence of torque ripple and acoustic noise, or the need of an encoder. However, in recent years, with new technological advances and the contribution of control techniques, those disadvantages are becoming less significant, particularly when compared with the many advantages associated to this machine, such as robustness, simple construction, high reliability, reduced maintenance and low cost production in a massive way. Thanks to this, the interest for *SRM* has increased in the last decades, operated as motor or generator, namely in applications such as electric vehicles, aircrafts and wind power generators, among others [1]–[8].

An important feature associated to *SRM* drives is its fault-tolerant capability, which is related to the main topic of this paper. Some literature can be found on this important issue [9]–[23]. In [9] the proposed solution for fault-tolerant capability goes through the modification of the converter topology under short-circuit fault condition. The modification of the switching states of the power semiconductors are proposed in [10]. Other approaches use artificial neural networks and genetic algorithms [11], the analyses of different fault tolerant situations with traditional Proportional-Integral (*PI*) and Integral-Proportional (*IP*) regulators [12], fault detections schemes [13] or even the modification of the geometry of the system using dual-channel *SRM* [14]. In [15] a mutually coupled dual three-phase *SRM* is used and

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in [16]–[18] it is adopted, as fault tolerant control strategy, the modification of the control parameters and references. Approaches using phase current reconstruction schemes were proposed in [19], [20]. In [20] it is presented an active fault-tolerant position sensor controller to increase the *SRM* drive reliability regarding position sensor failures. Other fault-tolerant topology schemes based on the special design of the motors were also proposed to mitigate or solve this problem [22], [23].

Another aspect associated to the fault tolerant operation in power electronic converters is the fault detection of the power semiconductors [24]–[26]. This part is usually essential for the change of the power converter operation from normal to fault tolerant. In this way, special attention is also being devoted to fault diagnosis, involving *SRM* drives. New fault diagnosis schemes, based on the analysis of the power converter supply current, were presented in [27]–[30]. In [31] a new algorithm for real-time diagnosis of power converter faults in *SRM* drives is proposed, using only the measured phase currents and in [32] it is presented an online fault diagnostic algorithm for power converter faults in *SRM* drives based on high frequency voltage signal injection. Other papers deal with other *SRM* related topics. A comprehensive analysis of *SRM* drive under different fault conditions is presented in [33] and a method to predict the performance characteristics under normal and fault operating conditions is presented in [34]. The use of *ANN* is also used in [35] to model stator winding fault.

The use of multilevel converters is now considered as a very interesting solution for several applications [36], [37]. A study in which is presented a multilevel inverter fed SRM for torque ripple minimization is proposed in [38]. In [39] the advantages of using an asymmetric three level neutral point diode clamped converter, when compared with the conventional two-level asymmetric half-bridge converter, are presented. An asymmetric NPC converter in which inherent dc-link voltage-boosting capacitors was incorporated for a four-phase SRM drive is presented in [40]. In [41] a multilevel converter is proposed to have an enhanced performance at high-speed range where, as generally recognized, the driving performance of *SRM* will be degraded because of the back electromagnetic force (*EMF*). In [42], [43] the torque ripple minimization is addressed based on multi-level converters. The advantages of using multilevel converters in *SRM* drives are also highlighted in [44]. In [45] it is described a novel fault-tolerant converter that takes the advantages of multilevel output converter in the normal operation mode and exploits the switching states that are destructive for the conventional *NPC* topology and use them for fault-tolerance purposes. An approach in which was developed a multilevel converter with Boost capability was also proposed by [46]. In [5] it is presented an integrated multilevel converter of SRMs fed for plug-in hybrid electric vehicle applications. One problem that in some multilevel topologies must be addressed is the balance of the DC voltage capacitors through the redundant switching states. This problem was addressed in some inverters like the NPC, T-Type and Flying capacitor [47]–[49]. A NPC multilevel topology adapted for the SRM presenting redundant states is also presented in [35], [39]. However, these works do not address the problem of using the redundant states for the balance of the capacitors or transistor fault condition.

As previously verified, several topologies and approaches have been proposed for *SRMs* with fault-tolerant capability. However, practically all of them have been proposed taking into consideration the unidirectional current flow in the windings of the motor. This is characteristic of this motor. However, as will be shown in the next section, this motor can also still rotate in the same direction and with the same torque characteristic, inverting the current flow in the windings. Thus, this work proposes a fault tolerant topology that is based in this concept, allowing in this way to propose a power converter with lower complexity, without mechanical or static relays and using classical modules that allows a reduced cost. On the other hand, the number of proposals regarding fault tolerant topologies with full fault tolerant capability for SRMs and multilevel operation is extremely reduced. Thus, besides the fault tolerant capability, the proposed topology also allows multilevel operation of the SRMs. Another issue that this work addresses is the problem related with the balance of the input capacitors. In this way, it is presented a proposal to use the redundant states for the balance of those capacitors in normal and fault tolerant condition.

II. SWITCHED RELUTANCE MACHINE

To describe the SRM operation principle it is necessary to recall that the reluctance of the magnetic circuit and its variations are dependent on the rotor position. In fact, *SRM* geometry and some constructive parameters, like the type of ferromagnetic material that is used, its thickness and lamination factor, directly influence the magnetic reluctance circuit. The variation of the magnetic reluctance in *SRM* is essential to have torque (reluctance torque) in this machine, and it can be properly controlled by accurately controlling the time of energizing and deenergizing stator phases. Its mathematical model is considered complex due to the nonlinearity of its magnetic circuit. For each phase, the *SRM* electrical equation can be expressed like (1), usually neglecting the mutual inductance, which means neglecting the magnetic influence among the phases.

$$u_j = R_j i_j + \frac{d\psi_j\left(\theta_r, i_j\right)}{dt} \tag{1}$$

where u_j denotes phase voltage, i_j phase current, R_j phase resistance, θ_r rotor position, j considered phase and $\psi_j\ (\theta_r, i_j)$ phase linkage flux. Eq. (1) can be rewritten as:

$$u_j = R_j i_j + \frac{\partial\psi_j\left(\theta_r, i_j\right)}{\partial i_j}\frac{di_j}{dt} + \frac{\partial\psi_j\left(\theta_r, i_j\right)}{\partial\theta_r}\omega_r \tag{2}$$

where the last term corresponds to the back *EMF*, depending on the rotor speed ω_r. This means that for high speed operation, the back EMF of the motor will present high values

and the input voltage should be even higher in order to assure phase current. This is a situation where a multilevel converter could be helpful imposing a high value of *DC* voltage. Particularly during the phase energizing and deenergizing periods, high voltage values are very desirable in order to minimize the commutation time between phases and the possibility of negative phase torque. For lower speeds the multilevel converter could also be very useful, particularly using lower voltage values, and so diminishing the switching frequency and consequently improving the efficiency level.

The *SRM* mathematical model should be completed by writing the equation for the torque developed by each phase (T_j). The total torque is obtained by adding, for each time instant, the torque developed by each phase. For each phase the torque is determined by the variation of the magnetic co-energy (W_C) produced in its magnetic circuit in relation to the variation of the rotor position and it is expressed as (3).

$$T_j\left(\theta_r, i_j\right) = \left.\frac{\partial W_C\left(\theta_r, i_j\right)}{\partial \theta_r}\right|_{i_j=const} \tag{3}$$

where the magnetic co-energy is defined by the following expression:

$$W_C\left(\theta_r, i_j\right) = \int_0^{i_j} \psi_j\left(\theta_r, i\right)\ di \tag{4}$$

The linkage flux of each phase can be expressed as:

$$\psi_j\left(\theta_r, i_j\right) = L_j\left(\theta_r\right)\ i_j \tag{5}$$

where the magnetic self-inductance coefficient (L_j) was introduced and it is considered, in this analysis, not dependent on the phase current, i_j. On the other hand, it depends on the rotor position and should be considered non-linear [50].

Using (5), the torque developed by each phase and represented in (3) can be rewritten as:

$$T_j\left(\theta_r, i_j\right) = \frac{1}{2}\frac{dL_j\left(\theta_r\right)}{d\theta_r} i_j^2 \tag{6}$$

which means that its value does not depend on the positive or negative signal of the phase current. This aspect is very important to support the methodology proposed in this paper.

The *SRM* is considered to have magnetic independence of the motor phases and can continue to operate despite partial failures occurring in the motor-converter unit. Such inherent fault-tolerant characteristic is useful in applications requiring high reliability, such as aircrafts or electrical vehicles. However, on the presence of faults, the speed variation and torque ripple increases, causing undesirable behavior.

III. PROPOSED CONVERTER WITH FAULT-TOLERANT CAPABILITY

There are several power converter topologies that can be used in *SRM* drives. However, the most used, and considered as conventional, is the asymmetrical half-bridge converter [4]. Using this topology is possible to apply three voltage levels $+V_{DC}$, *0* and $-V_{DC}$, depending of the switching states that are applied. Also, besides the limitation regarding the number of voltage levels, this converter does not present fault-tolerant capability. In fact, an open or short-circuit fault in one of the power semiconductors will have an important impact in the operation of the *SRM*. Due to these limitations, multilevel power converters have also been applied to *SRM*. One of the proposed multilevel structures is the neutral point clamped asymmetrical half-bridge converter (*NPC-AHB*). As presented in fig. 1, this topology consists of two controlled power semiconductors and one diode per leg, as well as two *DC* capacitors in serial connection with their common point connected to each of the legs through a clamped diode. With this topology is possible to extend the number of voltage levels that can be applied to the windings. In fact, it is possible to apply five voltage levels (two negatives, two positives and a zero voltage).

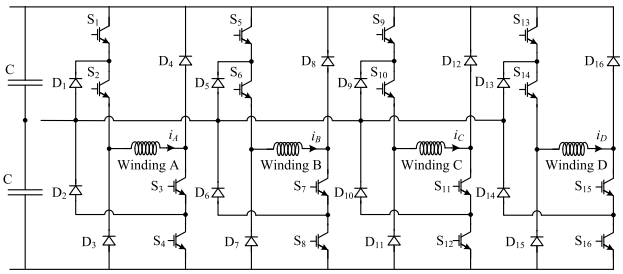

FIGURE 1. Neutral point clamped asymmetrical half-bridge converter (*NPC-AHB*) topology for *SRM* drives.

Besides the increase of voltage levels, this topology also provides some fault-tolerant capability. In fact, a short circuit in the outer transistors will not affect the operation of the *SRM*. However, if there is an open circuit fault in those transistors, then the applied voltage to the winding in the magnetization process will be limited to half of the *DC* bus voltage. A fault in the inner transistor will also have impact in the applied voltage to the winding. The most critical is when there is an open circuit fault, since in this case is not possible to magnetize the winding. Another critical issue is when there is a fault in one of the isolated diodes. This situation could lead to a seriously impact in the system, since a short-circuit will also originate another short-circuit in one of the capacitors or bus. Thus, a fault in a power semiconductor can lead to a fault operation in the phase winding and consequently the motor will not work as desirable due to important variations and limitations in the speed and torque.

With the purpose to provide a complete fault-tolerant capability to a fault in power semiconductors, instead of an asymmetrical half-bridge converter, it is proposed, in this paper, the use of a full bridge neutral point clamped converter, as presented in fig. 2. In accordance with this scheme, instead of two fully controlled switches and one diode four fully controlled power semiconductors with antiparallel diodes will be used. This topology results in a simple structure for the *SRM* drive since it is a standard in industry for classical electrical machine drives. This proposal is based on the principle that in this machine, the torque developed by each phase is a function

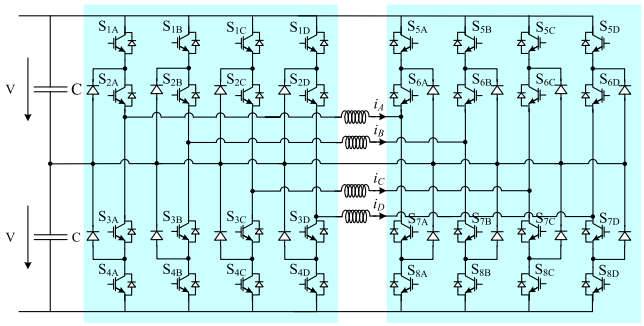

FIGURE 2. Proposed neutral point clamped converter with fault tolerant capability for *SRM* drives.

of the winding square current (eq. 6). Thus, the direction of the rotor movement is independent of the winding current direction allowing in this way to invert this current.

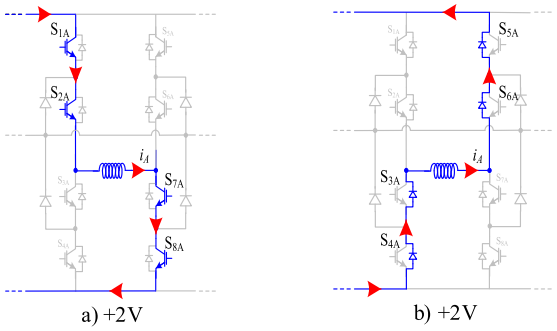

FIGURE 3. Operation modes for the proposed converter in normal operation for the maximum DC voltages.

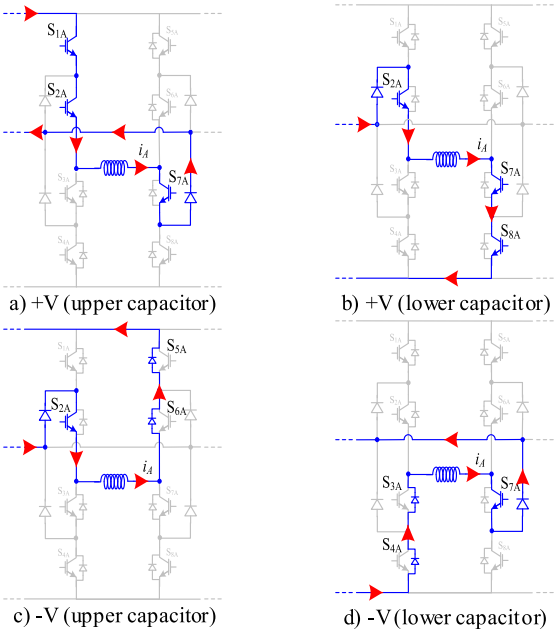

FIGURE 4. Operation modes for the proposed converter in normal operation for the intermediate DC voltages.

Considering the proposed power converter in normal operation, there are up to nine operation modes for each winding, depending of the operation point of the *SRM*. For example, when it is required to operate with the maximum *DC* voltages, two operation modes can be used (fig. 3 a) and b). When it is required half of the maximum *DC* voltage four operation modes can be used (fig. 4 a) b) c) and d)). However, it should be noted that in this case the voltage balance of the *DC* bus voltage capacitors should be ensured. This will be made by the redundant states when half of the *DC* voltage is applied (fig. 4). In fig. 5 presents three operation modes to achieve the zero voltage. For the inverted currents, it can be used a similar strategy.

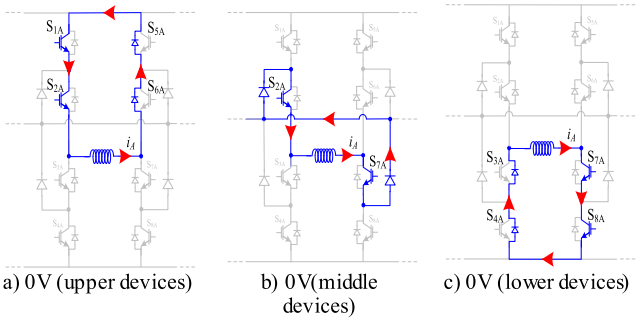

FIGURE 5. Operation modes for the proposed converter in normal operation to achieve zero voltage.

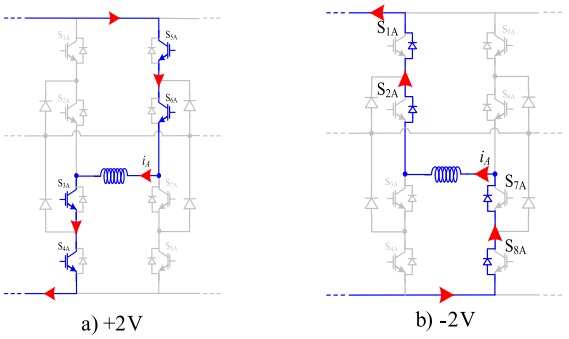

FIGURE 6. Operation modes for the proposed converter in fault tolerant mode (inversion of the current excitation) for the maximum DC voltages.

With the proposed topology for the *SRM* drive it is possible to obtain a high circuit reconfiguration capability, the through the possibility of using an approach based on the bidirectional current excitation. In healthy conditions the power converter works as the classical asymmetrical half-bridge converter. However, in case of a fault condition in one power semiconductor the topology can be reconfigured in order to invert the current excitation of the *SRM*. Associated to this situation there are also a total of nine operation modes for each winding, as shown in fig. 6, 7 and 8. Thus, for the operation at the maximum *DC* voltage, it can also be used two operation modes (fig. 6 a) and b)). For the situation in which it is required the application of half of the *DC* voltage, it must also be ensured the balance of the *DC* bus voltage capacitors through the redundant states.

From this analysis, it is possible to see the increased fault-tolerant capability regarding faults in power semiconductors,

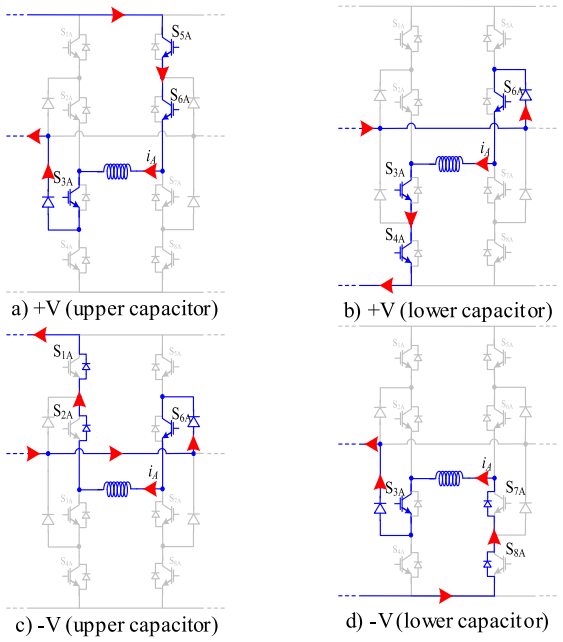

FIGURE 7. Operation modes for the proposed converter in fault tolerant mode (inversion of the current excitation) for the intermediate DC voltages.

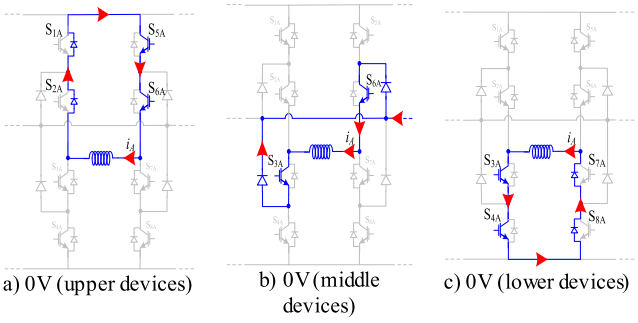

FIGURE 8. Operation modes for the proposed converter in normal operation (inversion of the current excitation) to achieve zero voltage.

since it is possible to change the direction of the winding currents (from positive to negative). This change can be realized through a change in the control of the switches in order to compensate the absence of the positive or negative voltage that should be applied to the machine winding. For example, if there is an open fault in switch S_{2A}, without change in control of the switches it is not possible to apply the required voltage to the winding of phase A.

IV. OPERATION IN FAULT-TOLERANTE MODE

As mentioned before, under a power semiconductor fault, the performance of the motor will be degraded. There are two major fault types, namely the open and short-circuit semiconductor failure. Normally the impact of these faults is different. In the case of an open-circuit semiconductor failure mode, the winding associated to this semiconductor cannot be magnetized anymore. In this way the *SRM* will work under the loss of that phase. This will originate an unbalanced and increased torque ripple. Regarding the short-circuit failure mode, the phase current associated to the semiconductor under fault will present large values. Due to this, the performance of the *SRM* will be seriously affected, since high values of negative torque can appear, as well as excessive winding heating.

To analyze the proposed power converter, it will be considered that under normal conditions the power semiconductors under control will be the upper ones of the legs associated to the left side of the windings and the lower ones of the legs associated to the right side of the windings (operation modes shown in fig. 3). In accordance with this, it will be considered that the windings' currents are positive. To analyze the power converter under fault and tolerant modes, it will be considered examples related with phase A.

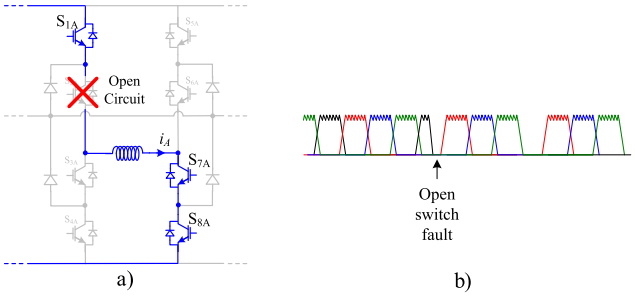

FIGURE 9. Impact of S_{2A} open-circuit failure: a) Power circuit; b) Winding currents before and after the fault.

If one of the inner controlled power semiconductors (S_{2A} or S_{7A}) presents an open-circuit failure, there is an interruption of the current in that winding (see fig. 9). Thus, to ensure full fault-tolerant capability, after the failure the winding currents should be inverted, since with the *SRM* in negative excitation condition, their performance will not present any kind of limitation. In this way, after the fault, power semiconductors S_{1A}, S_{2A}, S_{7A} and S_{8A} must be permanently turned off and power semiconductors S_{3A}, S_{4A}, S_{5A} and S_{6A} will be used to control the current of the winding (see fig. 10).

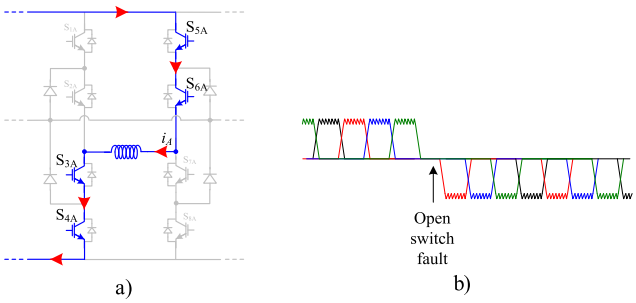

FIGURE 10. Operation in fault tolerant mode after a S_{2A} open-circuit failure (inversion of the current excitation): a) Power circuit; b) Winding currents before and after the failure.

In the case of an open fault in the outer controlled power semiconductors (S_{1A} or S_{8A}), there is no interruption of the current in that winding. However, there will be a limitation in the magnetization process since the applied voltage to the winding will be limited to half of the total *DC* voltage. Thus, for high speed operation modes, the phase under fault will

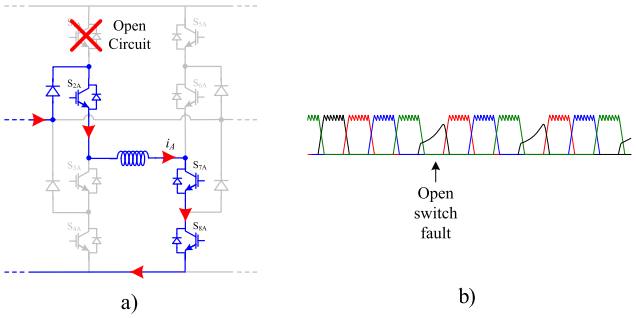

FIGURE 11. Impact of S_{1A} open-circuit failure: a) Power circuit; b) Winding currents before and after the fault.

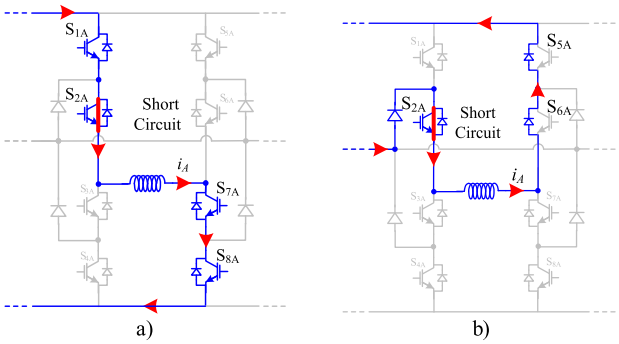

FIGURE 12. Impact of S_{2A} short-circuit failure in the demagnetization process: a) Magnetization mode; b) Demagnetization mode.

not be able to generate the required current due to the limited applied voltage to the winding (only half of the voltage). Fig. 11 shows the impact of this fault condition. However, this problem can also be overcome in an identical way of the previous fault, more specifically through the *SRM* in negative excitation condition.

In the case of a power semiconductor under a short circuit fault the behavior will be considerably different from an open circuit fault. Depending on the exact location of the faulty device, the impact on the performance of the *SRM* will be different. One of the failures that could affect the *SRM* is when there is a short-circuit fault in the outer controlled semiconductors (S_{1A} or S_{8A}). Considering for example a short circuit fault in semiconductor S_{1A}, the voltage applied to the winding can still be controlled through semiconductors S_{2A}, S_{7A} and S8A, since S_{2A} is in serial connection with S_{1A}. The impact of this fault will only be visible when is necessary to apply half of the maximum *DC* voltage through the control of the semiconductors S_{2A}, S_{7A} and S_{8A}. Due to this, in many operation modes the switching frequency of the leg under fault will increase. Moreover, this fault can be overcome in an identical way of an open circuit fault in which the *SRM* operates in negative excitation condition. If occurs a short circuit fault in one of the inner controlled power semiconductors, then there will be a different impact on the performance of the *SRM*. In this situation, the magnetization process will not be affected since it will be possible to apply the two voltage levels. However, there will be an impact in the demagnetization process, since only half of the maximum *DC* voltage is possible to be applied to the winding. For example, for a short-circuit fault in the power semiconductor S_{2A}, in the demagnetization process, the current will always flow through that semiconductor (see fig. 12). However, since the impact is only on the demagnetization process it is always possible to ensure the required current (which does not happen in the case of an open circuit fault in the outer controller power switches). Besides that, there is also another impact that this fault can originate. In this situation, the balance of the capacitor voltages can be affected, as will be verified in the next section.

In order to present a comparison with the existing multilevel power converter, it is presented a study about the theoretical probability of failure expected from both converters (*NPC-AHB* and proposed topology, as presented in Fig.1 and Fig.2, respectively) after the failure in the IGBTs of one phase (winding *A*). In this study it was considered both failure modes (open and short-circuit) separately and the capability to achieve the desired voltage level. In order to simplify this analysis, especially in the case of short-circuit failure, it was also considered that, for each failure mode, the next failures present the same mode. Reliability quantifies the probability of a system failing within a given time interval [0, t], i.e. it is a function of time, $R(t)$ [51]. For a constant failure rate component, λ, the reliability is usually determined by the following exponential distribution (7):

$$R(t) = e^{-\lambda t} \tag{7}$$

The reliability of stand-by redundancy systems with ideal switching without repair and identical and constant failure rates can be described by the Poisson distribution (8) [52].

$$R(t) = \sum_{k=0}^{n-1} \frac{(\lambda t)^2}{k!} e^{-\lambda t} \tag{8}$$

The probability of failure is then calculated by (9):

$$Q(t) = 1 - R(t) \tag{9}$$

The following tables present the estimated probability of failure after five years (43800 hours) of operation and with a constant failure rate of $\lambda = 10^{-6}h^{-1}$ for the *NPC-AHB* and proposed topology after the first failure regarding different failure modes, different power devices and desired voltages.

From this analysis, it is possible to conclude that the proposed solution is far more reliable regarding the open circuit failure mode, independent of the device under failure and desired voltage level.

Regarding the reliability over the short-circuit failure mode, the proposed topology is more reliable only when the device under failure is an outer device (e.g. S_{1A}, S_{3A}, S_{5A}, S_{8A}) or when is required to impose 0 V. For the remaining devices the reliability is the same.

TABLE 1. Estimated probability of failure to 5 year of operation after the first failure *NPC-AHB*.

	Open circuit failures			Short-circuit failure modes		
Device Failure	+2V	+V	0V	+2V	+V	0V
S_1	Fail	0.1231 (*)	0.0446	7.87E-5	1.84E-3 (*)	0.0446
S_2	Fail	Fail	0.0838	7.87E-5	0.0446	0.0838
S_3	Fail	Fail	0.0838	7.87E-5	0.0446	0.0838
S_4	Fail	0.1231 (*)	0.0446	7.87E-5	1.84E-3 (*)	0.0446

(*) – Voltage balance of capacitors not possible;
Fail – the converter fails immediately to achieve the desired voltage when the failure happens in the specific power device

TABLE 2. Estimated probability of failure to 5 year of operation after the first failure (Proposed topology), admitting the proposed changes in the control strategy.

	Open circuit failures			Short-circuit failure modes		
Device Failure	±2V	±V	0V	±2V	±V	0V
S_{1A}	0.1607	0.0105	0.0019	3.37E-6	7.87E-5	7.77E-12
S_{2A}	0.1607	0.0855	0.0037	7.87E-5	0.0446	8.19E-5
S_{3A}	0.1607	0.0855	0.0037	7.87E-5	0.0446	8.19E-5
S_{4A}	0.1607	0.0105	0.0019	3.37E-6	7.87E-5	7.77E-12
S_{5A}	0.1607	0.0105	0.0019	3.37E-6	7.87E-5	7.77E-12
S_{6A}	0.1607	0.0855	0.0037	7.87E-5	0.0446	8.19E-5
S_{7A}	0.1607	0.0855	0.0037	7.87E-5	0.0446	8.19E-5
S_{8A}	0.1607	0.0105	0.0019	3.37E-6	7.87E-5	7.77E-12

TABLE 3. Comparison with existing fault-tolerant schemes.

Methods / Items	[16], [17]	[9]	[36]	[22],[23]	Proposed
Multilevel operation	No	No	Yes	No	Yes
Motor	Traditional SRM	Traditional SRM	Traditional SRM	Special Design	Traditional SRM
Converter modularity	Low	High	Low	High	High
Additional mechanical or static switches	Yes	No	No	No	No
Fault tolerant ability	Medium	High	Medium	High	High
Control complexity	Low	Medium	High	Medium	High

V. COMPARISON WITH EXISTING FAULT-TOLERANT DRIVES

As mentioned before, several fault-tolerant drives were already developed and presented. For the adoption of a certain drive, several factors must be considered. In this way, the proposed drive will be compared with other fault-tolerant schemes. A resume of this comparison can be seen in Table 3. It was made among the classical *SRM* drive and topologies considered more similar with the proposed one.

One of the aspects that is usually considered is the modularity in order to allow a large-scale industrial production at an expectable cost. So, regarding this aspect the proposed solution presents that modularity since it uses *NPC* legs that inclusive are most used in drives for classical induction motors. Another aspect is that the proposed drive can be used with traditional motors. Under the point of view of the fault tolerance ability the proposed topology presents high capability since it can be operated under open and short–circuits conditions. Moreover, this is achieved under multilevel operation, which very few topologies allow to. Another characteristic associated to some fault tolerant drives is the requirement of additional mechanical or static commutators. Regarding the proposed drive, there is no need to add those commutators, which simplifies the topology. One of the issues related with this proposed drive is that requires a control system with more complexity. Indeed, besides the current controller, it is also required to ensure the balance of the applied voltage to the *DC* capacitors that are in serial connection.

VI. CONTROL OF THE DRIVE AND BALANCE OF THE DC VOLTAGE CAPACITORS

There are several schemes that can be used to control the SRM. In this work it was adopted the control system presented in the diagram of fig. 13. The current controller and correspondent modulator are the base of most of the control systems used for the *SRM*.

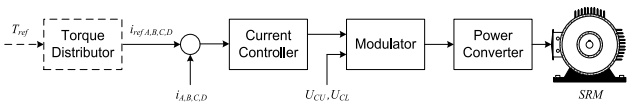

FIGURE 13. Block diagram of the *SRM* speed controller.

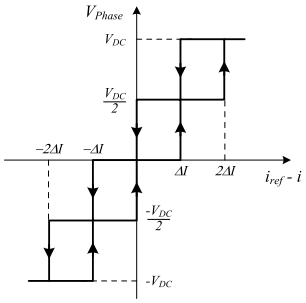

FIGURE 14. Proposed multilevel comparator for the current controller.

The current controller, which regulates the phase current, will be implemented by a current hysteresis controller. However, the conventional hysteresis controller presents a limitation regarding the number of voltage levels. Thus, to overcome this limitation, instead of a classical two-level hysteretic comparator, it is proposed the use of a multilevel hysteretic comparator. Thus, in order to generate the five possible voltage levels, it will be used a five-level comparator as presented in fig. 14. In this way, the applied voltage level will be function of the current error (eq. 10), in which the applied voltage will be increased with the increase of the

TABLE 4. Redundant combinations for the intermediate voltages.

State	S_{1A}	S_{2A}	S_{3A}	S_{4A}	S_{5A}	S_{6A}	S_{7A}	S_{8A}	Voltage Level
1	1	1	0	0	0	0	1	0	$+V_{DC}/2$
2	1	1	0	0	0	1	0	0	$+V_{DC}/2$
3	0	1	0	0	0	0	1	1	$+V_{DC}/2$
4	0	0	1	0	0	0	1	1	$+V_{DC}/2$
5	0	1	0	0	1	1	0	0	$-V_{DC}/2$
6	0	0	1	0	1	1	0	0	$-V_{DC}/2$
7	0	0	1	1	0	1	0	0	$-V_{DC}/2$
8	0	0	1	1	0	0	1	0	$-V_{DC}/2$

current error.

$$\begin{cases} if \;\; i_{ref} - i \;\; > \;\; +2\,\Delta i \;\Rightarrow\; V_{phase} \;=\; +V_{DC} \\ if \;\; i_{ref} - i \;\; > \;\; +\Delta i \;\Rightarrow\; V_{phase} \;=\; +\dfrac{V_{DC}}{2} \\ if \;\; i_{ref} - i \;\; > \;\; -\Delta i \;\Rightarrow\; V_{phase} \;=\; -\dfrac{V_{DC}}{2} \\ if \;\; i_{ref} - i \;\; < \;\; -2\,\Delta i \;\Rightarrow\; V_{phase} \;=\; -V_{DC} \end{cases} \tag{10}$$

Another aspect related with the control system is the generation of the gate signals that are function of the current error. This is done through a modulator connected to the output of the hysteretic comparator. For the voltage levels ($-V_{DC}$ and $+V_{DC}$) there is only one possible combination. However, for the inner voltage levels there are several possible switching combinations for the same voltage level. In the case of the intermediate voltage the adopted switching combination must be chosen in a detailed way. In fact, an important issue related with the *NPC* multilevel topology is the necessity to ensure the balance of the applied voltage to the *DC* capacitors that are in serial connection. There are two ways to ensure this balance, either through the right combination of the switches that control the phase under operation, either through the switches that control one of the phases that are not in operation. This second possibility is due to the phase independence of this type of motor. However, the balance will be made mainly through the switches that control the phase under operation.

Through the analysis of the topology associated to one of the phases, it is possible to see that regarding the two intermediate voltages there are 8 combinations that can be used (being half of them for positive and the other half for negative levels), as presented in Table 4. Thus, when the intermediate voltage is selected to control the current, it is fundamental to choose the state that allows to balance the voltage across the *DC* capacitors.

In order to balance the voltage across the capacitors, it will be considered a control law associated to these capacitor voltages. This law is given by (11) and consists in the difference between the measured capacitor voltages.

$$e_{V_{DC}} = V_{DC\_capacitor\_upper} - V_{DC\_capacitor\_lower} \tag{11}$$

From the analysis of the circuit and the switches states presented in Table 2, is possible to see that for the intermediate voltage $+V_{DC}/2$ and positive winding current, state 1 discharges upper capacitor and state 3 discharges the lower capacitor. Thus, in accordance with this analysis is possible to define the final strategy to balance these capacitors. The selection of the switching combination for the intermediate voltages will be then defined by the conditions presented in Table 5.

TABLE 5. Selection of the states to balance the DC voltage capacitors.

	$i > 0$	$i < 0$
$+V_{DC}/2$	1	4
$-V_{DC}/2$	8	6

a) Decrease $e_{V_{DC}}$

	$i > 0$	$i < 0$
$+V_{DC}/2$	3	2
$-V_{DC}/2$	5	7

b) Increase $e_{V_{DC}}$

Since in several operation modes is necessary to balance the voltage across the *DC* capacitors, a fault in one of the switches will limit that capability due to the reduction of the number of redundant combinations, affecting the balance. However, due to the fault-tolerant capability of the proposed topology, this can be solved through the combination of different power semiconductors used in this situation (with the inversion of the winding current). This is the case for the open-circuit failure mode in the outer controlled power semiconductor S_{1A}. Considering this switch failure, it is not possible to use the state 1 anymore (see table 4), by which the balance of the voltages across the capacitors is lost. In this situation, the voltage across the lower capacitor will decrease due to the impossibility to use that state. However, the other healthy legs will attenuate this problem, since when they are in operation it will be possible to start again to use states that allow to balance those voltages. This unbalance will be less affected for machines with higher number of windings. Another fault condition that will affect the balance of the voltage capacitors is the short-circuit failure mode in the inner controlled power semiconductor S_2. In this situation, the use of state 8 can no longer be used, affecting in this way the capability to maintain the voltage of the lower capacitor at the desired value. In fact, in this situation, as in the previous case, the voltage across the lower capacitor will decrease, recovering from the unbalance by the other healthy legs.

VII. SIMULATION TESTS

The proposed *SRM* drive was verified through a simulation system that was built in program *Matlab/Simulink*. The models of the power components of the fault tolerant converter were obtained from the component libraries of the *Simscape Power Systems*. The system consists on a four-phase 8/6 *SRM*, capacitors of 100 μF and feed by a 300V *DC* power supply. The *SRM* was controlled by a flat-top current controller with a current reference of 6 A. The characteristics of the proposed drive were verified through several tests in different conditions, namely: normal, open transistor fault, short-circuit fault and fault tolerant.

The results of a test in normal operation for a speed of 1800 rpm can be seen in Fig. 15. From this figure is

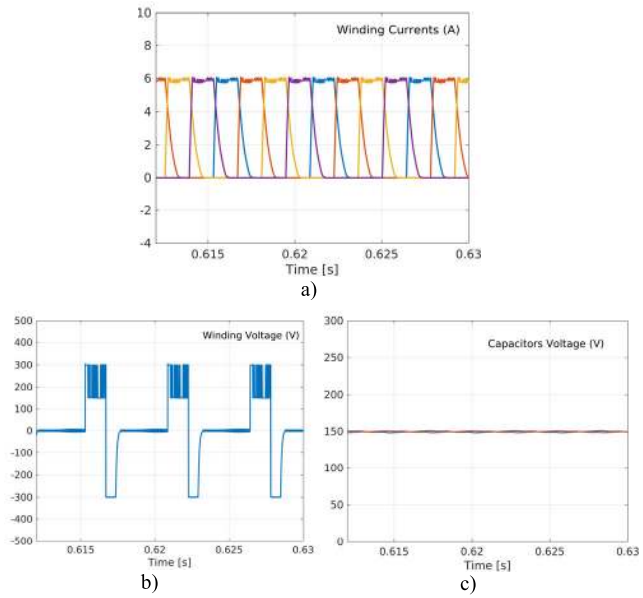

FIGURE 15. Simulation results for the *SRM* in normal operation for a speed of 1800 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

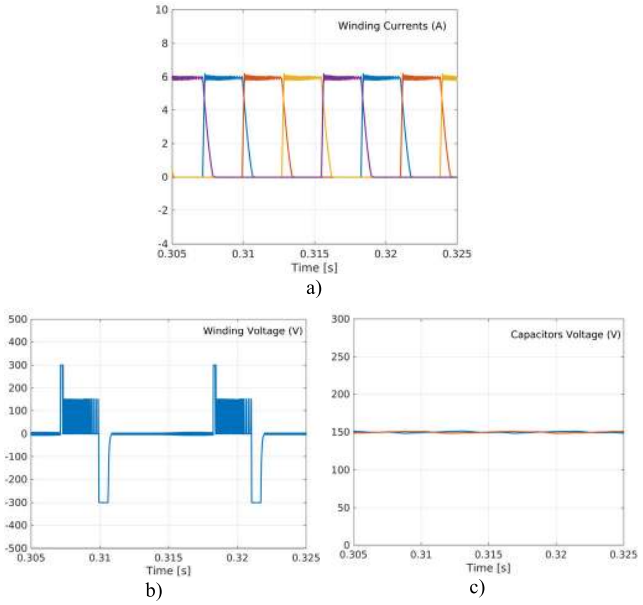

FIGURE 16. Simulation results for the *SRM* in normal operation for of speed 900 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

possible to see the waveforms of the *SRM* winding currents and correspondent voltage applied to winding A. These waveforms show that the applied voltage to the windings is near the maximum *DC* voltage bus and switching between the top levels ($+V_{DC}$ and $+V_{DC}/2$). It also shows a balance between the voltages across the capacitors. Another simulation in normal operation but for a different speed (900 rpm) was also performed. The obtained waveforms of the *SRM* winding currents and correspondent voltage applied to winding A can be seen in Fig. 16. Since the speed is reduced the voltage applied to the windings in the magnetizing and demagnetizing modes is also reduced (becoming half of the previous experimental test), switching in this case between $+V_{DC}/2$ and 0. However, to ensure a fast transition between phases when the winding is magnetized for the first time the applied voltage is the maximum. The balance between the voltages across the capacitors is also balanced.

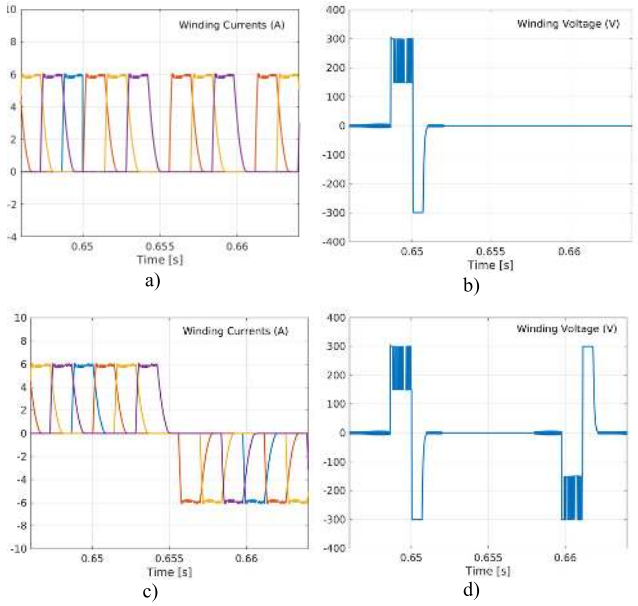

FIGURE 17. Simulation results for the *SRM* in open-circuit transistor (S_{2A}) failure and fault-tolerant condition operating at 1800 rpm: a) Winding currents in failure mode; b) Applied voltage to winding A in failure mode; c) Winding currents in fault tolerant operation; d) Applied voltage to winding A in fault tolerant operation.

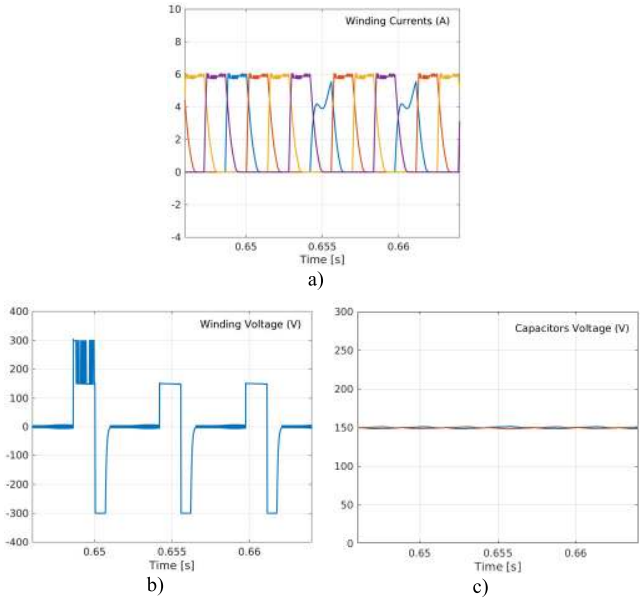

FIGURE 18. Simulation results for the *SRM* in open-circuit transistor (S_{1A}) failure operating at 1800 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

The simulation under faulty condition and fault-tolerant operation is presented in Fig. 17. The results were obtained

for a high-speed operation with an open-circuit failure in power transistor S_{2A}. In this figure the waveforms of the winding currents and applied voltage to winding A are presented. Analyzing these results, it is possible to see that under this open-circuit failure mode the current in winding A will always be zero. However, this problem is overcome when the circuit is operating in fault-tolerant mode, as shown in Figs. 17 c) and d). Another open-circuit failure mode was performed, considering a different power semiconductor, S1A. The obtained simulation waveforms of the winding currents and applied voltage to winding A are presented in Fig. 18. From these results is possible to verify that under this condition the voltage applied during the excitation mode is half of the maximum *DC* bus voltage. Due to that there will be an impact of the winding current associated to the leg under fault. Indeed, since is not possible to apply all the DC voltage to the winding, the current will not reach the reference value. Another issue related with this failure mode is that the voltage ripple of capacitors will increase (see fig. 18 c)). During the operation of the faulty leg and the magnetization process the lower capacitor will be always in discharging mode and the upper in charging mode. As in the previous situation, these limitations can be overcome by the fault-tolerant operation, more specifically through the inversion of the currents. In this fault tolerant mode, the operation of the circuit will be the same as the one presented in figs. 17 c) and d).

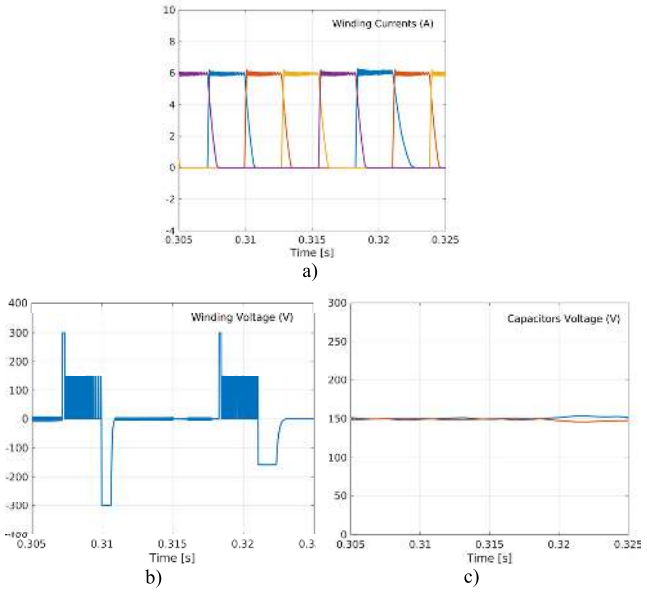

FIGURE 19. Simulation results for the *SRM* in short-circuit transistor (S_{2A}) failure operating at 900 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

Another simulation, in which a short-circuit failure in the transistor S_{2A} occurs, was also performed. From the obtained waveforms it is possible to verify that the demagnetization process in winding A, during the transition between phases, becomes more difficult (Fig. 19 a)). This is due to the limitation of the applied voltage to winding A that always presents a minimum voltage of $-V_{DC}/2$, instead of the maximum *DC* bus voltage (see fig. 19 b)). However, although some impact on the demagnetization process, it is still possible to maintain the required current. Due to the adopted control, this fault does not affect the balance of the voltage across the capacitors as can be seen in fig. 19 c).

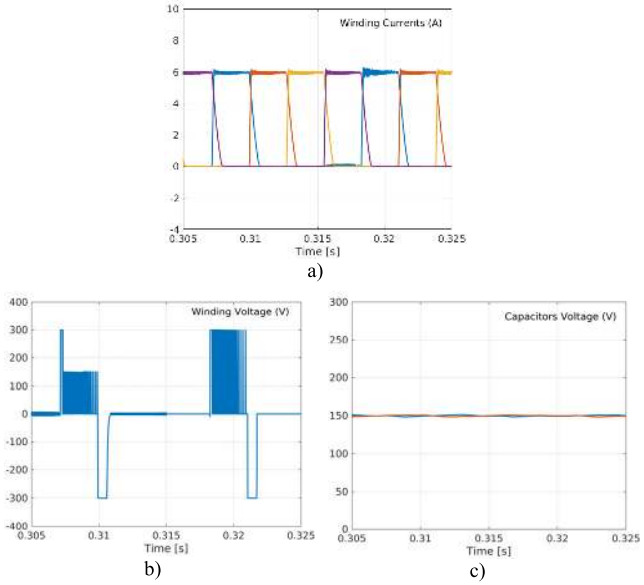

FIGURE 20. Simulation results for the *SRM* in short-circuit transistor (S_{1A}) condition operation at 900 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

The implementation of another simulation with a transistor in short-circuit fault was also made, now considering S_{1A}. In normal operation, the control of this transistor is used to shift between the total voltage V_{DC} and the middle voltage $V_{DC}/2$. Thus, considering this fault condition, it is not possible to obtain the middle voltage (see Fig. 20 b)). Nevertheless, this will not affect winding currents as shown in Fig. 20 a). However, due to the loss of the middle voltage, there will be an increase of the switching frequency. On the other hand, since the middle voltage will not be used, the voltage balance of the capacitors will not be affected (see fig. 20 c)). Anyway, the middle voltage can again be ensured if the transistor S_{8A} is used to provide $V_{DC}/2$. However, in this case there will be an impact on the voltage balance of the capacitors. A solution for all these conditions can be obtained by inverting the currents, as presented in figs. 17 c) and d).

VIII. EXPERIMENTAL VERIFICATION

The characteristics and fault-tolerant capability of the proposed *SRM* drive were also verified through several experimental tests. For these tests, it was used an experimental system consisting by a four-phase 8/6 *SRM*, the new proposed inverter, circuit drives and sensors. The drive was feed by a 100 V *DC* power supply. To control the *SRM*, it was used the flat-top current control, with a current reference of 6 A. Several experimental tests were performed in four different conditions: normal operation, open-circuit transistor fault, short-circuit transistor fault and fault tolerant. The control

algorithm of the SRM drive was performed on a DSPACE tool. In this tool, several decision tables were introduced in order to deal with all the operation modes (normal and failure modes) and capacitors balance. The failure modes can be selected in the DSPACE tool, turning on and turning off the desired power devices in order to produce a single open- or short-circuit failure. According to the specific failure mode (in which the faulty transistor is permanently turning off or on) the control strategy must change to provide the necessary fault tolerance, as described in section IV.

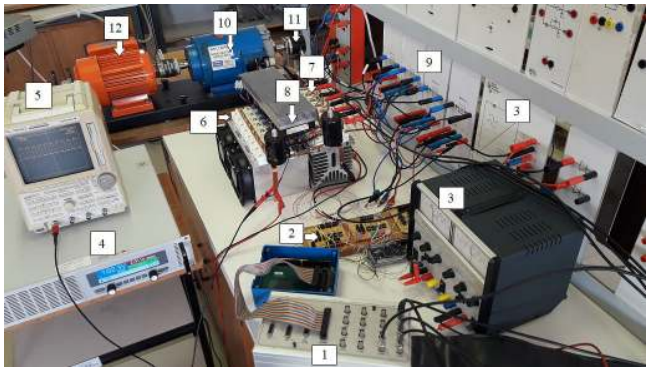

FIGURE 21. Photograph of the laboratorial prototype (1 – DSPACE connection board 2 – Gate driving circuits 3 - Power supplies to ventilation and driving circuits 4 – DC power source 5 – Oscilloscope 6 – Top IGBT power modules 7 Bottom IGBT power modules 8 – NPC diode power modules 9 – Analog current sensors to the four-phases 10 – SRM 11 – Absolute encoder 12 – DC generator used as mechanic load).

Fig. 21 shows a photograph of the laboratorial prototype that was used to obtain the experimental verification.

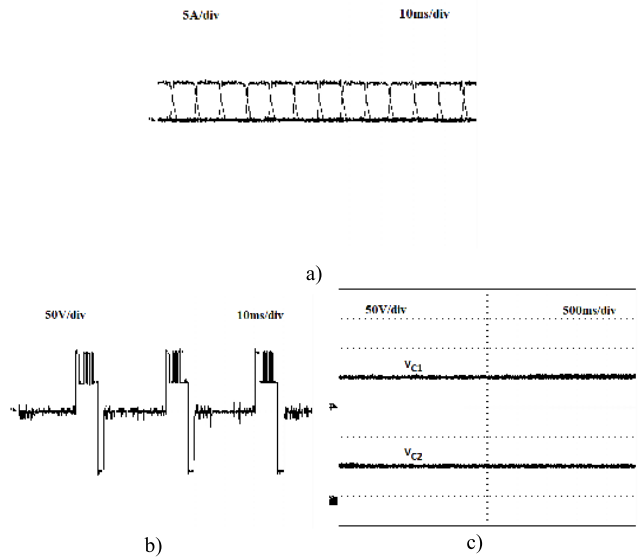

FIGURE 22. Experimental results for the *SRM* in normal operation for a speed of 1870 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

Experimental tests with different speeds have been performed to evaluate the behavior of the multilevel drive in these conditions. Fig. 22 presents several waveforms for normal operation with a speed of 1870 rpm. It is possible

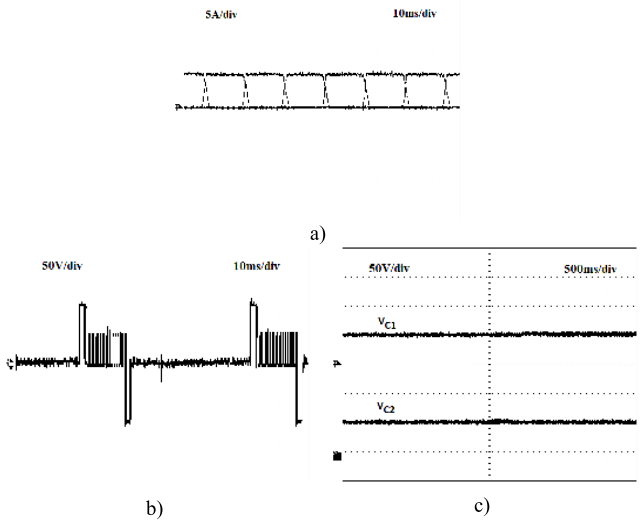

FIGURE 23. Experimental results for the *SRM* in normal operation for of speed 980 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

to see the behavior of the winding currents of the *SRM* (fig. 22 a)) and the correspondent voltage applied to winding A (fig. 22 b)). As can be seen in this experimental test, the applied voltage to the windings is near the maximum *DC* voltage bus and switching voltage between the top levels ($+V_{DC}$ and $+V_{DC}/2$). Fig. 22 c) shows the voltage across both capacitors, where the respective balance can be confirmed. Another experimental test in normal operation was also made, but in which it was applied a heavier load torque resulting in a speed of 980 rpm (see fig. 23). The obtained behavior of the winding currents and applied voltage to winding A for this condition are presented in fig. 23 a) and b) respectively. From these results is possible to see that the voltage applied to the windings in the magnetizing and demagnetizing modes is now half of the previous experimental test (test with higher speed), switching in this case between $+V_{DC}/2$ and 0. It is also possible to confirm that when the winding is magnetized for the first time the maximum applied voltage ensures a fast magnetization and demagnetization in each phase. This figure also shows that the voltage across the capacitors is also maintained stable and balanced (see fig. 23 c)).

Several experimental tests in faulty condition and fault-tolerant operation were also performed. Fig. 24 presents the results obtained for a high-speed operation with an open-circuit failure in transistor S_{2A}. It should be noted that a failure in transistor S_{7A} would originate the same behavior. In this figure it is presented the behavior of the winding currents and applied voltage to winding *A* under two operation modes, faulty mode (fig. 24 a) and b)) and fault-tolerant mode (fig. 24 c) and d)).

From these results is possible to confirm that under an open-circuit fault in S_{2A} the current in winding *A* will always be maintained at zero. In this situation the speed tends to decrease, and the torque ripple tends to increase. These results also show that in fault-tolerant operation this drawback is

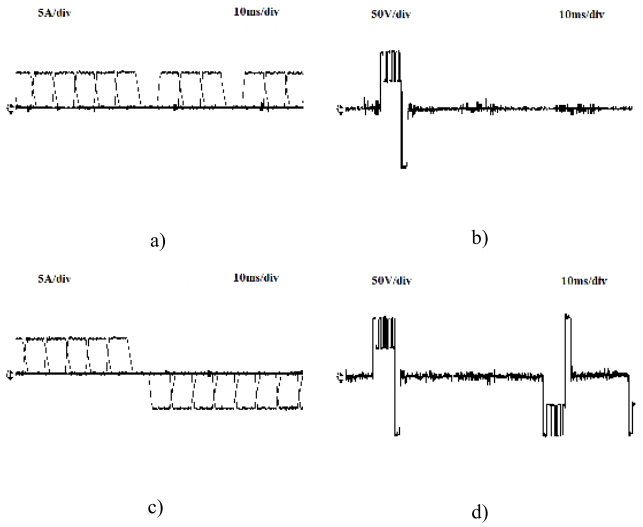

FIGURE 24. Experimental results for the *SRM* in open-circuit transistor (S_{2A}) failure and fault tolerant condition operation at 1870 rpm: a) Winding currents in failure mode; b) Applied voltage to winding A in failure mode; c) Winding currents in fault tolerant operation; d) Applied voltage to winding A in fault tolerant operation.

overcome through the inversion of the winding currents. Through the analysis of the applied voltage is also possible to verify the two different operation modes (faulty device and fault-tolerant). In fact, after the open-circuit failure, it is not possible to apply a positive voltage. In fault tolerant mode, it becomes again possible to apply a voltage to the winding but with an inverse polarity in all the windings.

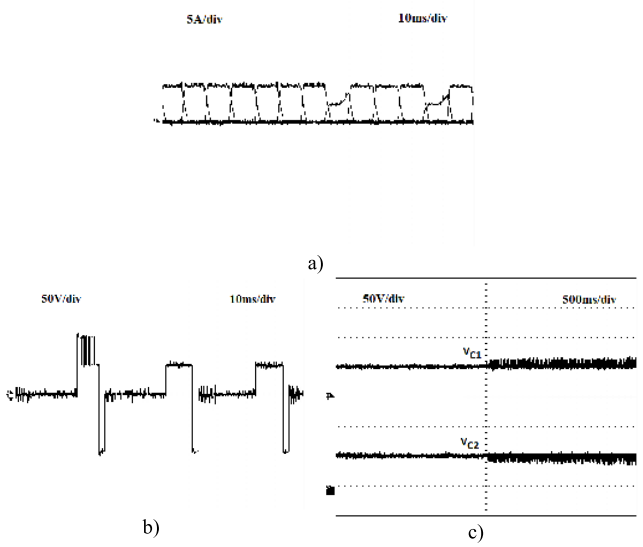

FIGURE 25. Experimental results for the *SRM* in open-circuit transistor (S_{1A}) failure operating at 1870 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

Another experimental test with an open-circuit transistor failure was also performed but in this case for the S_{1A} (the behavior is the same for the S_{8A}). This test was performed for the speed of 1870 rpm. Figs. 25 a) and b) show the behavior of the winding currents and applied voltage to winding A considering this transistor fault. Regarding the applied voltage it is possible to see that the voltage applied during the excitation mode is half of the maximum DC bus voltage. This limitation will have impact on the currents, since the amplitude of the phase current associated to the leg under fault is lower than the one that is required due to the reduced voltage applied. Another impact due to this fault is that the voltage ripple of capacitors will increase (see fig. 25 c)). Notice that during the operation of the faulty leg the lower capacitor will be always in discharging mode and the upper in charging mode. Thus, only when the operation changes to the healthy leg the balance will be achieved again. These limitations can be overcome by the fault-tolerant operation in which the magnetizing current is inverted. In this case, the operation of the circuit will be the same as the one presented in figs. 24 c) and d).

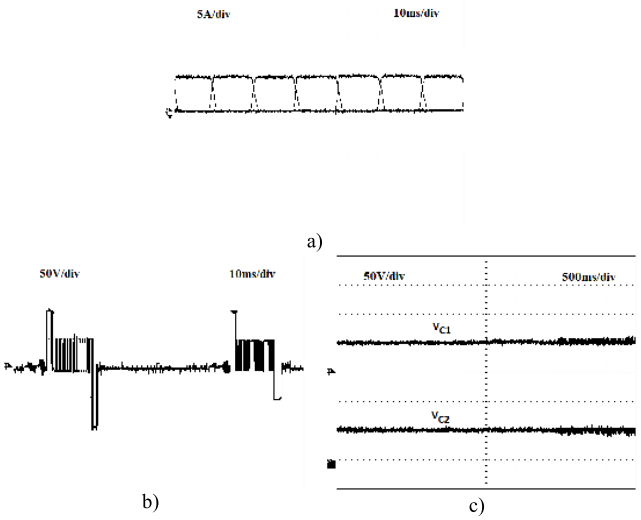

FIGURE 26. Experimental results for the *SRM* in short-circuit transistor (S_{2A}) failure operating at 980 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

Experimental tests considering short-circuit failures in power semiconductors were also performed. Fig. 26 presents the obtained results for an operation with a short circuit fault in transistor S_{2A}. From this figure is possible to see that the demagnetization process in winding A, during the transition between phases, becomes more difficult. In fact, the current through that winding presents a lower variation when compared with the others (see fig. 26 a)). This is due to the limitation of the applied voltage to winding A that always presents a minimum voltage of $-V_{DC}/2$ (see fig. 26 b)). However, from these figures, it is possible to see that, since the impact is only on the demagnetization process, it is always possible to ensure the required current. Regarding the balance of the voltage across the capacitors there is no impact as can be seen in fig. 26 c).

Another test with a power semiconductor in short circuit was also performed, in this case for S_{1A}. Fig. 27 shows the current and voltage at the terminals of the winding associated to the leg under fault. From these figures is possible to see

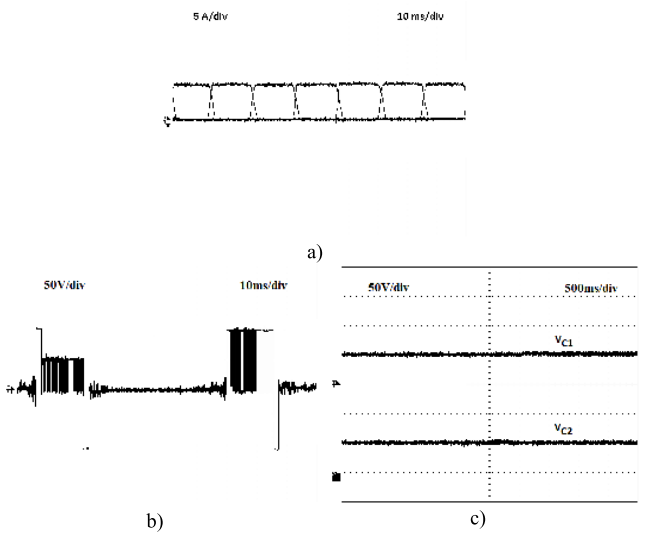

FIGURE 27. Experimental results for the *SRM* in short-circuit transistor (S_{1A}) failure operating at 980 rpm: a) Winding currents; b) Applied voltage to winding A; c) Capacitor voltages.

that after the fault the middle voltage $V_{DC}/2$ is lost (see fig. 27 b)), increasing the switching frequency of the switches of the faulty leg. Since the middle voltage will be not used, the voltage balance of the capacitors will not be affected (see fig. 27 c)). However, if the power semiconductor S_{8A} is used to provide $V_{DC}/2$ then the middle voltage can again be ensured. Nevertheless, in this case (using S_{8A}) there will be an impact on the voltage balance of the capacitors. Since the voltage balance can only be ensured by the healthy legs, during the operation of the faulty legs there will be an unbalance of those voltages, increasing the ripple. Those problems can be fully solved through current inversion, as presented in figs. 24 c) and d).

IX. CONCLUSION

In this paper, a new fault tolerant *SRM* drive with multilevel characteristics was proposed. The proposed drive is based on a *NPC* modular topology, allowing to apply five voltage levels to the *SRM* windings. An analysis of the several faults that can arise on the proposed power converter was presented. From this analysis it was possible to verify that several changes can be performed in the power converter to maintain the operation with minimum degradation or even achieve a full fault-tolerant operation mode through the inversion of the current excitation. For the control system it was used the flat-top current control. To allow the multilevel operation it was proposed a current controller with a multilevel hysteretic comparator. The problem of the balance between the capacitors voltages was also addressed, being proposed and experimentally tested an algorithm to control the drive in a way that properly ensures the capacitors balance. The effectiveness and capabilities of the proposed fault-tolerant topology were verified through several simulation and experimental tests, using a four-phase 8/6 *SRM*. From the obtained experimental results, it was possible to verify that this drive is a promising solution to be applied in industrial applications with high reliability.

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