A Multilevel Inverter System for an Induction Motor With Open-End Windings

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***Abstract*—In this paper, a multilevel inverter system for an open-end winding induction motor drive is described. Multilevel inversion is achieved by feeding an open-end winding induction motor with two two-level inverters in cascade (equivalent to a three-level inverter) from one end and a single two-level inverter from the other end of the motor. The combined inverter system with open-end winding induction motor produces voltage space-vector locations identical to a six-level inverter. A total of 512 space-vector combinations are available in the proposed scheme, distributed over 91 space-vector locations. The proposed inverter drive scheme is capable of producing a multilevel pulsewidth-modulation (PWM) waveform for the phase voltage ranging from a two-level waveform to a six-level waveform depending on the modulation range. A space-vector PWM scheme for the proposed drive is implemented using a 1.5-kW induction motor with open-end winding structure.**

***Index Terms*—Induction motor drive, multilevel inverters, open-end winding, pulsewidth-modulation (PWM) strategy.**

I. Introduction

MULTILEVEL inverters produce a stepped output phase voltage with a refined harmonic profile when compared to a two-level inverter-fed drive system [1], [2]. The circuit complexity and cost inhibit extension of the conventional three-level neutral-point-clamped (NPC) configuration to higher levels [2]–[4]. Certain modifications have been suggested to extend the conventional NPC three-level inverters for a higher number of levels [5], [6]. Flying-capacitor and series-connected H-bridge configurations [7]–[10] have also been suggested as alternative circuit topologies. However, these configurations are also complex for higher number of levels. Open-end winding induction motors, obtained by removing the neutral point of the stator windings of ordinary motors, offer another approach to multilevel inversion. It has been shown that two two-level inverters, connected at either end of an open-end winding induction motor, are capable of achieving three-level inversion [11]. In this scheme, each inverter is powered by an isolated dc-link voltage, which is half compared to the conventional drive (a single two-level inverter feeding a normal motor). Open-end winding motors require either harmonic filters or isolation transformers to prevent currents of the triplen harmonic order flowing in the motor phases and the semiconductor devices. A space-vector-modulated pulsewidth-modulation (PWM) scheme has been suggested in [12] for the power circuit topology proposed in [11]. With this PWM scheme, a total of 64 space-vector combinations are possible, distributed over 19 space-vector locations. A further improvisation is suggested in [13], in which two two-level inverters with unequal dc-link voltages (which are in the ratio $2:1$), feed an open-end winding induction motor. It has been shown that this configuration is capable of achieving four-level inversion [13]. The total number of space-vector locations produced in this scheme is enhanced to 37. A reduction in the switching ripple is achieved with this scheme, compared to the former, as the number of constituent sectors is enhanced to 54, compared to 24 with the former.

In this paper, a multilevel inverter system for an open-end winding induction motor is proposed. The proposed multilevel inverter system produces multilevel PWM waveforms ranging from a two-level inverter waveform to a six-level inverter waveform, depending on the range of modulation.

In the power circuit topology proposed in this paper, an open-end winding induction motor is fed with a three-level inverter at one end and a two-level inverter at the other. Unequal dc-link voltages are employed for individual inverters. An alternative circuit configuration is adopted to realize the three-level inverter, in which three-level inversion is obtained by connecting two two-level inverters in cascade.

The proposed inverter scheme is capable of producing 512 voltage space-vector combinations distributed over 91 voltage space-vector locations. The total number of constituent sectors in this scheme is enhanced to 150. Thus, this scheme is a further improvization of the multilevel inverter scheme suggested in [13]. Consequently, a further reduction of the switching ripple in the motor phase voltage waveform is achieved with this circuit configuration, compared to the one proposed in [13]. With the proposed scheme, the motor phase voltage waveform shows a smooth six-level inverter waveform in the range of higher modulation.

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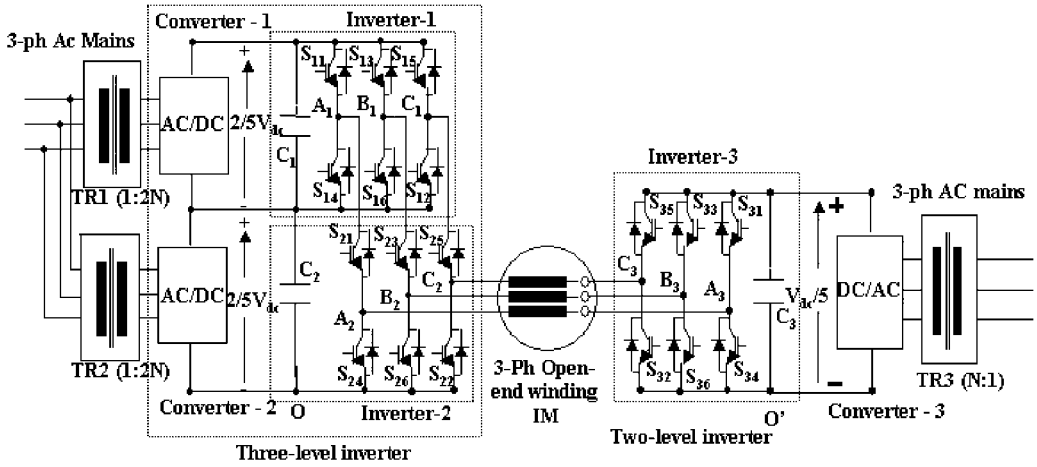


Fig. 1. Schematic circuit diagram of the proposed inverter scheme.

II. Proposed Power Circuit Configuration

The power circuit topology, proposed to realize multilevel inversion, is depicted in Fig. 1.

In this circuit configuration, an open-end winding induction motor is fed with a three-level inverter (constituted by two two-level inverters, connected in cascade) at one end, and with a two-level inverter at the other end. From Fig. 1 it may be noted that inverter-1 and inverter-2 together constitute the three-level inverter. The dc-link voltages of inverter-1, inverter-2, and inverter-3 are $(2/5)V_{\rm dc}, (2/5)V_{\rm dc}$, and $(1/5)V_{\rm dc}$ respectively, where $V_{\rm dc}$ is the dc-link voltage of an equivalent conventional system (a system in which a single two-level inverter feeds a conventional induction motor).

The pole voltage of any phase of inverter-2 (for example v_{A2O}, Fig. 1), attains a voltage of $(2/5)V_{\rm dc}$, if the following conditions are satisfied.

1) The top switch of that leg in inverter-2, in this case S_{21}, is turned on (Fig. 1).
2) The bottom switch of the corresponding leg in inverter-1, in this case S_{14}, is turned on (Fig. 1).

Similarly the pole voltage of any phase of inverter-2 (for example v_{A2O}, Fig. 1), attains a voltage of $(4/5)V_{\rm dc}$, if the following conditions are satisfied.

1) The top switch of that leg in inverter-2 (in this case S_{21}) is turned on (Fig. 1).
2) The top switch of the corresponding leg in inverter-1 (in this case S_{11}) is turned on (Fig. 1).

Thus, the dc-input points of individual phases of inverter-2 may be connected to a dc-link voltage of either $(4/5)V_{\rm dc}$ or $(2/5)V_{\rm dc}$ by turning on the top switch or the bottom switch of the corresponding phase leg in inverter-1. (Fig. 1). Additionally, the pole voltage of a given phase in inverter-2 attains a voltage of zero, if the bottom switch of the corresponding leg in inverter-2 is turned on.

Therefore, the pole voltage of a given phase for inverter-2 is capable of assuming one of the three possible values: 0, $(2/5)V_{\rm dc}$, and $(4/5)V_{\rm dc}$, which is the characteristic of a three-level inverter. This configuration of three-level inverter eliminates the neutral point fluctuations as isolated dc power supplies are employed to power the individual inverters. Hence the capacitors C_1 and C_2 carry only the ripple currents. Also, the neutral point clamping diodes are eliminated in this three-level inverter circuit. Another advantage with this three-level inverter configuration is that, the bus-bar design of the two-level inverter is considerably simpler compared to that of the conventional NPC three-level configuration. Two existing two-level inverters can be retrofitted to make the present three-level inverter configuration. However, three devices (S_{24}, S_{26}, and S_{22}, Fig. 1) are to be rated to block a voltage of $(4/5)V_{\rm dc}$.

If the points O and O′ (Fig. 1) are connected, the zero sequence components of the motor-phase currents (currents of the triplen harmonic order) exclusively flow through the link—OO′. The components of the positive and the negative sequence current flow exclusively through the motor phases connected to inverter-2 and inverter-3. However, when the points-O and O′ are not connected, there is no path for the currents of the triplen harmonic order and thus the entire triplen harmonic content in the motor phase voltage is dropped across the points O and O′. Table I illustrates the levels in the motor phase voltage, assuming that the points-O and O' are short circuited. Thus, the three phases of the motor can attain six distinct voltage levels independently, as shown in the third column of Table I. Thus, the proposed drive (Fig. 1) is capable of six-level inversion. Fig. 2 depicts the voltage space-vector combinations from the three-level inverter [Fig. 2(a)] and the two-level inverter [Fig. 2(b)], respectively.

Table II presents individual inverter states and the switches turned on to realize that state, for all the three inverters.

It may be noted that the three-level inverter has 64 space-vector combinations, as inverter-1 and inverter-2 can assume eight states each independently of the other. These 64 combinations are distributed over 19 space-vector locations as shown in Fig. 2(a). The two-level inverter has eight space vectors distributed over seven locations [Fig. 2(b)]. Therefore, the number of resultant combinations for the combined system is the product of the individual contributions of 64 and eight, respectively, from the three-level and the two-level inverters, and is equal to 512. For example, a combination "126" means that inverter-1 assumes a state of $1(+--)$; inverter-2 assumes a state of $2(++-)$ and inverter-3 assumes a state of $6(+-+)$ (Table II).

TABLE I
POLE VOLTAGES OF THE INDIVIDUAL INVERTERS AND THE MOTOR PHASE VOLTAGE

Pole-voltage of the three-level inverter (v_{A2O})	Pole-voltage of the two-level inverter ($v_{A3O'}$)	Motor phase voltage (v_{A2A3}) $v_{A2A3} = v_{A2O} - v_{A3O'}$
0	(1/5) V_{dc}	- (1/5) V_{dc}
0	0	0
(2/5) V_{dc}	(1/5) V_{dc}	(1/5) V_{dc}
(2/5) V_{dc}	0	(2/5) V_{dc}
(4/5) V_{dc}	(1/5) V_{dc}	(3/5) V_{dc}
(4/5) V_{dc}	0	(4/5) V_{dc}

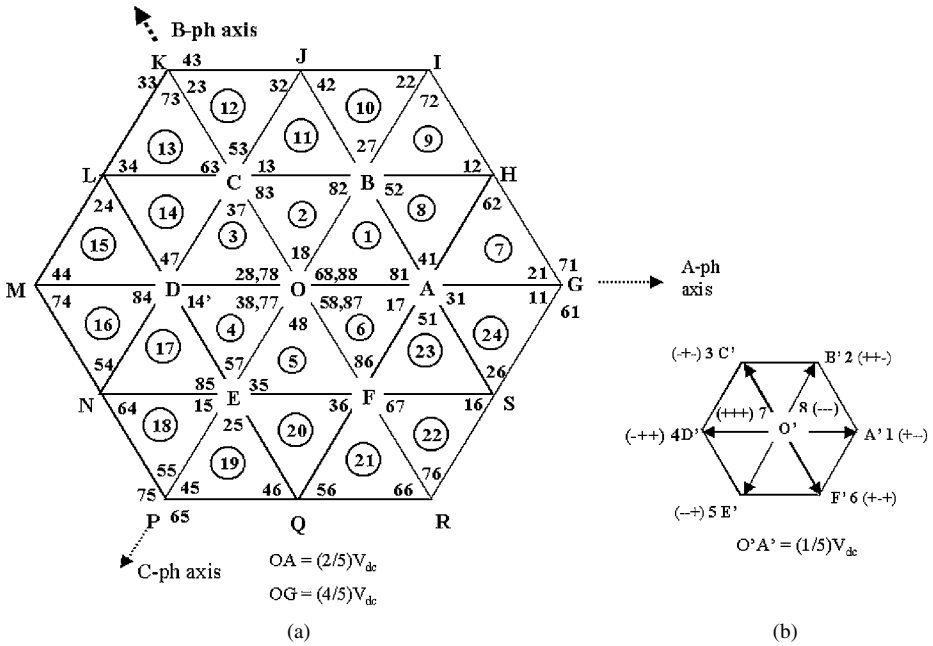


Fig. 2. Voltage space-vector locations of the three-level inverter (left) and the two-level inverter (right).

TABLE II
INVERTER STATES FOR INDIVIDUAL INVERTERS

State of Inverters	Switches turned on for inverter –1	Switches turned on for inverter –2	Switches turned on for inverter –3
1 (+ - -)	S_{16}, S_{11}, S_{12}	S_{26}, S_{21}, S_{22}	S_{36}, S_{31}, S_{32}
2 (+ + -)	S_{11}, S_{12}, S_{13}	S_{21}, S_{22}, S_{23}	S_{31}, S_{32}, S_{33}
3 (- + -)	S_{12}, S_{13}, S_{14}	S_{22}, S_{23}, S_{24}	S_{32}, S_{33}, S_{34}
4 (- + +)	S_{13}, S_{14}, S_{15}	S_{23}, S_{24}, S_{25}	S_{33}, S_{34}, S_{35}
5 (- - +)	S_{14}, S_{15}, S_{16}	S_{24}, S_{25}, S_{26}	S_{34}, S_{35}, S_{36}
6 (+ - +)	S_{15}, S_{16}, S_{11}	S_{25}, S_{26}, S_{21}	S_{35}, S_{36}, S_{31}
7 (+ + +)	S_{11}, S_{13}, S_{15}	S_{21}, S_{23}, S_{25}	S_{31}, S_{33}, S_{35}
8 (- - -)	S_{12}, S_{14}, S_{16}	S_{22}, S_{24}, S_{26}	S_{32}, S_{34}, S_{36}

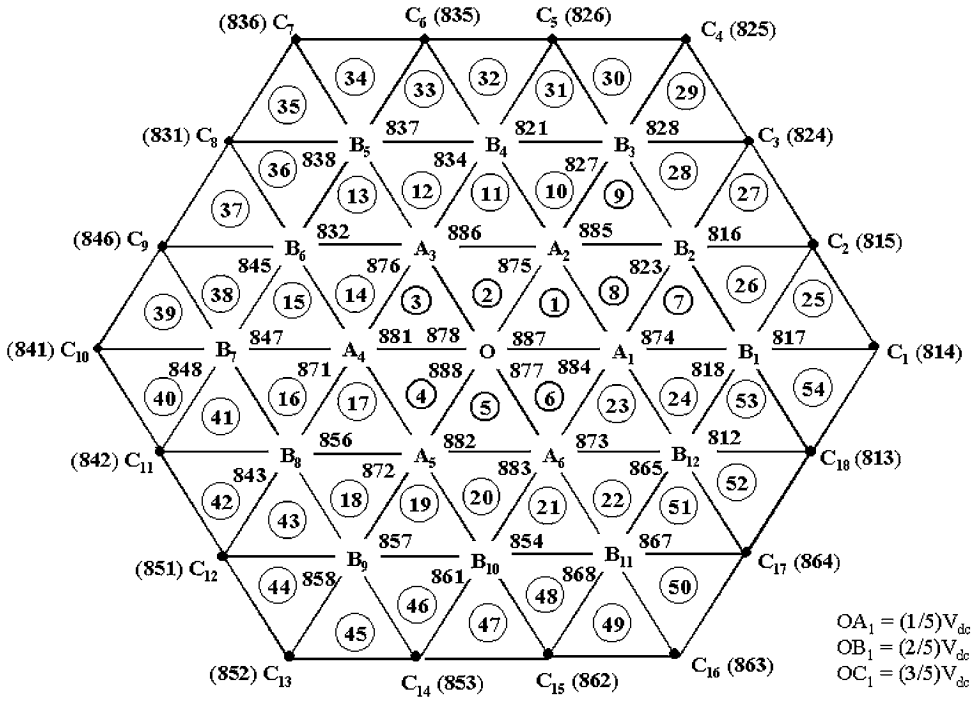


Fig. 3. Voltage space-vector locations for the proposed six-level inverter topology with inverter-1 (Fig. 1) clamped to a state of—$8(---)$.

The pole voltages of inverter-3 (the two-level inverter), e.g., $v_{A3O'}$, assume one of the two values, either 0 or $(1/5)V_{\rm dc}$, depending on whether the top switch or the bottom switch of a given phase leg is turned on.It may be expected that many locations in the resultant space-vector diagram show redundant combinations. However, in the switching strategy employed in this scheme, all these combinations have not been used, as the intent of this work is limited only to demonstrate the capability of the power circuit topology rather than devising an elegant control algorithm using these combinations.

In the present work, only certain space-vector combinations are used to demonstrate the capability of the proposed power circuit.

Certain space-vector combinations are not used to ensure that the capacitor C_3, which is placed on the side of lower voltage, is not charged by C_1 or C_2, which are placed on the sides of higher voltage (Fig. 1). Alternatively, one could use a regenerative front-end converter for the ac–dc conversion in the lower side that is capable of maintaining a stiff dc voltage across the capacitor C_3 and use all the space-vector combinations.

One of the advantages of the proposed scheme is that only inverter-3 is switched in the lowest modulation range in the V/f mode of speed control for the induction motor. Inverter-1 and inverter-2 are both clamped to a state of $8(---)$ in this case. In the middle range of modulation, inverter-2 and inverter-3 are switched, while in the higher range of modulation, all the three inverters are switched. Since inverter-1 and inverter-2 are not switched in the lowest modulation range, the switching losses are due entirely to the switching of inverter-3. Similarly in the middle range of modulation, the switching losses are due to the switching of inverter-2 and inverter-3 only.

Fig. 3 shows the voltage space-vector locations and the voltage space-vector combinations of the individual inverters in the lowest and the middle range of modulation. As mentioned earlier, in these two ranges of modulation, inverter-1 is not switched and is clamped to a state of $8(---)$. When inverter-1 is clamped to a state of $8(---)$, the dc-input points for inverter-2 are all connected to the dc-link voltage of $(2/5)V_{\rm dc}$. Hence, the pole voltage of inverter-2, v_{A2O}, can assume one of the states—0 or $(2/5)V_{\rm dc}$ as in a two-level inverter. As mentioned earlier, the pole voltage of inverter-3, $v_{A3O'}$, can assume one of the states—0 or $(1/5)V_{\rm dc}$. Thus, the ratio of the dc-link voltages connected at either end of the open-end winding induction motor is equal to 2:1 and in this range of operation, the proposed power circuit configuration behaves exactly similar to the four-level drive described in [13]. Fig. 4 illustrates the space-vector locations and the space-vector combinations in the higher modulation range, i.e., when inverter-1 is also switched along with inverter-2 and inverter-3. It may be expected that, the space-vector locations obtained by switching inverter-2 and inverter-3 exclusively form a subset to the one obtained by switching all the three inverters (The inner region shown in broken lines in Fig. 4 is identical to Fig. 3). It is evident from Figs. 3 and 4 that the switching of inverter-1 adds two more layers to the structure shown in Fig. 3. It can be observed that a total of 150 sectors are present in Fig. 4, organized into five layers. The structure constituted by the inner three layers is identical to Fig. 3.

III. Switching Strategy and PWM Pattern Generation

With the proposed circuit configuration, a total of 512 space-vector combinations are possible, which are distributed over 91 voltage space-vector locations. These space-vector locations form the vertices of 150 equilateral triangles, which are referred to as sectors (Figs. 3 and 4). These sectors are distributed into five layers (Figs. 3 and 4). Layer 1 consists of the equilateral

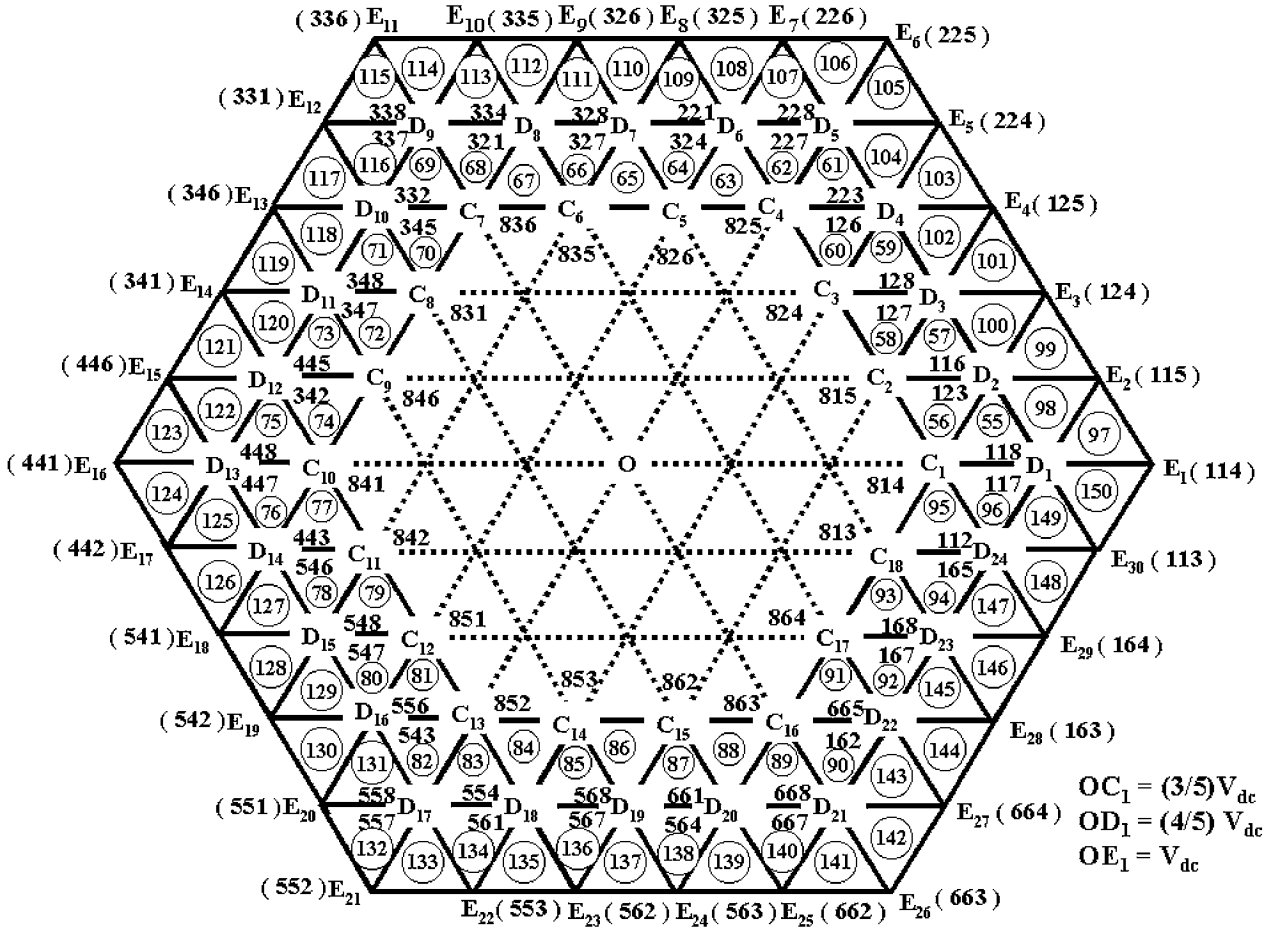


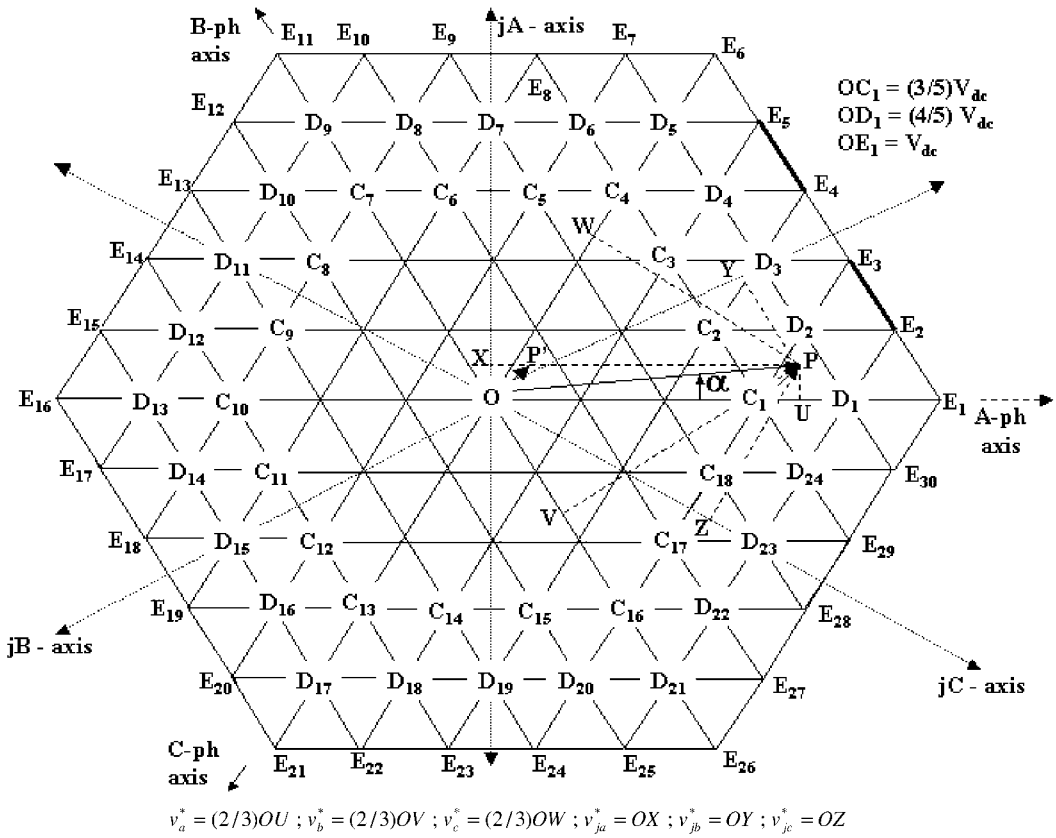
Fig. 4. Voltage space-vector locations for the proposed six-level inverter topology when inverter-1 is also switched (shaded region is identical to the one shown in Fig. 3).

triangles numbered "1"–"6" (Fig. 3). Similarly, layer 2 consists of the sectors numbered "7"–"24", and layer 3 consists of the sectors numbered "25"–"54" (Fig. 3). Similarly, layer 4 is constituted by the sectors numbered "55"–"96" and layer 5 comprises of the sectors numbered "97"–"150" (Fig. 4). The reference voltage space vector for the space-vector modulation is denoted as $\mathbf{v}_{\rm sr}$. The symbols T_0, T_1, and T_2, respectively, denote the time duration for which the vector combinations situated at the vertices of a sector (in which the tip of the reference voltage space vector is situated) are switched for the realizing of the reference voltage space vector in the average sense. The symbols v_a^*, v_b^*, and v_c^* denote the instantaneous reference phase voltages, which constitute the reference voltage space vector **OP** [Fig. 5(a)].

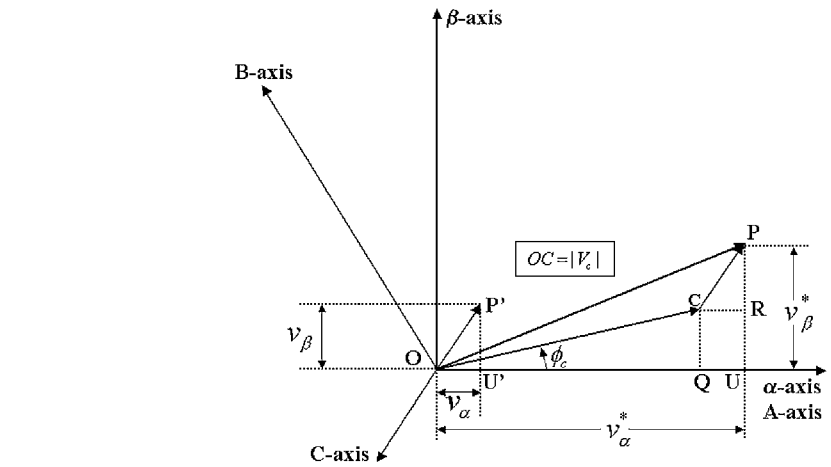
The sampling time period for space-vector modulation is denoted as T_s and is equal to the sum of the time periods T_1, T_2, and T_0. Each cycle of the load phase voltage is divided into 48 equal subintervals. Each of these subinterval durations corresponds to the sampling interval T_s. This division is maintained for the entire modulation range with V/f control.

Six adjacent sectors constitute a subhexagon. 60 such subhexagons can be identified with their centers located at A_1–D_{24} (Figs. 3 and 4). In addition, there is one inner subhexagon with its center at O (Fig. 3). Each outer sector can be mapped to the inner sector by shifting the outer subhexagonal center to the inner hexagonal center O. The method employed to determine the timing periods T_0, T_1, and T_2 to realize the reference voltage space vector $\mathbf{v}_{\rm sr}$, in the present work involves the following steps:

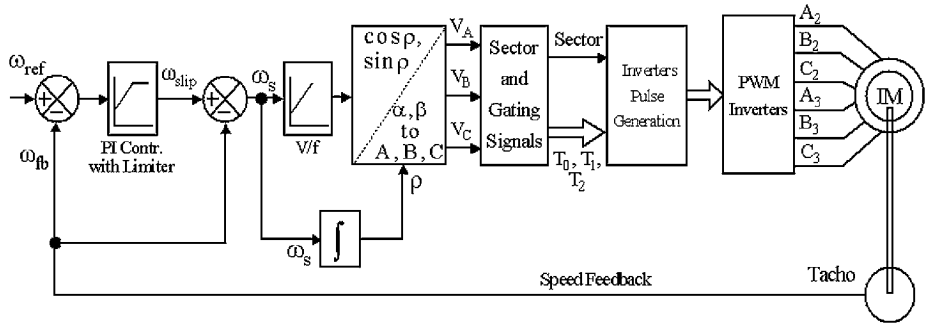
1) identification of the sector in which the tip of the reference space vector $\mathbf{v}_{\rm sr}$ [**OP**, Fig. 5(a)] is situated;
2) iIdentification of the outer subhexagon to which the sector belongs;
3) shifting the outer subhexagonal center to the inner most hexagonal center using an appropriate coordinate transformation so that the reference voltage space vector is mapped to the corresponding sector in the inner most subhexagon; thus, the reference voltage space vector **OP** gets mapped as $\mathbf{OP'}$ in the inner subhexagon [Fig. 5(a)];
4) determination of the transformed instantaneous reference phase voltages v_a, v_b, and v_c corresponding to $\mathbf{OP'}$;
5) determination of the sector vertex switching time periods T_0, T_1, and T_2 to synthesize $\mathbf{OP'}$ in the inner most hexagon using only the transformed instantaneous reference phase voltages v_a, v_b, and v_c [13], [14];
6) employing these time periods (T_0, T_1 and T_2) to switch the space-vector combinations available at the vertices forming the sector in which the tip of the actual reference space vector **OP** is situated, using appropriate lookup tables [13].



(a)

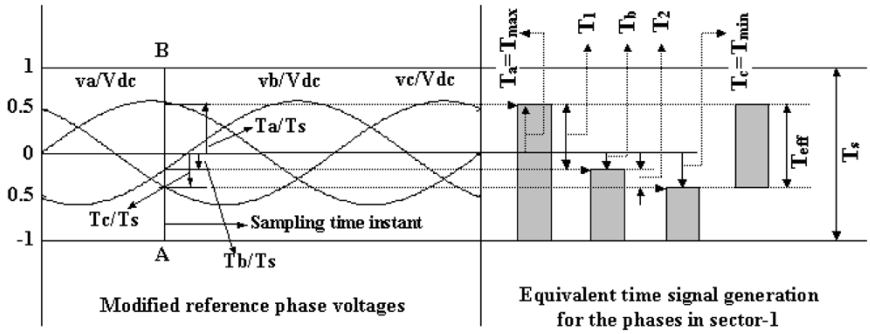


(b)

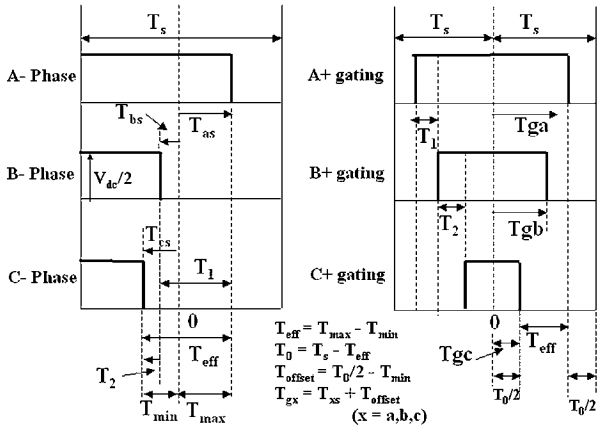


(c)

Fig. 5. (a) Sector identification by resolving $\mathbf{v}_{sr}$ along the jA, jB, and jC axes. (b) Reference voltage vector and the nearest subhexagonal center. (c) Block schematic of the controller.



(d)



(e)

Fig. 5. *(Continued.)* (d) Sampling of reference phase voltages in sector-1 and the generation of equivalent time signals. (e) Generation of gating signals in sector-1.

Thus, this procedure is conceptually equivalent to realize the mapped reference space vector in the inner hexagon and applying a vectored offset to realize the actual reference space vector in the outer sector. It may be noted that this procedure ensures that the reference space vector **OP** is realized by switching amongst the three vertices, which are situated in the closest proximity to its tip. Consequently, the switching ripple in the output voltage waveform is minimized.

A. Sector Identification

The sector identification is based on level comparators along the ja, jb, jc axes, which are perpendicular to the a, b, c axes, respectively. The symbols v^*_{ja}, v^*_{jb}, and v^*_{jc}, denote the projections of $\mathbf{v}_{\rm sr}$ onto the ja, jb and the jc axes, respectively [12].

It may be verified that the tip of $\mathbf{v_{sr}}$, the reference voltage space vector, is situated in sector 1 if

$$\begin{aligned} v^*_{ja} &< (\sqrt{3}/10)V_{\rm dc} \\ v^*_{jb} &\geq -(\sqrt{3}/10)V_{\rm dc} \\ v^*_{jc} &< (\sqrt{3}/10)V_{\rm dc}. \end{aligned} \tag{1}$$

An inspection for the affirmation of the above condition facilitates to assert if the tip of $\mathbf{v}_{\rm sr}$ is situated in sector 1. A similar procedure can be adopted for the identification of all other sectors.

B. Mapping the Outer Sectors Into the Inner Hexagon

The symbols v^*_α and v^*_β denote the components of **OP** in the "α" and the "β" directions. The α axis is placed along the A-phase axis. The β axis is in quadrature to the α axis. The instantaneous reference phase voltages v^*_a, v^*_b, and v^*_c, which constitute the reference voltage space vector **OP** [Fig. 5(a)], are obtained by projecting **OP** onto the respective phase axes and multiplying the lengths of these projections by a factor of (2/3).

The factor (2/3) arises out of the conventional abc–$\alpha\beta$ transformation, namely,

$$\begin{bmatrix} v^*_a \\ v^*_b \\ v^*_c \end{bmatrix} = \begin{bmatrix} 2/3 & 0 \\ -1/3 & 1/\sqrt{3} \\ -1/3 & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} v^*_\alpha \\ v^*_\beta \end{bmatrix}. \tag{2}$$

The instantaneous reference voltages v_a, v_b, and v_c constitute the transformed reference voltage vector $\mathbf{OP'}$ [Fig. 5(a)]. Similarly the symbols v_α and v_β denote the components of the transformed vector $\mathbf{OP'}$ in the directions of the "α" and the "β" axes.

The generalized coordinate transformation between the actual phase references (v^*_a, v^*_b, and v^*_c) and the transformed references (v_a, v_b, and v_c) is derived in the following section.

C. Generalized Coordinate Transformation to Shift the Subhexagonal Centers to the Center of the Inner Hexagon

Fig. 5(b) shows the reference voltage vector **OP.** The position vector of the nearest subhexagonal center, denoted by **OC**, is also shown in this figure. When the subhexagonal center C is shifted to the point O, the vector **CP** (**OP-OC**) is mapped into the inner subhexagon as the vector $\mathbf{OP'}$ [Fig. 5(a)].

The position vector of the subhexagonal center OC is expressed in polar form as follows:

$$\text{OC} = |V_c| \angle \phi_c. \tag{3}$$

From Fig. 5(b), the following equations may be written:

$$\mathbf{OU} = \mathbf{OQ} + \mathbf{QU} \tag{4}$$

$$v_\alpha^* = v_\alpha + |V_c| \cos \phi_c. \tag{5}$$

Similarly,

$$\mathbf{PU} = \mathbf{PR} + \mathbf{RU} = \mathbf{PR} + \mathbf{P'U'} \tag{6}$$

$$v_\beta^* = v_\beta + |V_c| \sin \phi_c. \tag{7}$$

From the classical ABC–$\alpha\beta$ transformation

$$v_\alpha^* = \frac{3}{2} v_a^*; \quad v_\beta^* = \frac{\sqrt{3}}{2}(v_b^* - v_c^*) \tag{8a}$$

and

$$v_\alpha = \frac{3}{2} v_a; \quad v_\beta = \frac{\sqrt{3}}{2}(v_b - v_c). \tag{8b}$$

Substituting (8a) and (8b) in (5) and (7)

$$\frac{3}{2} v_a + |V_c| \cos \phi_c = \frac{3}{2} v_a^* \tag{9}$$

i.e.,

$$v_a = v_a^* - \frac{2}{3} |V_c| \cos \phi_c. \tag{10}$$

Equation (10) may also be written as

$$v_a = v_a^* + \frac{2}{3} |V_c| \cos(\pi - \phi_c). \tag{11}$$

Substituting (8a) and (8b) in (7)

$$\frac{\sqrt{3}}{2}(v_b^* - v_c^*) = \frac{\sqrt{3}}{2}(v_b - v_c) + |V_c| \sin \phi_c \tag{12}$$

$$\therefore (v_b - v_c) = (v_b^* - v_c^*) - \frac{2}{\sqrt{3}} |V_c| \sin \phi_c. \tag{13}$$

Since

$$v_a + v_b + v_c = 0, \quad \text{it follows that } v_a = -v_b - v_c. \tag{14}$$

Substituting (11) in (14)

$$-v_b - v_c = v_a^* + \frac{2}{3} |V_c| \cos(\pi - \phi_c). \tag{15}$$

Adding (13) and (15)

$$-2v_c = v_b^* - v_c^* - \frac{2}{\sqrt{3}} |V_c| \sin \phi_c + v_a^* + \frac{2}{3} |V_c| \cos(\pi - \phi_c). \tag{16}$$

Noting that $v_a^* + v_b^* = -v_c^*$,

$$-2v_c = -2v_c^* - \frac{2}{\sqrt{3}} |V_c| \sin \phi_c + \frac{2}{3} |V_c| \cos(\pi - \phi_c) \tag{17}$$

i.e.,

$$v_c = v_c^* + \frac{2|V_c|}{3} \left(\frac{\sqrt{3}}{2} \sin \phi_c + \frac{1}{2} \cos \phi_c \right) \tag{18}$$

or

$$v_c = v_c^* + \frac{2|V_c|}{3} \cos(\pi/3 - \phi_c). \tag{19}$$

Adding (11) and (19)

$$(v_a + v_c) = (v_a^* + v_c^*) + \frac{2|V_c|}{3} [\cos(\pi - \phi_c) + \cos(\pi/3 - \phi_c)]. \tag{20}$$

Noting that $v_a + v_c = -v_b, v_a^* + v_c^* = -v_b^*$ and simplifying

$$v_b = v_b^* + \frac{2|V_c|}{3} \cos(5\pi/3 - \phi_c). \tag{21}$$

Equations (11), (21), and (19) give the generalized transformation between the actual instantaneous phase references v_a^*, v_b^*, v_c^* and the transformed references v_a, v_b, v_c. These three equations may be expressed in the matrix form as

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} + \frac{2|V_c|}{3} \begin{bmatrix} \cos(\pi - \phi_c) \\ \cos(5\pi/3 - \phi_c) \\ \cos(\pi/3 - \phi_c) \end{bmatrix}. \tag{22}$$

For the sake of clarity, the procedure for coordinate transformation is demonstrated for the subhexagonal center D_2. In the triangle OD_1D_2, it is known that

$$\text{OD}_1 = \frac{4}{5} V_{\text{dc}}, \text{D}_1\text{D}_2 = \frac{1}{5} V_{\text{dc}}, \quad \text{and} \quad \angle OD_1D_2 = 60^0 \tag{23}$$

By using the cosine rule

$$OD_2^2 = OD_1^2 + D_1D_2^2 - 2(OD_1)(OD_2) \cos \angle OD_1D_2. \tag{24}$$

Substituting the quantities in (23) in (24)

$$OD_2 = |V_c| = \frac{\sqrt{13}}{5} V_{\text{dc}}. \tag{25}$$

Using the sine rule

$$\frac{\frac{\sqrt{13}}{5} V_{\text{dc}}}{\sin 60^0} = \frac{\frac{V_{\text{dc}}}{5}}{\sin \phi_c} \Rightarrow \phi_c = 13.89^0. \tag{26}$$

Substituting the values of $|V_c|$ and ϕ_c for the subhexagonal center D_2 in (22) one gets

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} + \begin{bmatrix} -0.466 \\ 0.133 \\ 0.333 \end{bmatrix} V_{\rm dc} \qquad (27)$$

which is the required subhexagonal transformation for the subhexagonal center D_2.

For the PWM modulator [Fig. 5(c)], the reference space phasor is represented by the equivalent three-phase reference phase amplitudes, generated by the speed controller [Fig. 5(c)]. Once the sector and the subhexagonal center is identified, as for the subhexagonal center D_2, the identified sector can be mapped to any of the innermost six sectors. The new modified reference phase voltages, forming the subhexagon with D_2 as the center, is given by (27). Now, the switching period computaion, for the outer sector vertices, will reduce to that of finding the timings (from the mapped inner sectors), for a conventional two-level inverter [12], [14]. The outer sector switching periods (T_0, T_1, T_2) for the vertices can be derived from the modified reference phase voltages ((27) for the sectors with subhexagonal center D_2).The modified reference phase voltage is converted to an equivalent time signal (T_a, T_b, T_c) [Fig. 5(d)], and from this, the inverter gating signals are generated by giving an appropriate time offset signal, for centering the switching periods of the middle inverter vectors, in a sampling interval [12], [14]. The relation between the inverter gating signals for the A, B, and C phases (T_{ga}, T_{gb}, T_{gc}) for the conventional two-level inverter and the the triangular vertices switching duration (T_0, T_1, T_2), for a space-vector PWM, in sector-1, is shown in Fig. 5(d) and (e). The required timing signals are derived from the modified reference phase voltages, as shown in Fig. 5(d) [14]. The relation between the inverter gating signals (T_{ga}, T_{gb}, T_{gc}) and the switching periods (T_0, T_1, T_2) for inverter vectors, forming the triangular sectors, for the conventional two-level inverter (for all the six sectors) is presented in Table III. For example, when the subhexagonal center D_2 is mapped to the inner most point "O" [Fig. 5(a)], the sector 99 (Fig. 4) will be mapped to the innermost sector 1. Now, the timings T_0, T_1, T_2 are determined for the sector 1 and the inverters vector combinations 123 (Fig. 4) are switched for the period T_0, 124 for the period T_2, and 115 for T_1, for the switchings in sector 99. For various sectors a lookup table can be formed for the T_0, T_1, T_2 periods and the inverter vector combinations, forming the sectors. Once the switching combinations for the ineverters are idenfied, the appropriate switches to be turned on for individual inverters can be obtained from Table II.

TABLE III
RELATION BETWEEN INVERTER GATE SIGNALS AND THE SECTOR VERTICES SWITCHING PERIODS

Sector	T_0	T_1	T_2
1	$2T_{gc}$	T_{ga}- T_{gb}	T_{gb}- T_{gc}
2	$2T_{gc}$	T_{ga}- T_{gc}	T_{gb}- T_{ga}
3	$2T_{ga}$	T_{gb}- T_{gc}	T_{gc}- T_{ga}
4	$2T_{ga}$	T_{gb}- T_{ga}	T_{gc}- T_{gb}
5	$2T_{gb}$	T_{gc}- T_{ga}	T_{ga}- T_{gb}
6	$2T_{gb}$	T_{gc}- T_{gb}	T_{ga}- T_{gc}

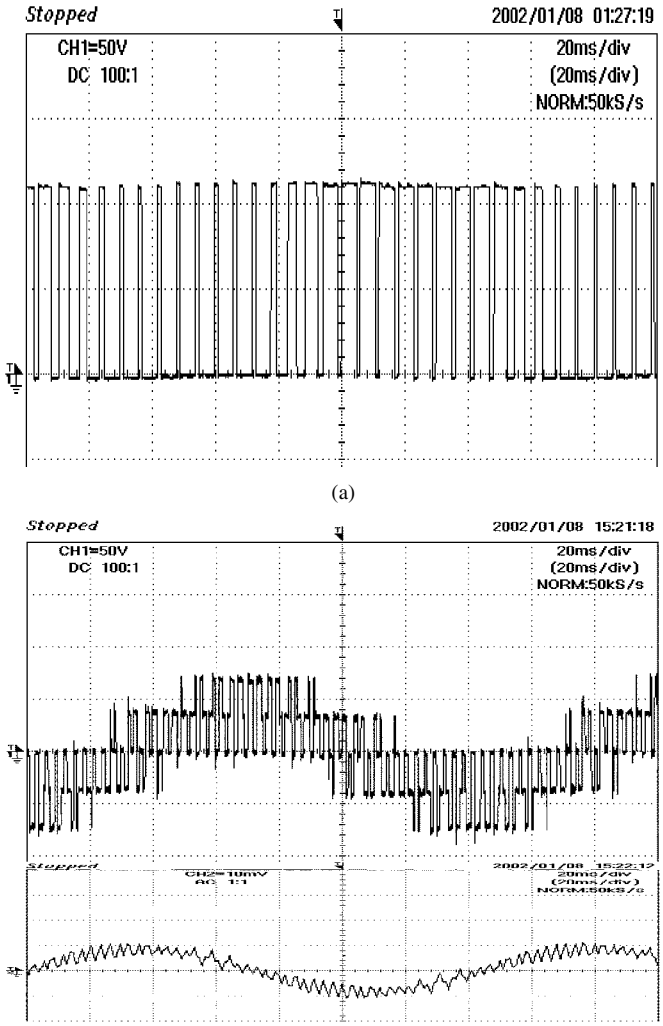


Fig. 6. (a) Pole voltage $v_{AO'}$ when $|\mathbf{v}_{\rm sr}| = 0.12\ V_{\rm dc}$ (experimental result). Scale: X axis: 20 ms/div. Y axis: 50 V/div. (b) Motor phase voltage v_{A2A3} (top) and motor phase current (bottom) when $|\mathbf{v}_{\rm sr}| = 0.12\ V_{\rm dc}$ (experimental result). Scale: X axis: 20 ms/div. Y axis: 50 V/div (top), 1 A/div (bottom).

D. Overmodulation

When the reference vector is located outside the hexagon "$E_1E_6E_{11}E_{16}E_{21}E_{26}$" [Fig. 5(a)], a modified reference voltage vector on the periphery of the hexagon having the same angle as the original reference vector is chosen. The modified active vector switching times T_1' and T_2' during overmodulation with the modified reference voltage vector may be calculated simply by the following conditions:

$$T_1' + T_2' = T_s \quad \text{and } T_1' : T_2' :: T_1 : T_2. \qquad (28)$$

Therefore,

$$T_1' = \left(\frac{T_1}{T_1 + T_2}\right) \cdot T_s, \quad T_2' = \left(\frac{T_2}{T_1 + T_2}\right) \cdot T_s. \qquad (29)$$

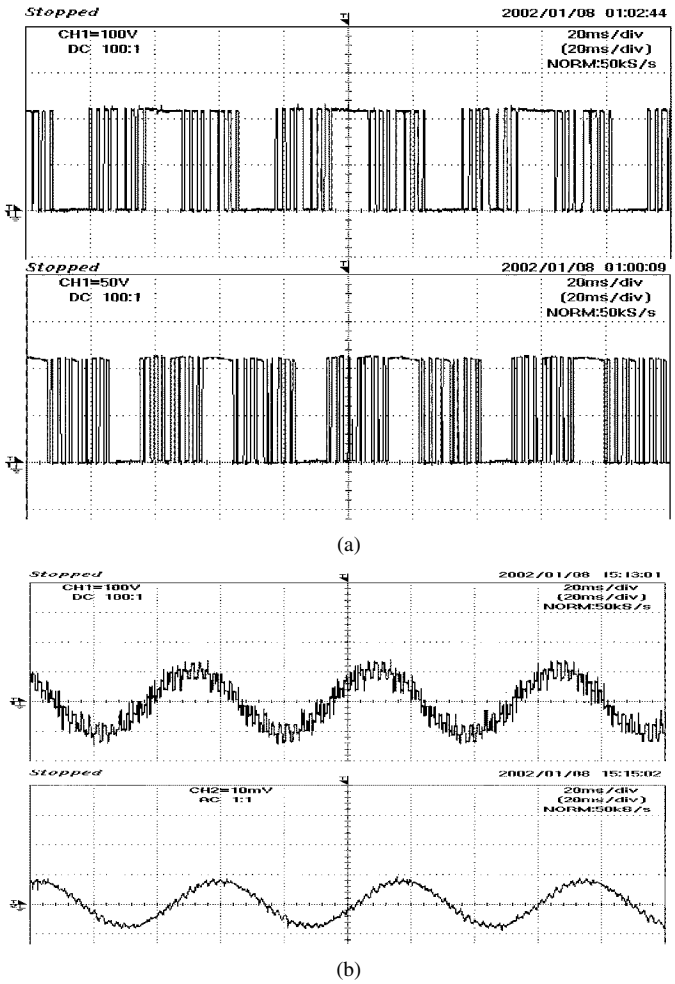


Fig. 7. (a) Pole voltages v_{A2O} (top) and $v_{A3O'}$ (bottom) when $|\mathbf{v}_{\rm sr}| = 0.3\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 20 ms/div. Y axis: 100 V/div (top), 50 V/div (bottom). (b) Motor phase voltage v_{A2A3} (top) and motor phase current (bottom) when $|\mathbf{v}_{\rm sr}| = 0.3\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 20 ms/div. Y axis: 100 V/div (top), 1A/div (bottom).

IV. Experimental Results and Discussion

The proposed scheme is implemented for a 1.5-kW three-phase open-end winding induction motor drive in open loop with V/f control, using a TMS 320F240 digital signal processor (DSP). The respective dc-bus voltages are approximately 200, 200, and 100 V for inverter-1, inverter-2, and inverter-3. This means that the dc-bus voltage of an equivalent conventional two-level inverter drive is approximately 500 V. Lookup tables are employed for the generation of PWM signals in each layer.

The experimental results for $|\mathbf{v}_{\rm sr}| = 0.12\ \mathrm{V_{dc}}$ are presented in Fig. 6(a) and (b). In this case, the tip of the reference voltage space vector $\mathbf{v}_{\rm sr}$ is confined to the inner sectors, i.e., sectors "1"–"6" (Fig. 3). As mentioned earlier, only inverter-3 is switched in this case. Fig. 6(a) presents the pole voltage waveform $v_{A3O'}$. The top trace of Fig. 6(b) depicts the actual motor phase voltage v_{A2A3} (Fig. 1) and the bottom trace of Fig. 6(b) illustrates the motor phase current at no load. The motor phase voltage shows the familiar two-level waveform as the switching is confined to the inner hexagon.

Similar experimental results are presented for $|\mathbf{v}_{\rm sr}| = 0.3\ \mathrm{V_{dc}}$. In this case, the tip of the reference voltage vector

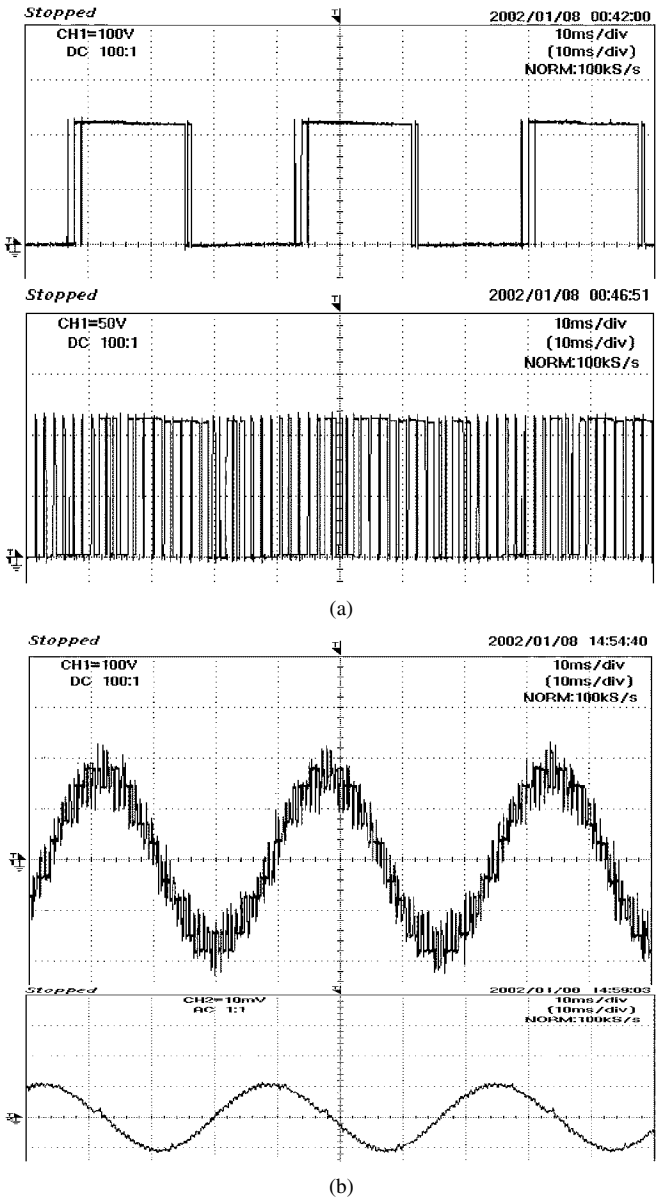
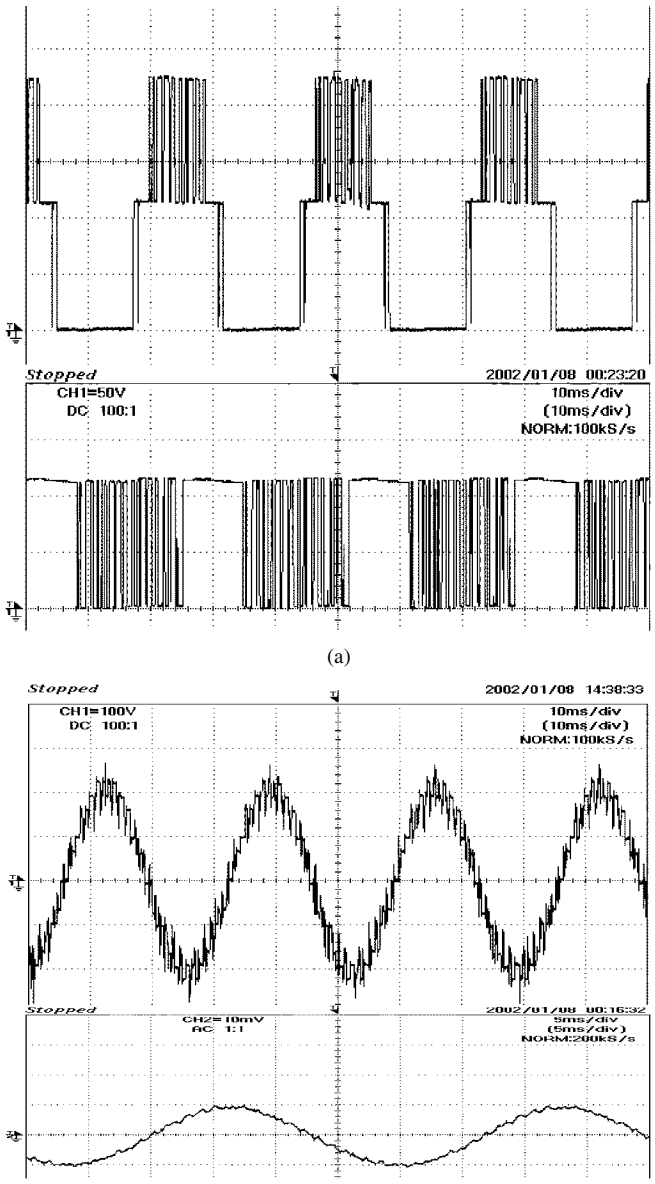


Fig. 8. (a) Pole voltages v_{A2O} (top) and $v_{A3O'}$ (bottom) when $|\mathbf{v}_{\rm sr}| = 0.48\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 10 ms/div. Y axis: 100 V/div (top), 50 V/div (bottom). (b) Motor phase voltage v_{A2A3} (top) and motor phase current (bottom) when $|\mathbf{v}_{\rm sr}| = 0.48\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 10 ms/div. Y axis: 100 volts/div (top), 1 A/div (bottom).

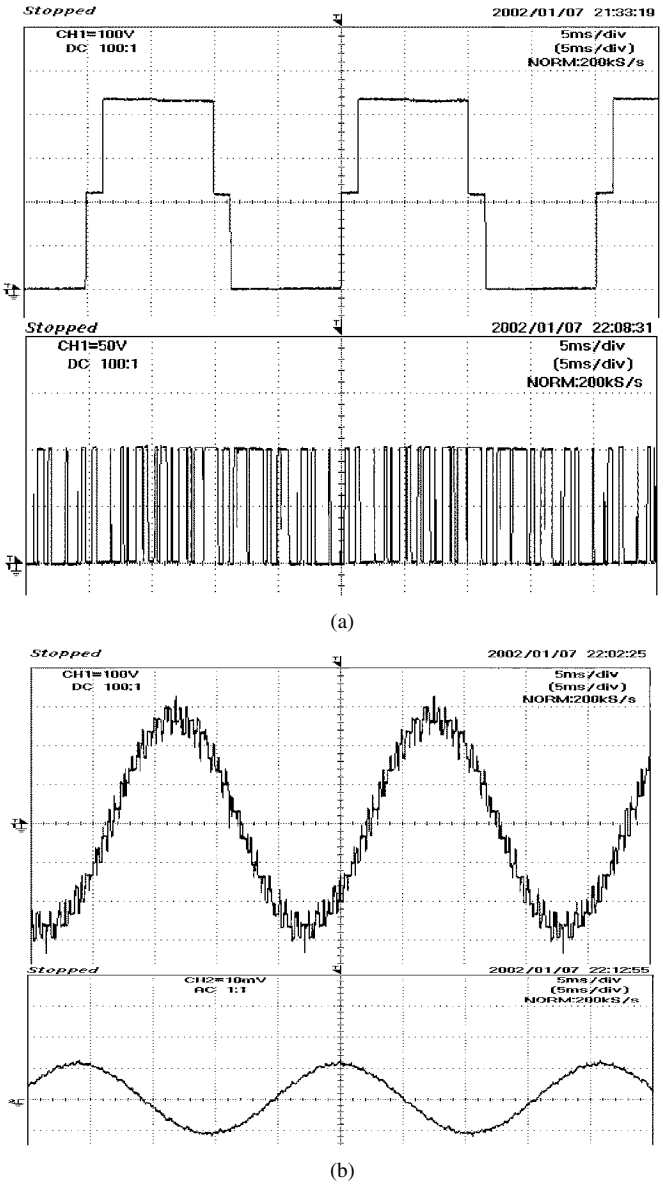
is confined to the layer-2, which consists of sectors numbered "7"–"24". In this operating region, inverter-2 and inverter-3 are switched while inverter-1 is clamped to a state of $8(---)$. Fig. 7(a) shows the pole voltage waveforms v_{A2O} and $v_{A3O'}$ (top and bottom traces respectively). Thus, the three-level inverter constituted by inverter-1 and inverter-2 effectively works as a two-level inverter as mentioned in Section II. Fig. 7(b) shows the waveforms of the motor phase voltage (top trace) and the motor phase current at no load (bottom trace). In this case, the motor phase voltage v_{A2A3} shows a three-level waveform. Similar conclusions can be drawn from the experimental results shown in Fig. 8 corresponding to the case $|\mathbf{v}_{\rm sr}| = 0.48\ \mathrm{V_{dc}}$. In this operating condition, the tip of $\mathbf{v}_{\rm sr}$ is situated exclusively in the sectors of layer 3 (sectors numbered "25"–"54"). In this region, also, inverter-1 is clamped to a state of $8(---)$. In



(a)

(b)

Fig. 9. (a) Pole voltages v_{A2O} (top) and $v_{A3O'}$ (bottom) when $|\mathbf{v}_{\rm sr}| = 0.65\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 10 ms/div. Y axis: 100 V/div (top), 50 V/div (bottom). (b) Motor phase voltage (top) v_{A2A3} and motor phase current (bottom) when $|\mathbf{v}_{\rm sr}| = 0.65\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 10 ms/div. Y axis: 100 V/div (top), 1A/div (bottom).



(a)

(b)

Fig. 10. (a) Pole voltages v_{A2O} (top) and $v_{A3O'}$ (bottom) when $|\mathbf{v}_{\rm sr}| = 0.83\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 5 ms/div. Y axis: 100 V/div (top), 50 V/div (bottom). (b) Motor phase voltage v_{A2A3} (top) and the motor phase current (bottom) when $|\mathbf{v}_{\rm sr}| = 0.83\ \mathrm{V_{dc}}$ (experimental result). Scale: X axis: 5 ms/div. Y axis: 100 V/div (top), 1 A/div (bottom).

this case, the motor phase voltage shows a four-level waveform. Fig. 9(a) and (b) illustrates the experimental results obtained when the tip of $\mathbf{v}_{\rm sr}$ is forced to be within the layer 4 (sectors "55–"96") and corresponds to the case of $|\mathbf{v}_{\rm sr}| = 0.65\ \mathrm{V_{dc}}$. Unlike the three previous cases, all three inverters are switched in this modulation range. Therefore, the pole voltage v_{A2O} shows all three levels as mentioned in Section II. Hence, the pole voltage waveform of the three-level inverter (constituted by inverter-1 and inverter-2) v_{A2O} [top trace, Fig. 9(a)] shows all the three possible levels, namely, -0, $(2/5)\ \mathrm{V_{dc}}$, and $(4/5)\ \mathrm{V_{dc}}$. The motor phase voltage v_{A2A3} is further refined, showing a five-level waveform, as the space-vector PWM scheme uses the 24 vertices "$\mathrm{D_1}$"–"$\mathrm{D_{24}}$" along with the vertices "$\mathrm{C_1}$"–"$\mathrm{C_{18}}$". Fig. 10 illustrates the experimental results obtained when the tip of $\mathbf{v}_{\rm sr}$ is restricted to be within layer 5 (sectors "97"–"150") and corresponds to the case of $|\mathbf{v}_{\rm sr}| = 0.83\ \mathrm{V_{dc}}$. The motor phase voltage v_{A2A3} is the most refined, now showing a six-level waveform, as the space-vector PWM scheme uses the 30 vertices "$\mathrm{E_1}$"–"$\mathrm{E_{30}}$" along with the vertices "$\mathrm{D_1}$"–"$\mathrm{D_{24}}$". Further experimental results are presented for the case of overmodulation and the 30-step operation. When the inverter system is overmodulated, the tip of $\mathbf{v}_{\rm sr}$ is forced to trace the outermost hexagon. The motor phase voltage shows a six-level waveform in this case also [top trace, Fig. 11(b)].

Fig. 12(a) presents the pole voltage waveforms and Fig. 12(b) presents the waveforms of the motor phase voltage v_{A2A3} (top trace) and the motor phase current (bottom trace) for the 30-step operation under no-load operation. The motor phase voltage clearly shows 30 steps in this case while the motor phase cur-

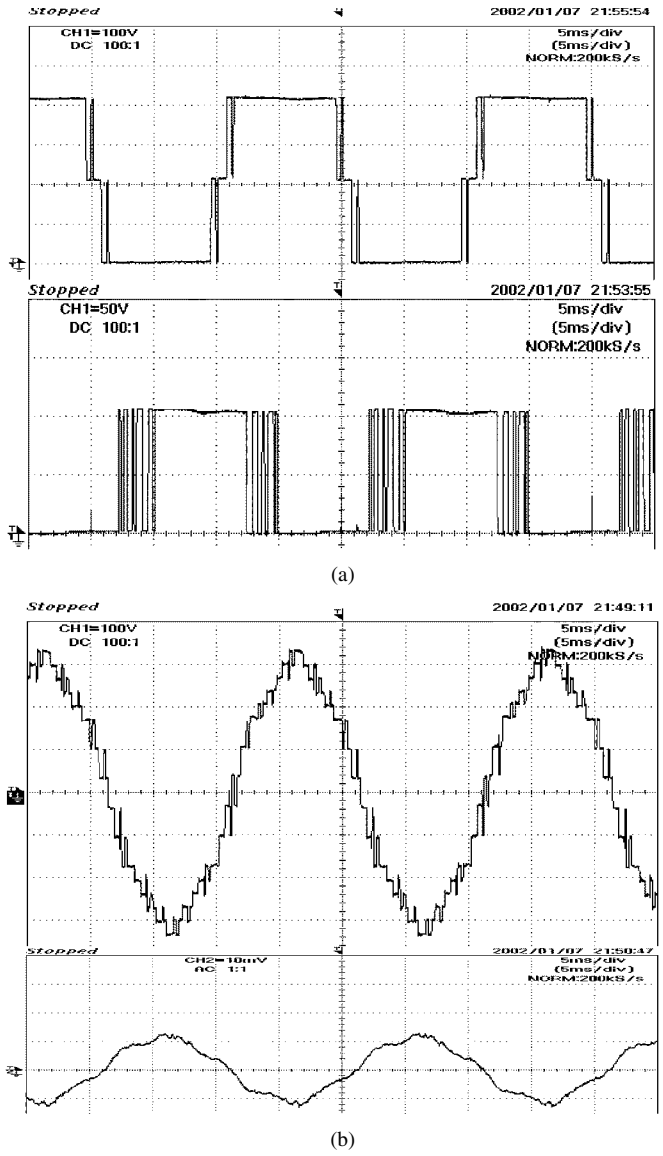


Fig. 11. (a) Pole voltages v_{A2O} (top) and $v_{A3O'}$ (bottom) when $|\mathbf{v}_{\rm sr}| = \mathrm{V}_{\rm dc}$, i.e., overmodulation (experimental result). Scale: X axis: 5 ms/div. Y axis: 100 V/div (top), 50 V/div (bottom). (b) Motor phase voltage v_{A2A3} (top) and the motor phase-current (bottom) when $|\mathbf{v}_{\rm sr}| = \mathrm{V}_{\rm dc}$, i.e., overmodulation. Scale: X axis: 5 ms/div. Y axis: 100 V/div (top), 1A/div (bottom).

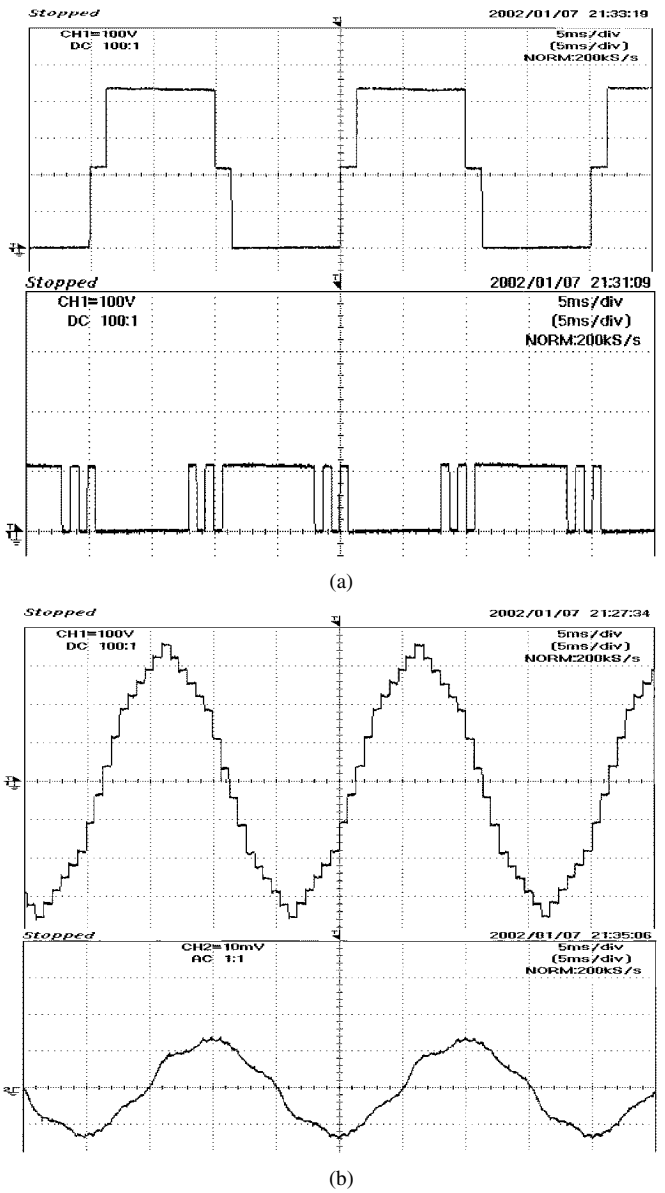


Fig. 12. (a) Pole voltages v_{A2O} (top) and $v_{A3O'}$ (bottom) for 30-step operation (experimental result). Scale: X axis: 5 ms/div. Y axis: 100 V/div (top), 50 V/div (bottom).

rent is slightly distorted compared to the earlier cases due to the increased magnitude of the lower order harmonics in phase voltage.

V. Conclusion

A scheme for a six-level voltage space-vector generation for an open-end winding induction motor in which a three-level and a two-level inverter are connected at either end of the motor has been proposed in this paper. In the proposed scheme, a total of 512 voltage space-vector combinations are present, distributed over 91 space-vector locations. The three-level inverter is realized by connecting two two-level inverters in cascade. This three-level inverter structure does not show the voltage fluctuations of the neutral point, as isolated power supplies are employed to power the individual inverters. Also, it can easily be synthesized by retrofitting two existing two-level inverters. This three-level configuration does not require the clamping diodes.

In the lowest modulation range, only one of the three inverters is switched. In the medium modulation range two inverters are switched and in the higher modulation range all three inverters are switched. This feature ensures that the switching losses are reduced in the lower and the middle ranges of modulation. The motor phase voltage shows a two-level waveform in the lowest modulation range, a three-level or a four-level waveform in the medium modulation range, and a five-level or a six-level waveform in the higher modulation range. This configuration needs three isolated power supplies.

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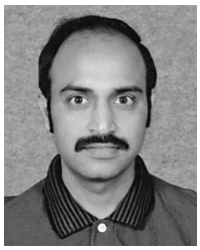

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