A Multilevel Medium-Voltage Inverter for Step-up-Transformer-less Grid Connection of Photovoltaic Power Plants

Md. Rabiul Islam, Youguang Guo, *Senior Member*, *IEEE*, and Jianguo Zhu, *Senior Member, IEEE*

Abstract—**Recently, medium (0.1–5 MW) and large scale (> 5 MW) photovoltaic (PV) power plants have attracted great attention, where medium voltage grid (typically 6–36 kV) connection is essential for efficient power transmission and distribution. A power frequency transformer operated at 50 or 60 Hz is generally used to step-up the traditional inverter's output low voltage (usually ≤ 400 V) into medium voltage level, as the medium voltage PV inverter has not been developed yet. Because of the heavy weight and large size of the power frequency transformer, the PV inverter system can be expensive and complex for installation and maintenance. As an alternative approach to achieve a compact and lightweight direct grid connection, a three-phase medium voltage PV inverter system is proposed in this paper. The 11 kV and 33 kV PV inverter systems are designed. A scaled down 3-phase 1.2 kV test rig is constructed to validate the proposed PV inverter. The experimental results are analyzed and discussed taking into account the switching schemes and filter circuits. The experimental results demonstrate the excellent feature of the proposed PV inverter system.**

Index Terms—**Photovoltaic (PV) power plants, PV inverters, grid integration, medium-voltage, step-up-transformer-less.**

I. INTRODUCTION

SINCE 2007 medium (0.1–5 MW) and large scale (> 5 MW) photovoltaic (PV) power plants have attracted great attention and power plants of more than 10 MW in capacity have thereby become a reality [1], [2]. More than 200 PV power plants have already been installed in the world; each of them generating an output of more than 10 MW. Of these plants, 34 are located in Spain and 26 in Germany. The number of PV power plants will continue to rise. More than 250 PV power plants will be installed within the next few years. Future PV power plants will have higher power capacity. Indeed, some are to have a capacity in excess of 250 MW. These multimegawatt PV power plants require large areas of land. Owing to this, they are usually installed in remote areas, far from cities. The 20 MW PV power plant in Beneixama, Spain, used about 200 SINVERT 100M inverters and installed approximately 100,000 PV modules in a land area of 500,000 m^2. For power transmission, a step-up-transformer is usually used in the PV inverter system to feed-in the solar energy into a medium voltage grid (typically 6–36

kV). ASEA Brown Boveri (ABB) and Siemens developed inverters for medium scale PV power plants. ABB central inverters are especially designed for medium scale PV power plants. The PVS800 version is 3-phase inverters with a power capacity in the range of 100–500 kW. The PVS800 inverter topology allows a parallel connection directly on the ac side, for grid connection through a step-up-transformer. The transformer steps-up the inverter output voltage from 300 V ac to grid voltage level. ABB has been delivering worldwide vacuum cast coil dry-type transformers for PV applications. Siemens developed SINVERT PVS inverter for medium scale PV power plants. The ac output voltage and power capacity of PVS version inverters are in the range of 288–370 V and 500–630 kW, respectively. The 1–2.52 MW central inverters can be designed by parallel connection of 2 to 4 PVS inverters through transformer and switchgear at the grid side. Siemens developed GEAFOL cast-resin transformers for grid connection of PV arrays.

Although these special transformers are compact compared with conventional distribution transformers, they are still large and heavy for remote area PV applications [3]. The large size and heavy weight step-up-transformer may increase the system weight and volume, and can be expensive and complex for installation and maintenance. The medium-voltage inverter may be the possible solution to connect the PV power plant to the medium-voltage grid directly. Moreover, it can be also possible to ensure electrical isolation through the inverter, which is important for the connection of PV power plants with medium-voltage grids. Therefore, medium-voltage inverters for step-up-transformer-less direct grid connection of PV systems have attracted great attention since the installation of large scale PV power plants commercially in 2007.

In 2011, different multilevel inverter topologies were compared for possible medium-voltage grid connection of PV power plants [4], [5]. Because of some special features, the modular multilevel cascaded (MMC) inverter topology is considered as a possible candidate for medium-voltage applications. The component numbers of the MMC inverters scale linearly with the number of levels, and individual modules are identical and completely modular in constriction, thereby enabling high-level number attainability. Furthermore, the MMC inverter does not require any auxiliary diodes and capacitors. Fig. 1 shows the requirements of auxiliary devices in different multilevel inverters. However, the MMC inverter requires multiple-isolated dc sources that must be balanced. In 2011, a high-frequency link was proposed to generate

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multiple-imbalanced sources for asymmetrical multilevel inverters [6]. In the proposed system, only the auxiliary H-bridges are connected through high-frequency-link. The main H-bridges are supplied directly from the source, which means there is no electrical isolation. Therefore, the use of this inverter is only for isolated winding motor applications.
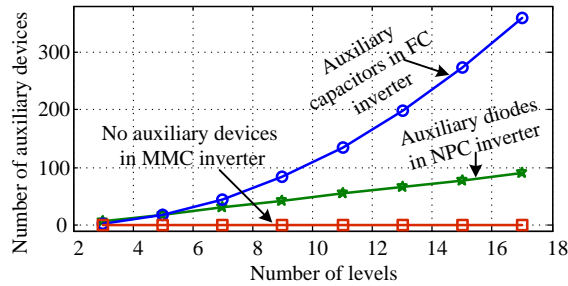

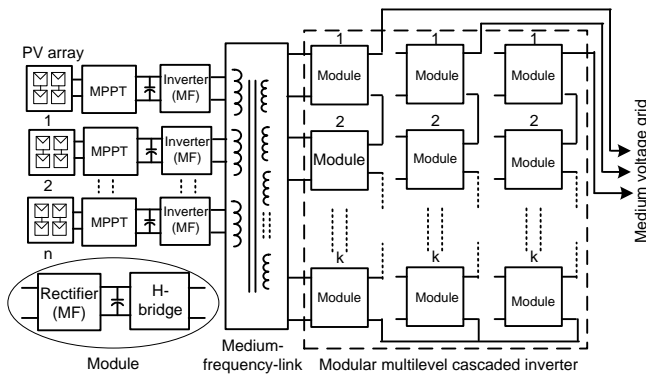Fig. 1. Auxiliary devices in different multilevel inverters.

Fig. 2. Proposed medium-voltage PV inverter system for step-up-transformer-less direct grid integration of PV power plants.

In 2011, a medium-frequency-link operated at a few kHz to MHz was proposed to generate multiple isolated and balanced dc sources for MMC inverters from a single source [7]. In order to verify the feasibility of the new technology, a Metglas amorphous alloy 2605SA1 based medium-frequency link was developed [8]. Compared with the power frequency transformers, the medium-frequency link has much smaller and lighter magnetic cores and windings, thus much lower costs. The amorphous alloy based medium-frequency link shows excellent electromagnetic characteristics, such as very low specific core losses and possibility to generate multiple-balanced sources [9].

In 2012, by combination of a quasi-Z source inverter into a MMC converter, a medium-voltage PV inverter was proposed [10]. The proposed PV inverter does not have isolation between PV array and medium-voltage grid. Multiple-isolated dc/dc converter based inverter topologies were proposed in [11], [12]. In the proposed configuration, the voltage balancing is the challenging issue, since each H-bridge cell is connected to a PV array through a dc/dc converter.

Common dc-link may be one of the possible solutions to minimize the voltage imbalance problem. In 2012, a common dc-link based PV inverter system was proposed [13], [14]. Although this design may reduce the voltage imbalance problem in grid side, the generations of common dc-link

voltage from different PV arrays make the inverter operation complex,and accordingly limit the range of maximum power point tracker (MPPT) operation.

In this paper, a three-phase medium voltage inverter is proposed for step-up-transformer-less direct grid connection of PV power plants. A medium-frequency link (common magnetic-link) instead of common dc-link is used to generate all the isolated and balanced dc supplies of MMC inverter from a single or multiple PV arrays. Accordingly, the link guarantees electrical isolation between the grid and the PV arrays. The basic block diagram of the proposed medium-voltage inverter for medium and large scale PV power plants is shown in Fig. 2. The 11 kV and 33 kV inverter systems are designed and analyzed taking into account the specified system performance, control complexity, cost and market availability of the semiconductors. To verify the feasibility of the proposed inverter system, a scaled down 1.2 kV laboratory prototype test platform is developed with a 5-level MMC inverter. The design and implementation of the prototyping test platform, and the experimental results are analyzed and discussed. The advantages of the proposed PV inverter are: 1) step-up-transformer-less and line-filter-less medium voltage grid connection; 2) an inherent minimization of the grid isolation problem through the magnetic-link; 3) an inherent dc-link voltage balance due to the common magnetic-link; 4) a wide range of MPPT operation; and 5) an overall compact and lightweight system.
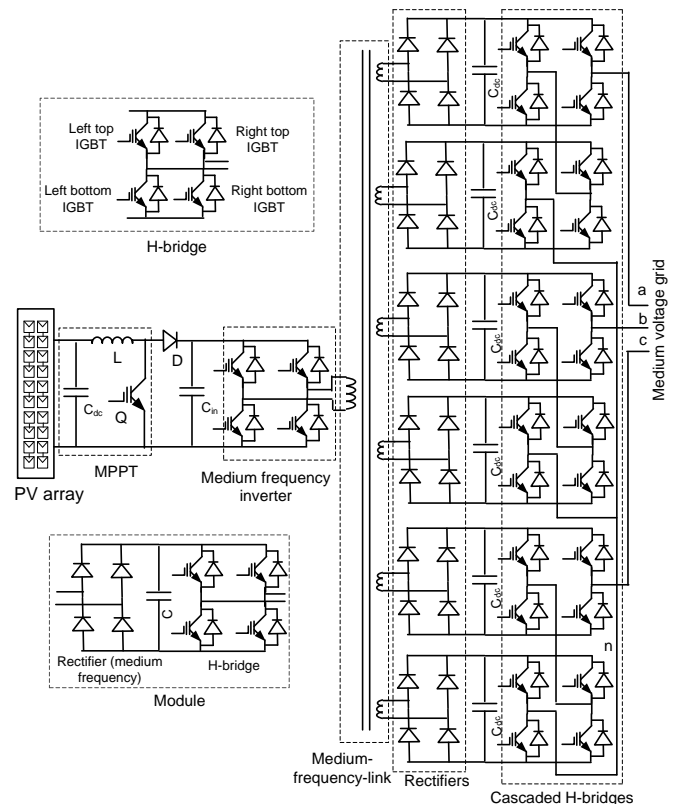

Fig. 3. Detailed power conversion circuit with 3-phase 5-level MMC inverter (for simplicity single PV array is used).

II. PROPOSED PHOTOVOLTAIC SYSTEM

In this paper, as an alternative approach to minimize voltage imbalance problem with wide range of MPPT operation, a Metglas amorphous alloy 2605SA1 based common magnetic-link is considered. The boost converter is considered for MPPT function mainly. The array dc power is converted to a medium-frequency ac through a medium-frequency inverter. The inverter also ensures constant output voltage. The inverter is connected to a primary winding of a multiwinding medium-frequency link. Each secondary winding works as an isolated source and is connected to H-bridge cell through a bridge rectifier. The number of primary windings depends on the number of PV arrays and the number of secondary windings depends on number of levels of the inverter. The detailed power circuit of a 3-phase 5-level PV inverter system is shown in Fig. 3, which is used to validate the proposed inverter in the laboratory. In large PV power plants, several PV arrays are operated in parallel. For this case multi-input and multi-output magnetic-link can be used, where each PV array is connected to a primary winding through a booster and medium frequency inverter as shown in Fig. 2. The magnetic-link provides electrical isolation between PV array and grid, thus inherently overcomes common mode and voltage imbalance problems.
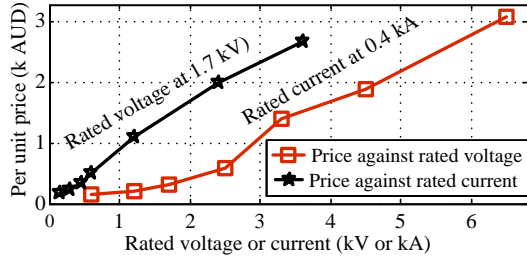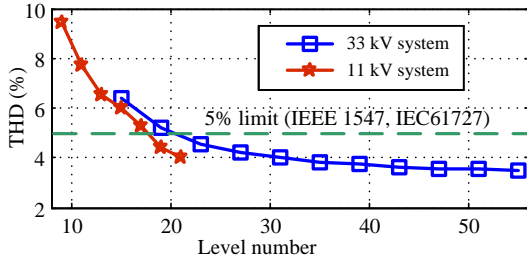

Fig. 4. Per unit price of IGBT, in kAUD

Fig. 5. Calculated THDs at different level number ranging from 7-level to 21-level for an 11 kV system and 15-level to 55-level for a 33 kV system.

III. DESIGN AND ANALYSIS OF THE PROPOSED SYSTEM

If $V_{ll(rms)}$ is the grid line to line voltage and L the number of levels of the inverter, the minimum dc-link voltage of each H-bridge can be calculated from

$$V_{dc(\min)} = \sqrt{2}\frac{V_{ll(rms)}}{(L-1)} . \qquad (1)$$

To determine the nominal dc-link voltage of each H-bridge cell, a voltage reserve of 4 % is assumed, i.e.

$$V_{dc(nom)} = 1.04V_{dc(\min)} . \qquad (2)$$

If $I_{p(rms)}$ is the inverter phase current, the apparent output power can be calculated from

$$S_c = \sqrt{3}V_{ll(rms)}I_{p(rms)} . \qquad (3)$$

The highest voltage rating of commercially available insulated gate bipolar transistor (IGBT) is 6.5 kV and this is suitable for 2.5 kV or lower voltage inverter systems with traditional 2-level inverter topology. Although high-voltage devices such as 3.3, 4.5 and 6.5 kV IGBTs are available in the market, they are still costly as shown in Fig. 4. The lower-voltage devices, such as 0.6, 0.9, 1.2, 1.7 and 2.5 kV IGBTs are not only mature in technology but also cheap. On the other hand, the cascaded connection of low-voltage rated semiconductors can be a cost effective solution for medium voltage inverter applications. The high-number of levels means that medium-voltage attainability is possible to connect the PV array to the medium-voltage ac network directly and also possible to improve the output power quality. The total harmonic distortions (THDs) of 11 kV and 33 kV inverter systems are illustrated in Fig. 5. The component number and control complexity increase linearly with the increase of level number. Therefore, optimal selection of number of inverter levels is important for the best performance/cost ratio of the PV systems.

Each H-bridge cell communication voltage of a 7-level topology based 11 kV inverter is 2696 V which may be supported by the 6.5 kV IGBT. Thus at least 7-level topology is required to design the 11 kV inverter. The output power quality of 21-level inverter is good enough to feed into the 11 kV ac grid directly. The cheap 1.7 kV IGBT can be used to design the 21-level inverter. For a 33 kV system, at least 15-level topology is required and 55-level topology is sufficient for the power quality. Therefore, 7-level to 21-level modular multilevel cascaded inverter topologies are considered for an 11 kV inverter system and 15-level to 55-level topologies are considered for a 33 kV inverter system. The device voltage utilization factor (DVUF), ratio of commutation voltage of respective commutation cells (V_{com}) and device commutation voltage for a device reliability of 100 failures in time (FIT) due to cosmic radiation ($V_{com@100FIT}$), are summarized in Tables I and II.

TABLE I
DVUF WITH DIFFERENT LEVEL NUMBER OF AN 11 kV SYSTEM

Level number	V_{com}	Rated device voltage kV	$V_{com@100FIT}$	DVUF (%)
7	2696	6.5	3600	75
9	2022	4.5	2250	90
11	1618	3.3	1800	90
13	1348	3.3	1800	75
15	1156	2.5	1200	96
17	1011	2.5	1200	84
19	898	1.7	900	99
21	809	1.7	900	90

Higher DVUF is essential for cost effective design, since semiconductor cost is the significant figure in medium-voltage

inverter applications. From Tables I and II, it can be seen that only a few inverters have high DVUF. In order to ensure cost effective design, the inverters with level numbers of 9, 11, 15, 19 and 21 for an 11 kV system and 15, 23, 29, 43 and 55 for a 33 kV system were considered for the further analysis. The 11 kV and 33-kV systems with the selected inverter topologies are designed and analyzed in the MATLAB/Simulink environment. The number of arithmetic and logic operations (ALOs) for switching section and cost of semiconductors are calculated as summarized in Tables III and IV. The number of ALOs is used to compare the complexity of the inverters. The THDs are calculated through the MATLAB/Simulink environment at a switching frequency range of 1–2 kHz. If P_{c_inv} is the conduction loss and P_{sw_inv} is the switching loss of semiconductor devices, the total losses in the inverter section of the proposed system can be described as

$$P_{loss\_inv} = P_{c\_inv} + P_{sw\_inv}. \qquad (4)$$

TABLE II
DVUF WITH DIFFERENT LEVEL NUMBER OF A 33 kV SYSTEM

Level number	V_{com}	Rated device voltage kV	$V_{com@100FIT}$	DVUF (%)
15	3467	6.5	3600	96
17	3034	6.5	3600	85
19	2697	6.5	3600	75
21	2427	6.5	3600	68
23	2206	4.5	2250	98
25	2022	4.5	2250	90
27	1867	4.5	2250	83
29	1734	3.3	1800	96
31	1618	3.3	1800	90
33	1517	3.3	1800	84
35	1428	3.3	1800	79
37	1348	3.3	1800	75
39	1277	3.3	1800	71
41	1214	3.3	1800	65
43	1156	2.5	1200	96
45	1103	2.5	1200	92
47	1055	2.5	1200	88
49	1011	2.5	1200	84
51	971	2.5	1200	81
53	934	2.5	1200	78
55	899	1.7	900	100

TABLE III
INVERTER COMPARISON FOR AN 11 kV SYSTEM

Level number	9	11	15	19	21
IGBTs	48	60	84	108	120
THD (%)	9.60	8.20	6.00	4.30	4.25
Cost (AU$)	86400	82159	47066	36670	40744
ALOs	44	55	77	99	110

TABLE IV
INVERTER COMPARISON FOR A 33 kV SYSTEM

Level number	15	23	29	43	55
IGBTs	84	132	168	252	324
THD (%)	6.40	4.54	4.12	3.61	3.47
Cost (AU$)	258552	237600	229992	141200	110030
ALOs	77	121	154	231	297

The switching losses in a multilevel inverters was approximated by [15]

$$P_{sw\_inv} = (AI_r + BI_r^2)f_c. \qquad (5)$$

where f_c is the carrier frequency of multilevel inverter. The switching loss of an active switch is proportional with the carrier frequency. The carrier frequency can be reduced linearly with the increase in number of levels. Although the number of active switching devices increases linearly with the number of levels, the reduction of carrier frequency can keep the total switching loss constant. The conduction losses in a switch and in an anti-parallel diode were represented by [15]

$$P_{c\_sw} = \frac{1}{2}I_rV_t\left(\frac{1}{\pi} + \frac{m_a}{4}p_f\right) + I_r^2R_{CE}\left(\frac{\sqrt{3}}{8\sqrt{\pi}} + \frac{m_a}{3\pi}p_f\right). \qquad (6)$$

and

$$P_{c\_D} = \frac{1}{2}I_rV_f\left(\frac{1}{\pi} - \frac{m_a}{4}p_f\right) + I_r^2R_{AK}\left(\frac{\sqrt{3}}{8\sqrt{\pi}} - \frac{m_a}{3\pi}p_f\right). \qquad (7)$$

where m_a is the amplitude modulation index, p_f the power factor of the current, I_r the device current, and V_t and V_f are the voltage drops at zero current condition, and R_{CE} and R_{AK} are the forward resistances of IGBT and diode, respectively, which can be collected from the manufacturer's data sheets.

The inverter section of the system consists of a series of H-bridge inverter cells in a cascaded connection. Therefore, the total conduction losses of an m-level inverter can be approximated as

$$P_{c\_inv} = 6(m-1)(P_{c\_sw} + P_{c\_D}). \qquad (8)$$

The device communication voltage of m-level inverter is (m-1) times lower than that of a device in the 2-level inverter. The on-state voltage drops of an IGBT and forward voltage of a diode are highly dependent on device voltage ratings. Fig. 6 plots the on-state voltage drops of different rated Mitsubishi Electric IGBTs. For these reasons, although the number of devices increases linearly with the number of levels, the total conduction loss can be constant. Therefore, the efficiency of the multilevel inverter remains almost constant to the variation of number of levels, and thereby the efficiency was not considered for the selection of number of levels.
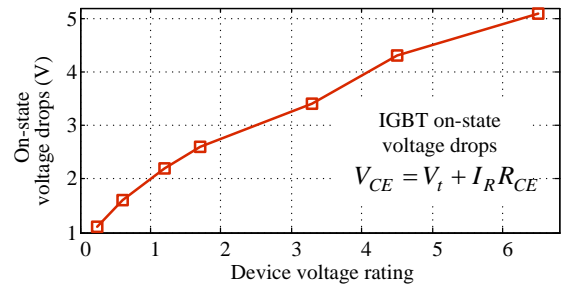

Fig. 6. On-state voltage drops of 600 A rated IGBTs.

If y is the given value, y_{min} the minimum value, and y_{max} the maximum value on a respective row of each inverter system, the normalized index value can be calculated as

$$I_d = \frac{y - y_{\min}}{y_{\max} - y_{\min}} \; . \tag{9}$$

Tables V and VI summarize the normalized index values of Tables III and IV, respectively. Based on Tables V and VI, the overall performance graphs are plotted in Figs. 7 and 8, respectively. For an 11 kV inverter, the total index value is the lowest at 19-level, because there is no significant output power quality improvement and semiconductor cost reduction for inverters with more than 19 levels. Furthermore, the component number and control complexity increase linearly with the increase in the number of levels. Therefore, 19-level topology is the optimal choice for an 11 kV PV inverter system. Similarly 43-level topology is the optimal choice for a 33 kV PV inverter system. The output voltages of 19-level and 43-level MMC inverters are shown in Figs. 9 and 10.

TABLE V
OVERALL COMPARISON FOR AN 11 KV SYSTEM

Level number	9	11	15	19	21
Performance	1.00	0.74	0.33	0.01	0.00
IGBTs cost	1.00	0.92	0.21	0.00	0.09
Complexity	0.00	0.17	0.50	0.83	1.00
Total index	2.00	1.83	1.04	0.84	1.09

TABLE VI
OVERALL COMPARISON FOR A 33 KV SYSTEM

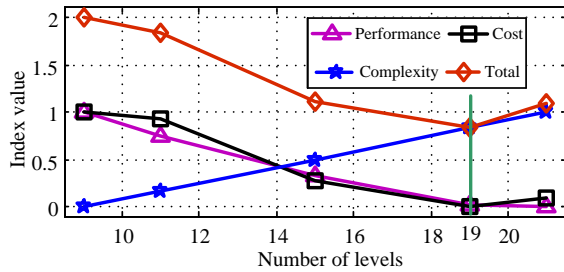| Level number	15	23	29	43	55
Performance	1.00	0.36	0.22	0.04	0.00
IGBTs cost	1.00	0.85	0.80	0.20	0.00
Complexity	0.00	0.20	0.35	0.70	1.00
Total index	2.00	1.41	1.37	0.94	1.00

Fig. 7. A graphical representation of index values at different number of levels ranging from 9-level to 21-level for an 11 kV system.
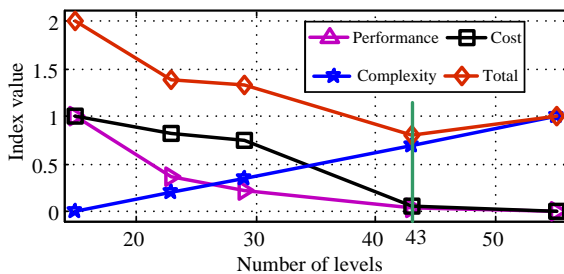

Fig. 8. A graphical representation of index values at different number of levels ranging from 15-level to 55-level for a 33 kV system.

The output power quality is good enough to feed the inverter output into the medium voltage grid directly. The THDs of an 11 kV inverter and of a 33 kV inverters are 4.3% and 3.6%, respectively.
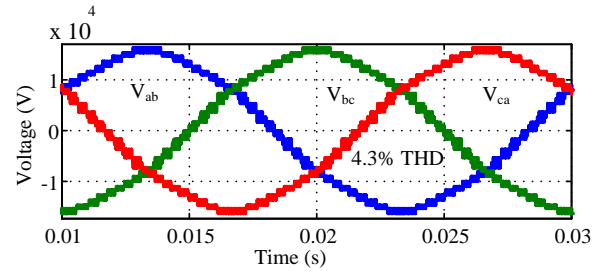

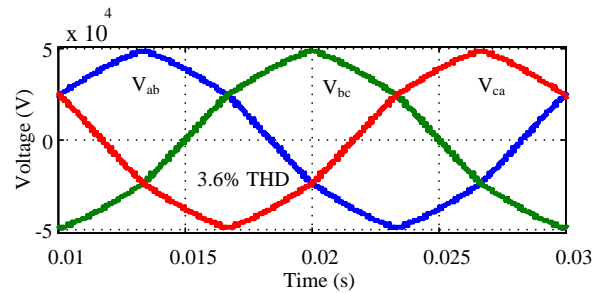Fig. 9. Line voltages of 19-level 11 kV inverter; without filter.

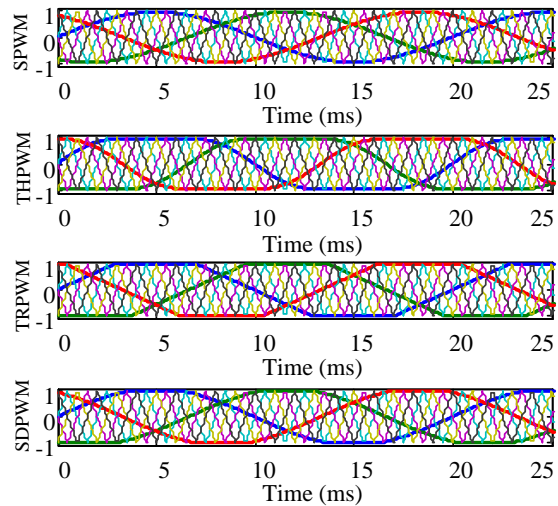Fig. 10. Line voltages of 43-level 33 kV inverter; without filter.

Fig. 11. Four different modulation schemes, where thin lines are the carrier signals and thick lines are the reference signals.

TABLE VII
THD (%) FOR DIFFERENT MODULATION SCHEMES

Level number	7	9	11	13	15	17	19
SPWM	11.80	9.60	8.20	6.90	6.00	5.20	4.30
THPWM	9.10	7.60	6.10	4.80	4.10	3.80	3.50
SDPWM	12.10	10.50	9.20	7.80	7.00	6.10	5.20
TRPWM	12.40	10.50	9.30	8.20	7.70	7.40	7.10

Different types of major reference signals used in the traditional converters can also be used in the multilevel

converter system: sinusoidal, third harmonic injected sinusoidal, sixty degree modulated sinusoidal and trapezoidal. The reference signals and phase-shifted carrier signals for 3-phase 5-level converter system are depicted in Fig. 11. Each has its unique advantages and disadvantages. It is possible to reduce the switching losses by reducing the number of switching in each period. Flatting the top of the reference signal waveform in the third harmonic injected sinusoidal, sixty degree modulated sinusoidal and trapezoidal not only allows the possibility of switching loss reduction but also increases the range of linear modulation. In this paper, four modulation schemes: the phase-shifted carriers with sinusoidal references (SPWM), the phase-shifted carriers with third harmonic injected sinusoidal references (THPWM), the phase-shifted carriers with sixty degree modulated sinusoidal references (SDPWM) and the phase-shifted carriers with trapezoidal type references (TRPWM) are applied on the 7-level to 19-level SCHB converter systems to analyze the performance. Among these four modulation schemes the THPWM scheme gives the best harmonic performance and SDPWM and TRPWM schemes have higher lower-order harmonic content than SPWM and THPWM schemes. Moreover, SPWM has shown higher reduction rate for high level number. Table VII summarizes the harmonic performance of different switching schemes.

IV. EXPERIMENTAL TESTING AND RESULTS ANALYSIS

A 5-level 3-phase MMC inverter requires six isolated and balanced dc sources. To couple the PV array to the 5-level inverter, a Metglas amorphous alloy 2605SA1 based medium-frequency link with six secondary windings is used. To minimize the proximity effect, Litz wires are used for windings with single layer placement as shown in Fig. 12. The medium-frequency link is excited by a 10 kHz square wave primary voltage, which is generated by an H-bridge inverter supplied by a 220 V PV array. The output of each secondary winding is connected to a fast recovery diode based rectifier with a low pass RC filter circuit. The electromagnetic performances of all secondary windings were found almost the same. Such similarity of characteristics is obligatory to generate balanced multiple sources for the MMC inverters.

The performance of digital signal processor (DSP) is limited by the clock rate, and the number of useful operations per clock. In addition, the available DSP can only at present provide about six pairs of PWM channels, which is clearly insufficient for the multilevel inverter systems (e.g. a 3-phase 5-level inverter requires 24 PWM signals). In this paper, a fully digital switching controller is developed and implemented with a Xilinx XC3S500E field programmable gate array (FPGA). The most common softwares such as MATLAB/Simulink and Xilinx ISE based design technique are used to develop the controller, which may save the development time and cost of the switching controller. Fig. 13 shows the basic architecture of the switching controller. In total, three reference signals are required, one for each phase leg. Look-up tables are used to generate the third harmonic injected sinusoidal reference signals and pure sinusoidal reference signals (only one in operation at a time) which

makes the control circuit totally digital and integrated. Including the inverted carrier signals, a total of four carriers are able to generate four gate pulses when comparing them with a reference signal. The other four gate pulses can be generated by just inverting these four gate pulses with a consideration of deadtime. In this project, 9-bit up-down counters are used to generate phase-shifted carrier signals. Fig. 14(a) shows the measured four PWM gate pulses for the top H-bridge cell in phase B. The input/output voltage waveforms of the medium-frequency link and dc-link voltage of the H-bridge module are shown in Fig. 14(b). The voltages before and after the boost converter or MPPT were measured as shown in Fig. 15.
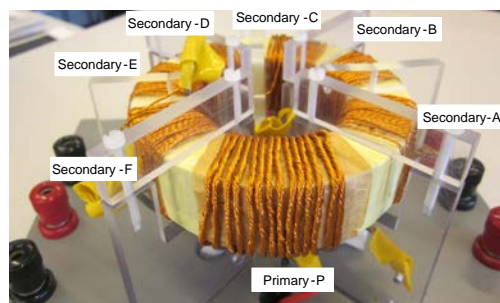

Fig. 12. Photograph of the medium-frequency link; Metglas sheet of 20 μm thickness and 25 mm width was glued with Araldite 2011 on the surface of each layer to develop the core.
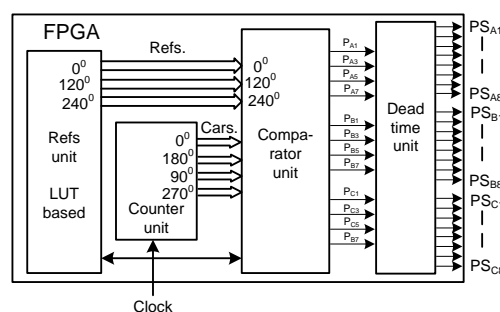

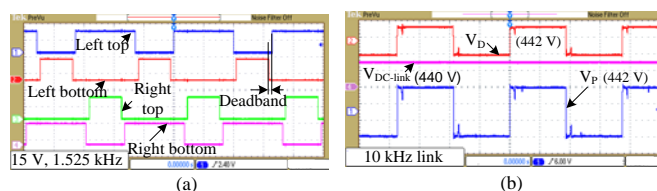Fig. 13. Architecture of the FPGA based switching controller.

Fig. 14. Measurement: (a) gate pulses for the top H-bridge cell in phase A, and (b) input/output voltage waveforms of the medium-frequency link and dc-link voltage of the H-bridge module.
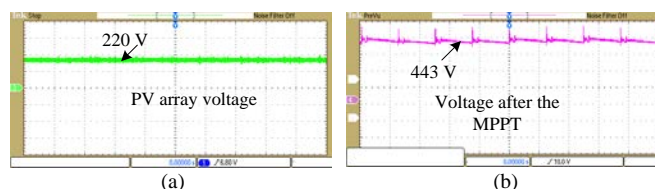

Fig. 15. Measured voltage: (a) before the boost converter, and (b) after the boost converter.

A scaled down 1.2 kV 3-phase 5-level MMC inverter is developed by using Semikron compact IGBT module SK30GH123 with Semikron isolated driver SKHI 20opA. Fig. 16 shows a photograph of the test platform.
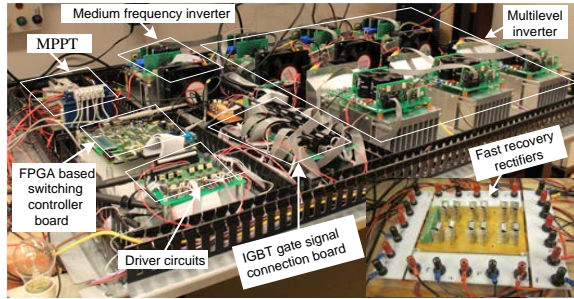

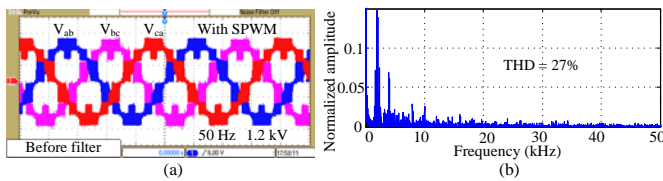Fig. 16. Photograph of the 1.2 kV, 2.5 kVA prototype test platform.

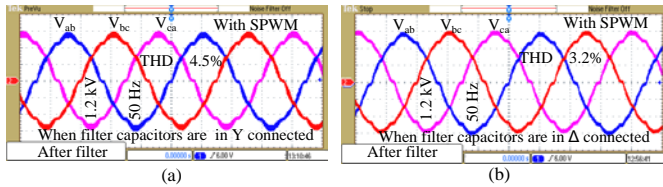Fig. 17. Line to line voltages with SPWM of the prototype system before filter circuit.

Fig. 18. Line to line voltages with SPWM of the prototype system after the filter when filter capacitors are: (a) in Y connected and (b) in Δ connected.

The SPWM and THPWM schemes are implemented and performances were verified by measuring the line voltages and they were found highly consistent with the theoretical and simulation results. The LC filter circuit is designed with 3 mH MTE RL 00401 reactor and 6 μF RS MR-P-MC-S-NF capacitors. In each phase, three capacitors are connected in series, which provides equivalent 2 μF capacitance with a rated voltage at 1.32 kV. The line to line voltages before filter circuit with SPWM scheme are illustrated in Fig. 17(a). Fig. 17(b) shows that the SPWM scheme gives higher THD, which was about 27%. The performances are also observed with Y and Δ connection of filter capacitors. The line voltages after filter circuit are shown in Fig. 18(a), when capacitors were Y connected. The significant improvement was observed when filter capacitors were Δ connected; THD reduced from 4.5% to about 3.2%. After filter circuit, the line voltages are depicted in Fig. 18(b), when capacitors are Δ connected. Fig. 19 shows the zoomed (zoom factor = 6) output line voltages for different combination of filter capacitors. The THPWM scheme provides much better results than the results with SPWM, which was found highly consistent with the simulation results. The line voltage waveforms before filter circuit with THPWM are illustrated in Fig. 20, which contains about 19% THD and

after filter it is reduced to less than 2.8%. Fig. 21 plots the line voltages after filter circuit, where capacitors are in Δ connected.

The line current waveforms with the filter circuit are shown in Fig. 22(a). As measured, with the filter circuit, the line current waveform contains about 2.72% THD. The frequency spectrum of line current with filter is illustrated in Fig. 22(b). The boost converter executes the MPPT, automatically adjusting output power according to the environment conditions (irradiance and temperature). The modified incremental conductance method is considered to track the maximum power point [16], [17]. The duty cycle can be changed by changing the reference current of the boost converter, in order to adjust the operating point to the maximum power point. To maintain a constant output voltage the medium frequency inverter gate pulses are controlled.
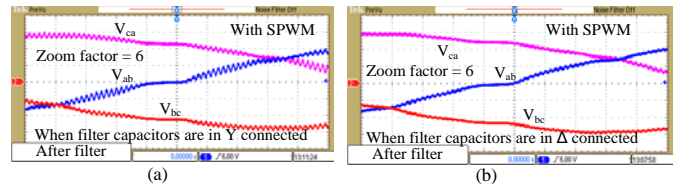

Fig. 19. Zoomed line to line voltages with SPWM of the prototype system after the filter when filter capacitors are: (a) in Y connected and (b) in Δ connected.
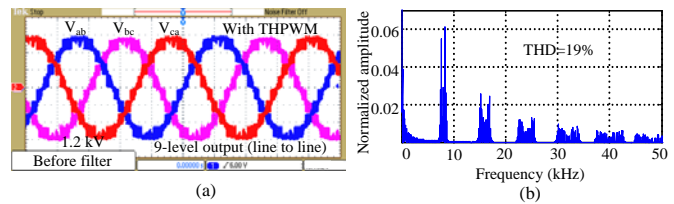

Fig. 20. Line to line voltages with SPWM of the prototype system before the filter.
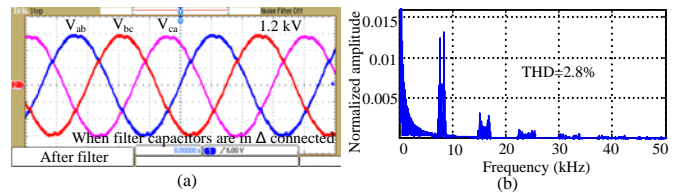

Fig. 21. Measured line voltages of the prototype inverter after the filter circuit.
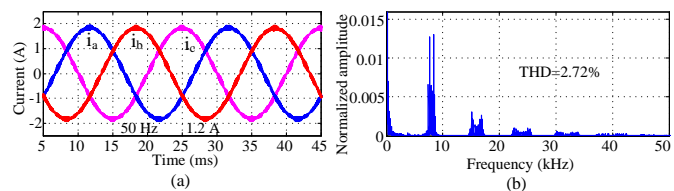

Fig. 22. Frequency spectrum of line voltage with filter circuit.

The multilevel inverter section of the proposed system gives about 92% efficiency with the fully rated power condition. The overall efficiency of the whole system was also calculated. The overall efficiency was much lower than that of

the multilevel inverter section due to the significant power losses in the dc-dc converter, 10 kHz inverter, medium-frequency link, and fast recovery rectifiers. The full load overall efficiency of the proposed system was measured at 75%. Table VIII summarizes the efficiency of the prototype inverter with different load conditions. Compared with the traditional PV inverter system (2-level inverter section only) about 15% lower efficiency was evaluated. Although the proposed system gives about 15% lower efficiency than that of a 2-level inverter, the overall performance is still similar to a 2-level inverter based traditional PV system, because the traditional system uses two main additional components, i.e. line filter, and the step-up transformer. The step-up transformers and harmonic neutralizing filters produce about 50% of the total losses and occupy up to 40% of the system volume [18]. With the proposed inverter, the elimination of the heavy and large step-up transformer and line filter will enable large cost savings in terms of the installation, running and maintenance of PV power plants.

TABLE VIII
EFFICIENCY OF THE PROPOSED PV INVERTER

Load (%)	Efficiency (%)	
	Multilevel inverter section	Overall system
25	75	50
50	86	65
75	89	70
100	92	74

V. CONCLUSION

In this paper, a new medium voltage PV inverter system is proposed for medium or large scale PV power plants. A common magnetic-link has been considered to interconnect PV arrays to form a single source. Multiple isolated and balanced dc supplies for multilevel inverter have been generated through the common magnetic-link, which automatically minimizes the voltage imbalance problem. The grid isolation and safety problems have also been solved inherently due to electrical isolation provided by the medium-frequency link. Although the additional windings and rectifiers may increase the loss of the proposed inverter, still the overall performance is similar with the traditional system, because the proposed inverter eliminates three main parts: 2-level inverter, line filter, and step-up transformer from the system. In this paper, the proposed system has been validated by a scaled down 1.2 kV prototype system. The same concept can be used to develop 6–36 kV system by changing the number of secondary windings and the number of levels of the inverter.

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