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**Version of attached file:**

Published Version

**Peer-review status of attached file:**

Peer-reviewed

**Citation for published item:**

Ng, C. H. and Parker, M. A. and Ran, L. and Tavner, P. J. and Bumby, J. R. and Spooner, E. (2008) 'A multilevel modular converter for a large, lightweight wind turbine generator.', *IEEE transactions on power electronics.*, 23 (3). pp. 1062-1074.

**Further information on publisher's website:**

<http://dx.doi.org/10.1109/TPEL.2008.921191>

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# A Multilevel Modular Converter for a Large, Light Weight Wind Turbine Generator

Chong H. Ng, Max A. Parker, Li Ran, *Member, IEEE*, Peter J. Tavner, *Member, IEEE*, Jim R. Bumby, and Ed Spooner

**Abstract**—In an onshore horizontal axis wind turbine, generator and converter are usually in the nacelle on the top of the tower, while the grid step-up transformer is placed at the bottom. Electric power is transmitted down through flexible cables of high current rating which are expensive and can suffer from large  $I^2R$  loss. An offshore wind turbine usually has to include the step-up transformer in the nacelle. This adds significantly to the mechanical loading of the tower even new designs aim to reduce the transformer size and weight. In either case, a transformer-less, high voltage, high reliability generating unit for nacelle installation would be an attractive technology for large wind turbines. This study presents a power electronic solution based on a permanent magnet generator design. A multilevel cascaded voltage source converter is developed to synthesize a high sinusoidal output voltage. The dc link voltages of inverter modules are balanced by rectifiers fed from isolated generator coils while the inverter switching strategy equalizes the power sharing between the modules. The switching strategy also reduces the low order harmonics to constrain the sizing of the dc link capacitors. The modulating effect between the ac and dc sides of the inverter is taken into account. This paper describes the generator-converter arrangement, analyzes the inverter switching effects and derives the switching strategy which is verified by simulation and laboratory experiment.

**Index Terms**—DC link capacitor, grid connection, harmonics, multilevel inverter, power balance, wind power.

## I. INTRODUCTION

VARIABLE speed generators are used for large turbines, as they can extract more energy with attenuated structural stresses and acoustic emissions compared to fixed speed systems. The doubly fed induction generator (DFIG) with a partially rated rotor side converter is currently the mainstream technology in the market for large wind turbines. But other topologies exist and new ones are being developed at lower cost with higher performance and reliability. For instance, low speed, direct drive generators offer a specific reliability benefit by eliminating the gearbox. Among the concepts pursued by different teams, permanent magnet generators with air-cored or iron-cored and slotless geometries have been particularly developed at Durham University [1], [2]. The air-cored generator features a light structure and large diameter to increase

the peripheral speed providing an adequate emf with reduced flux density and accommodating the large number of isolated stator coils. The slotless design could be of smaller diameter but would also incorporate a large number of isolated stator coils. In either case the objective is to reduce the generator weight for large direct drive wind turbine applications of output greater than 4.5 MW. This leads to light machine constructions in which the air gap dimensions are relatively flexible under self-weight and load conditions, resulting in variations in the emfs developed in the coils.

This paper is a study of the electronic power conversion stage of such wind turbines aimed at application on such generators.

In many direct drive systems, including the one that is concerned here, fully rated converters are required to control the generator and interface to the grid. Commercially available converters can be costly but also limited regarding the control functions needed for grid connection. This study demonstrates a new modular converter with a switching strategy that can be integrated into a modular permanent magnet generator so that the overall performance, cost and reliability can be improved.

It is quite easy to obtain a high current rating with a voltage source converter but to obtain high voltage rating can be costly. Therefore in most wind turbine systems, a step-up transformer is needed on the grid side. In an onshore horizontal axis turbine, the generator and converter are housed in the nacelle at the top of the tower. However the step-up transformer is usually located at ground level. In wind turbines with yaw control, which usually means large turbines, electrical power is transmitted from the nacelle using droop cables. In order to cope with excessive wind-up or twisting, a cable length margin is incorporated of up to three to four times tower height. In low voltage systems therefore high current flows through cables of considerable length, induce significant  $I^2R$  loss. Paralleling the cables reduces the loss but increases initial cost as high current cables are expensive. There are modified transformer designs which aim to reduce the size and weight so that the transformer can be included in the nacelle. In spite of the progress made, this adds significantly to the mechanical loading of the tower and hence has mainly been adopted in offshore turbines where estate at sea level is costly. Wind farm developers often use transformers that are marginally rated, to minimize the component cost. The reliability of the whole system is then reduced. Records show that failures of these components have caused significant downtime in existing wind farms [3]–[5] and it is essential to improve the reliability of large wind turbines if they are to be positioned offshore. It is therefore desirable to develop a generator-converter system that can still be housed in the nacelle but output at

Manuscript received September 5, 2007; revised October 25, 2007. Recommended for publication by Associate Editor J. Guerrero.

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Digital Object Identifier 10.1109/TPEL.2008.921191

high voltage and hence reduce the current for direct grid interface without the need for a step-up transformer. There are also cost considerations for the architecture of the generator and converter architecture as described in [6].

Commercial two-level voltage source converters are usually of low voltage design limited by the device rating. The maximum ac voltage is 690 V using 1700 V IGBTs. Multilevel converters can provide higher voltage rating but cannot be obtained as an off-the-shelf product. A well known technical difficulty of a multilevel converter is balancing the dc link voltages in particular when the converter is processing real power [7]–[9].

This paper shows a method of applying a modular multilevel converter to a permanent magnet generator with a large number of isolated coils. A simplified representation of the generator-converter arrangement is shown in Fig. 1. The coil voltages are actively rectified to stabilize the dc links. This avoids the fundamental problem of balancing the dc link voltages but initial study indicates that three issues must be addressed in order for the system to achieve the intended objectives.

DC link voltages contain second order etc. harmonics which cause zero sequence harmonic voltages at the ac output. In the present application, the multilevel modules are connected in a three-phase star with neutral earthed to allow detection of phase to ground fault. The wind farm transformer is configured in  $Y_0-Y_0$  for the same reason, providing a zero sequence current path. The switching strategy must prevent any adverse modulation which will otherwise be absorbed by over-sizing the system components.

In order to produce a genuine modular design, the power extracted from each generator coil should ideally be equal. The dc link voltage balancing issue is translated into the requirement for equalizing the real power that is extracted from each dc link level. The switching strategy of the multilevel inverter must therefore equalize real power sharing between the converter levels.

Identical coils and converter modules could then be mass-manufactured to reduce individual costs and raise system reliability. Fault tolerant operation could also be achieved as a result.

An overall control strategy is used to regulate the output real power of the converter according to the speed of the turbine for maximum power tracking [10]. This is achieved by changing the phase angle of the output voltage. In order to control the output reactive power, the voltage amplitude is controlled, requiring control of each of the dc link average voltages. This is achieved by using an active rectifier for each coil as shown in Fig. 1. In addition to the above three issues, a transformer-less configuration must prevent dc current injection into the grid [11]. The raised output voltage of the converter reduces the output current and developments in instrumentation have enabled active cancellation of dc current injection by feedback control [12], [13] but this issue is not considered further in this paper. Results regarding the dynamic behaviour of the converter during grid disturbances are presented in [14].

This paper derives a steady state switching strategy for the multilevel inverter by addressing the above three issues using simulation and a 2.5 kW experimental machine and modular converter system. An 11 kV, 1.8 MW wind turbine system is

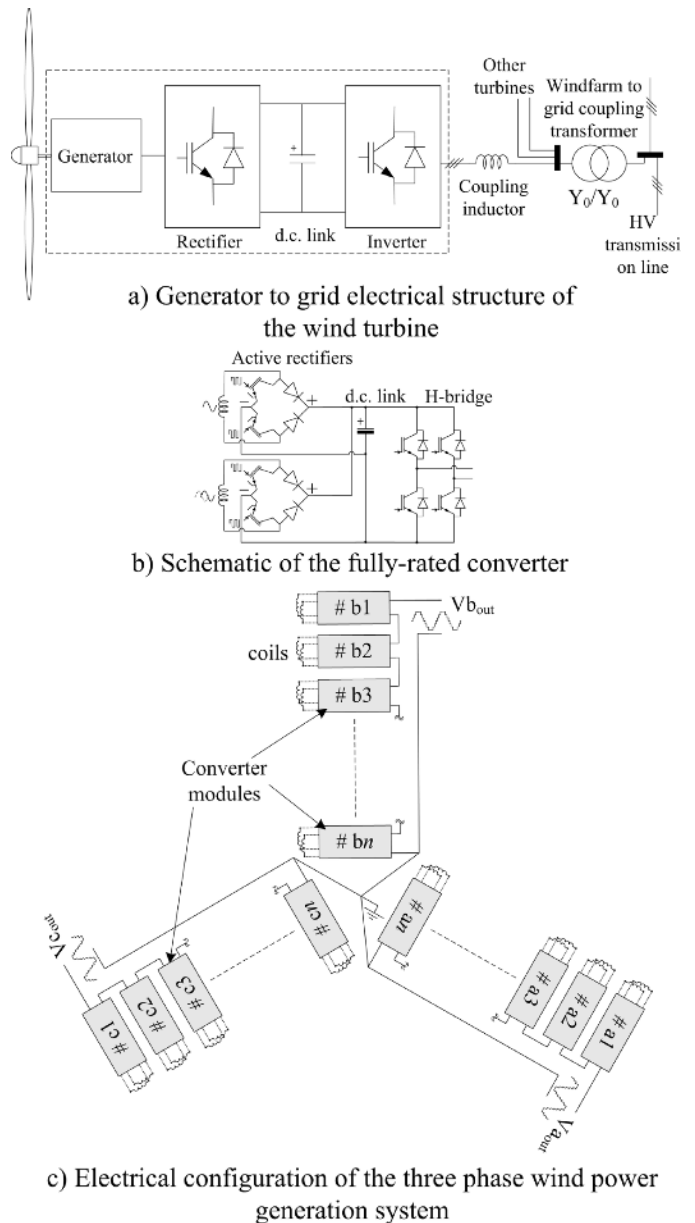


Fig. 1. (a) Wind turbine to grid electrical connection block diagram, (b) schematic of the converter, and (c) configuration of the proposed modular three phase wind power generator.

then considered to demonstrate the effectiveness of the system under full-size conditions but the results of the paper could be extended to any other applications. It is assumed that the generator design can always be arranged to provide the necessary number of coils and the phase relationship between the coil voltages.

Section II outlines the main reasons for adopting the generator-converter configuration. Section III analyzes the harmonic characteristics, which depend on the switching strategy and affect the sizing of some components, in particular the dc link capacitors. Section IV derives the desired switching strategy by considering the requirement of power sharing and determining the optimum switching angles. Section V gives an experimental evaluation of the scheme and presents the experimental results. Section VI supports the experimental results by further simulation studies on a full scale system.

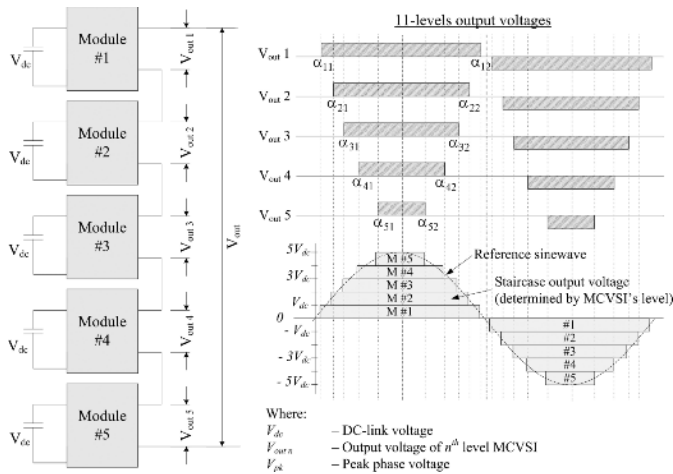


Fig. 2. Multilevel cascaded voltage source inverter (11-level) configuration and its output voltage waveform.

## II. MULTILEVEL CASCADED VOLTAGE SOURCE INVERTER (MCVSI)

H-bridge inverter modules are connected in series on the output ac side to form an MCVSI. The dc link of each module is stabilized by active rectifiers fed from generator coils. The total input power into each dc link can be controlled to be ripple free, except for the high frequency spikes due to switching of the active rectifiers. Referring to Fig. 1(b), each dc link is supplied by two generator coils. The active rectifier controls the current extracted from each coil so that a unity power factor is obtained at the coil terminals. Constant dc side power is obtained if the sinusoidal voltages of the two coils are phase shifted by  $90^\circ$ s as shown in (1) below. The coil voltage ( $V$ ) depends on the machine speed while current ( $I$ ) is set by the control loop to stabilize the dc link voltage

$$p_{dc\_link}(t) = \sqrt{2}V \sin(\omega t) \sqrt{2}I \sin(\omega t) + \sqrt{2}V \sin\left(\omega t + \frac{\pi}{2}\right) \sqrt{2}I \sin\left(\omega t + \frac{\pi}{2}\right) = 2VI. \quad (1)$$

One phase of the grid inverter and its output voltage waveform using the standard switching scheme [15] are expanded in Fig. 2, taking as an example a five-module system resulting in an 11-level phase-neutral voltage waveform. The dc link voltages of the inverter modules, which are assumed to be equal, are switched to synthesize the desired sinusoidal waveform. Each module operates according to a switching function which can be considered as taking values of  $+1$ ,  $0$  and  $-1$  corresponding to  $+V_{dc}$ ,  $0$  and  $-V_{dc}$  respectively at the ac output of the module where  $V_{dc}$  is the dc link voltage. The standard switching angles for different number of modules can be found in [16] and they are set to reduce the output harmonic content. The module duty cycles are different causing unequal real power sharing, which will be addressed later.

There exist other multilevel inverter topologies, in particular the neutral point clamped (NPC) and flying capacitors (FC). They all aim to reduce the voltage stress on the individual switching devices in high voltage applications. The switching frequency of each device is kept low, resulting in low switching

TABLE I  
UNITS FOR MAGNETIC PROPERTIES

|                   | MCVSI     | NPC          | FC       |
|-------------------|-----------|--------------|----------|
| Switching devices | $2(m-1)$  | $2(m-1)$     | $2(m-1)$ |
| Clamping diodes   | $n/a$     | $(m-1)(m-2)$ | $n/a$    |
| Capacitors        | $(m-1)/2$ | $m-1$        | $2m+1$   |

Note: Clamping capacitors in NPC are assumed to have the same rating as d.c.-link storage capacitors

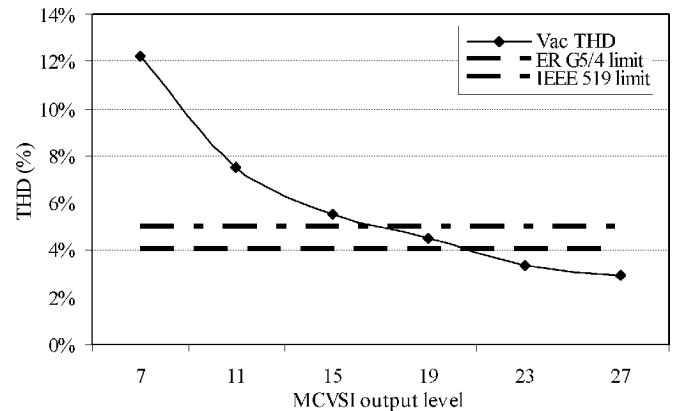


Fig. 3. THD for different MCVSI levels.

losses. Compared to others, the MCVSI topology has been adopted in this study because of its following features [8]:

- 1) a modular construction, allowing the use of large numbers of identical, mass-produced, high reliability modules and the possibility of a high degree of fault-tolerance;
- 2) fewer power semiconductor devices compared to the NPC and FC topologies;
- 3) no clamping diodes compared to the NPC topology;
- 4) fewer reservoir capacitors compared to the FC topology.

The numbers of active semiconductor switching devices, diodes and capacitors required by the three types of multilevel inverters are listed in Table I for a comparison purpose, where  $m$  is the number of levels in the synthesized output phase voltage.

## III. MCVSI HARMONIC DISTORTION

The dc link voltages of an MCVSI are often assumed to be constant and identical. With the standard switching scheme, the ac harmonic distortion depends on the voltage quantization level, hence a higher level MCVSI will always produce a less distorted output [17], [18]. Fig. 3 shows the total harmonic distortion (THD, % of fundamental) of the output phase voltage for different MCVSI levels,  $m$ . It is observed that, the harmonic distortion indeed reduces with increased level of cascading.

With finite dc link capacitance, the dc link voltages could contain a large second order harmonic of the fundamental output frequency. This depends on the load level and is the result of the switching function of each inverter module being modulated by the fundamental output current [19]. It can be shown that in such a case there is a mechanism that gives rise to additional, predominantly third order, harmonics in the output voltage of the inverter. These harmonics are of zero phase sequence. Due to the earthed neutral arrangement of the generator, shown in

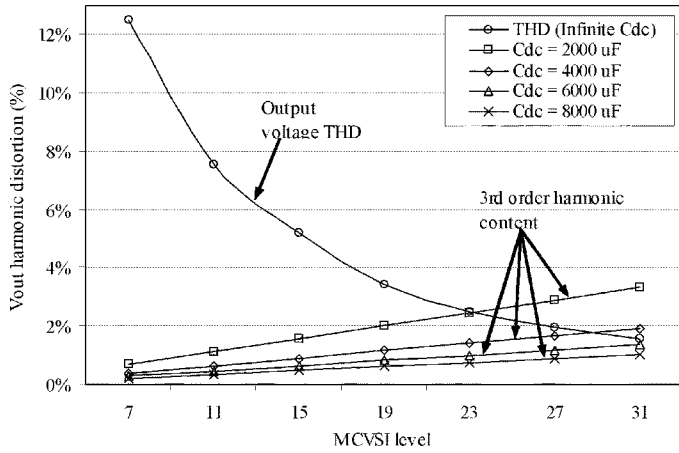


Fig. 4. MCVSI ac side harmonic distortion.

Fig. 1(c), such harmonics can cause detrimental effects in the system [20]. The second order harmonic current to be absorbed on the dc side of an inverter module is

$$i'_{dc}(2\omega_1 t) = i_{ac}(\omega_1 t)h_{sw}(\omega_1 t) \quad (2)$$

where  $i_{ac}(\omega_1 t)$  is the fundamental output current and  $h_{sw}(\omega_1 t)$  the fundamental component of the switching function associated with the H-bridge module concerned.

The inverter module's fundamental switching harmonic,  $h_{sw}(\omega_1 t)$ , will then modulate with the second order harmonic voltage of the dc link and transfer to the ac side as a third order harmonic voltage and consequently current

$$\begin{aligned} v_{ac}(3\omega_1 t) &= v'_{dc}(2\omega_1 t)h_{sw}(\omega_1 t) \\ &= i'_{dc}(2\omega_1 t)X_{dc}(2\omega_1)h_{sw}(\omega_1 t) \end{aligned} \quad (3)$$

where  $X_{dc}(2\omega_1)$  is the reactance of the dc link capacitor at the second order harmonic frequency. The resultant third order harmonic current is only limited by the zero sequence harmonic impedance in the output circuit, which is usually low.

In practice, complex modulating interactions occur in the system because the switching functions contain more than second order harmonics and the inverter output current is already distorted. As a result, a series of additional harmonics can be generated in the inverter output voltage. Obviously the interactions depend on the output load current of the inverter. If this is to be compensated by modifying the switching pattern of the inverter, the controller must work in closed loop as the operating point changes.

For the 1.8 MW system that is detailed later in the Section VI, Fig. 4 shows the simulated third order harmonic in the output voltage assuming that the system operates at full load. The change of THD with the number of voltage levels ( $m$ ) is shown in Fig. 5. Four different values of the dc link capacitance are compared. It is observed that the third order harmonic in the output voltage increases with the number of voltage levels and is always significant compared with the THD values previously shown in Fig. 3 for the ideal case. Although the dc link capacitance attenuates the adverse interaction, it is hardly possible

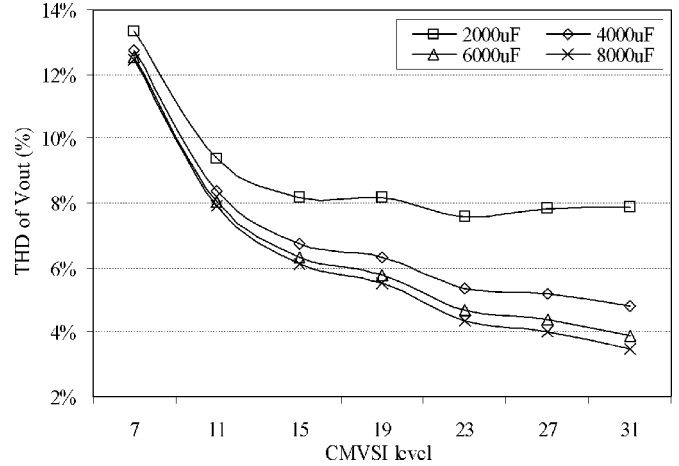


Fig. 5. Inverter output voltage THD.

to constrain the THD below 3% if the capacitance is less than 4000  $\mu$ F.

The capacitors can account for more than half of the total component cost of a power converter module. They also occupy a large footprint, making the modules larger than they need to be. Given the voltage rating in the application, the size and cost of the dc link capacitors are determined mainly by two factors: 1) the ripple current to be absorbed which determines the power losses in the capacitors and 2) the allowable ripple of the dc link voltage. Design experience in high power converter systems shows that the capacitors will be excessively large if the capacitance is selected to keep the dc link voltage ripple acceptably small for the purpose of avoiding the adverse modulating effect such as that analyzed above [21]. The switching strategy is therefore required to accept the non-constant dc link voltages.

#### IV. PROPOSED SWITCHING STRATEGY

The analysis above shows that the third order harmonic and other modulation products in the inverter output voltage caused by the non-constant dc link voltages will become a dominant issue when the number of the synthesized voltage levels increases. This will exceed the gain being made in terms of finer voltage quantization. The distortion can be reduced by using larger dc link capacitors but the drawback will be the increased cost and larger footprint. A new switching strategy is proposed to solve the problem, by means of which the harmonic distortion can be reduced without using costly and large capacitors.

##### A. Equalized Power Sharing

In addition to harmonic distortion, unequal electrical power distribution between cascaded modules has been a common problem for the conventional fundamental frequency switching MCVSI. Referring to Fig. 2, unequal duty cycle distribution causes some modules to be more heavily loaded than others. This reduces the utilization of the semiconductor devices and is against the concept of a modular design where it is desirable, from a fault-tolerant point of view, for all modules to be identical. Therefore, in spite of the fact that the dc link voltage balancing is no longer an issue because dc link voltages are independently provided by isolated coils and rectifiers,

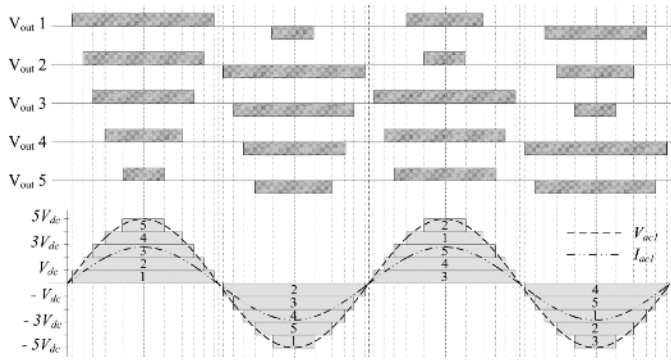


Fig. 6. Integral cycle switching scheme.

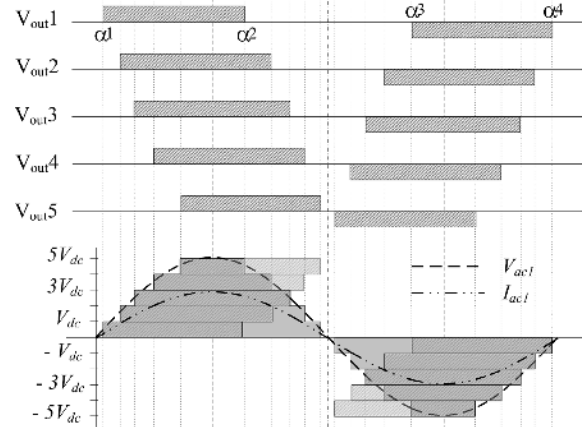


Fig. 8. Half cycle asymmetrical switching scheme.

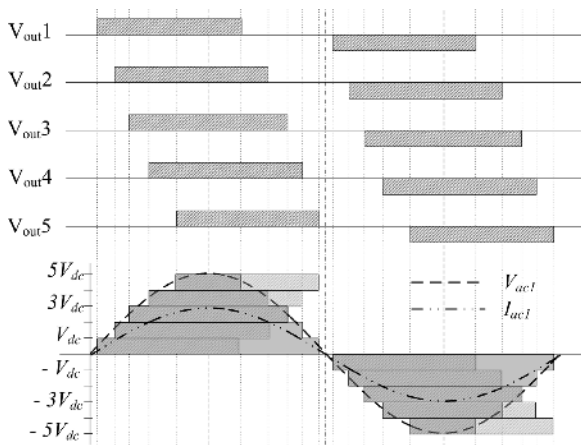


Fig. 7. Half cycle symmetrical switching scheme.

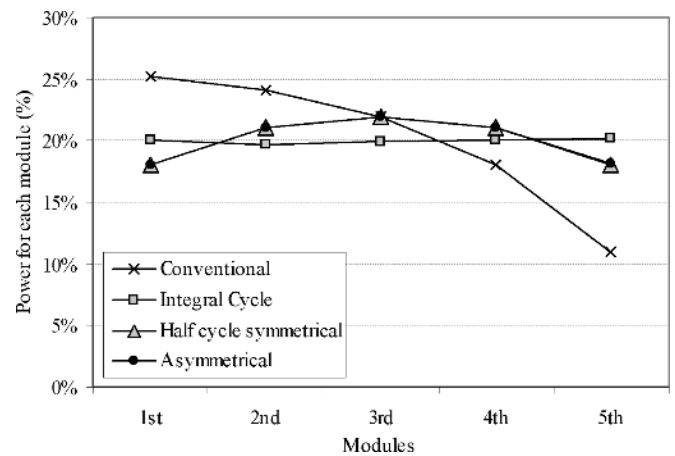


Fig. 9. 11-level MCVSI power sharing curve (unity power factor).

equalized power sharing between the inverter modules is still a desirable feature for the system being developed.

F. Z. Peng *et al.* [22], [23] suggested an integral cycle switching scheme as illustrated in Fig. 6, for the MCVSI to balance the power sharing between the modules.

This switching scheme gives a very balanced average power sharing between all the modules, to be shown later in Fig. 10. However, in reality, an inter-cycle difference of power still exists in each module. It can be shown that depending on the output phase voltage level ‘*m*’, such a half cycle rotating switching scheme causes significant low order harmonics, predominantly at frequency of  $2(m - 1)$  Hz, in the output voltage of the multilevel inverter if the dc link capacitance is insufficient.

The half cycle symmetrical switching scheme is shown in Fig. 7. The switching functions of all the modules are of the same width but phase shifted in order to synthesize the output waveform. For the same output current flowing through all the modules, the power factor with respect to the individual fundamental output voltage is different from one module to another. As a result, the real power varies, with the modules in the centre taking more power than the modules on the top or bottom of the cascaded phase if the overall output power factor is unity. In this case, the pattern of real power sharing changes with the overall output power factor, as to be shown later.

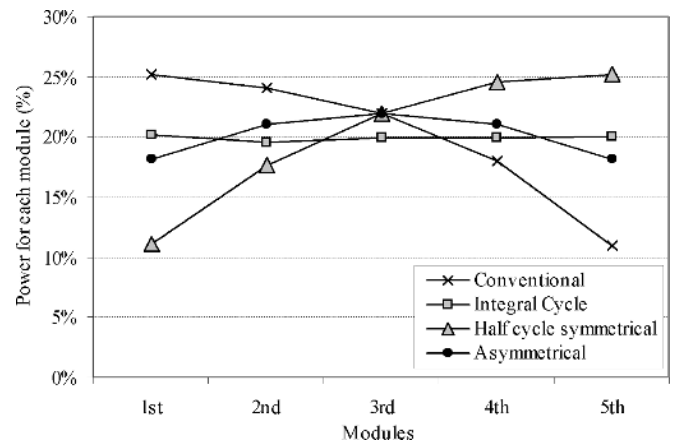


Fig. 10. 11-level MCVSI power sharing (injecting reactive power, power factor: 0.81).

To correct this, an improved switching strategy is shown in Fig. 8. Similar to other switching schemes, the switching function of each module is defined by four phase angles which are determined trigonometrically as follows:

$$\alpha_{1-(i)} = \frac{[\sin^{-1}(\frac{i}{M}) - \alpha_{1-(i-1)}]}{2 + \alpha_{1-(i-1)}} \quad (4)$$

$$\alpha_{2-(i)} = \pi - \alpha_{1-(M+1-i)} \quad (5)$$

TABLE II  
SWITCHING ANGLES OF ASYMMETRICAL SCHEME

| Firing angle ( $\alpha_1, \alpha_2$ ) | $\alpha_1$ (in degree) |       |       |       |       | $\alpha_2$ (in degree) |        |        |        |        |
|---------------------------------------|------------------------|-------|-------|-------|-------|------------------------|--------|--------|--------|--------|
|                                       | 5                      | 7     | 9     | 11    | 13    | 5                      | 7      | 9      | 11     | 13     |
| Number of Module                      |                        |       |       |       |       |                        |        |        |        |        |
| VSI #1                                | 5.52                   | 4.02  | 3.15  | 2.59  | 2.19  | 108.43                 | 105.50 | 103.63 | 102.31 | 101.31 |
| VSI #2                                | 17.56                  | 12.41 | 9.61  | 7.85  | 6.63  | 135.00                 | 127.71 | 123.10 | 119.86 | 117.41 |
| VSI #3                                | 30.22                  | 20.99 | 16.16 | 13.15 | 11.10 | 149.78                 | 139.78 | 133.57 | 129.22 | 125.96 |
| VSI #4                                | 45.00                  | 30.11 | 22.93 | 18.58 | 15.63 | 162.44                 | 149.89 | 142.22 | 136.91 | 132.95 |
| VSI #5                                | 71.57                  | 40.22 | 30.07 | 24.18 | 20.27 | 174.48                 | 159.01 | 149.93 | 143.71 | 139.10 |
| VSI #6                                | x                      | 52.29 | 37.78 | 30.05 | 25.05 | x                      | 167.59 | 157.07 | 149.95 | 144.72 |
| VSI #7                                | x                      | 74.50 | 46.43 | 36.29 | 30.03 | x                      | 175.98 | 163.84 | 155.82 | 149.97 |
| VSI #8                                | x                      | x     | 56.90 | 43.09 | 35.28 | x                      | x      | 170.39 | 161.42 | 154.95 |
| VSI #9                                | x                      | x     | 76.37 | 50.78 | 40.90 | x                      | x      | 176.85 | 166.85 | 159.73 |
| VSI #10                               | x                      | x     | x     | 60.14 | 47.05 | x                      | x      | x      | 172.15 | 164.37 |
| VSI #11                               | x                      | x     | x     | 77.69 | 54.04 | x                      | x      | x      | 177.41 | 168.90 |
| VSI #12                               | x                      | x     | x     | x     | 62.59 | x                      | x      | x      | x      | 173.37 |
| VSI #13                               | x                      | x     | x     | x     | 78.69 | x                      | x      | x      | x      | 177.81 |

| Firing angle ( $\alpha_3, \alpha_4$ ) | $\alpha_3$ (in degree) |        |        |        |        | $\alpha_4$ (in degree) |        |        |        |        |
|---------------------------------------|------------------------|--------|--------|--------|--------|------------------------|--------|--------|--------|--------|
|                                       | 5                      | 7      | 9      | 11     | 13     | 5                      | 7      | 9      | 11     | 13     |
| Number of Module                      |                        |        |        |        |        |                        |        |        |        |        |
| VSI #1                                | 251.57                 | 254.50 | 256.37 | 257.69 | 258.69 | 354.48                 | 355.98 | 356.85 | 357.41 | 357.81 |
| VSI #2                                | 225.00                 | 232.29 | 236.90 | 240.14 | 242.59 | 342.44                 | 347.59 | 350.39 | 352.15 | 353.37 |
| VSI #3                                | 210.22                 | 220.22 | 226.43 | 230.78 | 234.04 | 329.78                 | 339.01 | 343.84 | 346.85 | 348.90 |
| VSI #4                                | 197.56                 | 210.11 | 217.78 | 223.09 | 227.05 | 315.00                 | 329.89 | 337.07 | 341.42 | 344.37 |
| VSI #5                                | 185.52                 | 200.99 | 210.07 | 216.29 | 220.90 | 288.43                 | 319.78 | 329.93 | 335.82 | 339.73 |
| VSI #6                                | x                      | 192.41 | 202.93 | 210.05 | 215.28 | x                      | 307.71 | 322.22 | 329.95 | 334.95 |
| VSI #7                                | x                      | 184.02 | 196.16 | 204.18 | 210.03 | x                      | 285.50 | 313.57 | 323.71 | 329.97 |
| VSI #8                                | x                      | x      | 189.61 | 198.58 | 205.05 | x                      | x      | 303.10 | 316.91 | 324.72 |
| VSI #9                                | x                      | x      | 183.15 | 193.15 | 200.27 | x                      | x      | 283.63 | 309.22 | 319.10 |
| VSI #10                               | x                      | x      | x      | 187.85 | 195.63 | x                      | x      | x      | 299.86 | 312.95 |
| VSI #11                               | x                      | x      | x      | 182.59 | 191.10 | x                      | x      | x      | 282.31 | 305.96 |
| VSI #12                               | x                      | x      | x      | x      | 186.63 | x                      | x      | x      | x      | 297.41 |
| VSI #13                               | x                      | x      | x      | x      | 182.19 | x                      | x      | x      | x      | 281.31 |

$$\alpha_{3-(i)} = 2\pi - \alpha_{2-(i)} \tag{6}$$

$$\alpha_{4-(i)} = 2\pi - \alpha_{1-(i)} \tag{7}$$

where  $i = 1, \dots, M$  denote the module number in the order as shown in Fig. 8. It is assumed that  $\alpha_{1(0)} = 0$ .

This switching scheme is termed asymmetrical because the switching function waveform is neither even nor half wave symmetrical. It is found that the fundamental components of all the switching functions are of similar amplitudes and in phase with each other. Consequently real power sharing between the modules is insensitive to the output power factor and is pre-determined.

For different number of modules, the switching angles can be readily calculated and some results are shown in Table II, starting from five modules converter.

Simulation results for the power sharing in an 11-level (five modules per phase) MCVSI with four different switching schemes including the three described in this section and the standard one previously described in Fig. 2, are compared in Fig. 9. The effect of reactive power demand on the different switching schemes is shown in Figs. 10 and 11. The integral cycle switching scheme was not adopted because of its generation of low frequency harmonics due to inter-cycle variation. The simulation results indicate that, apart from integral cycle scheme, the asymmetrical half cycle switching scheme gives a relatively good and consistent power sharing profile, which is insensitive to the output real and reactive power demand. Fig. 12 shows the power variation comparison for different levels of MCVSI when the proposed asymmetrical switching

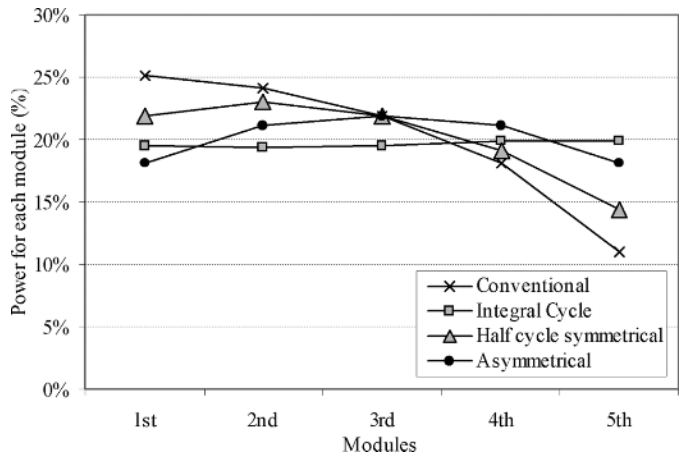


Fig. 11. 11-level MCVSI power sharing (absorbing reactive power, power factor: 0.86).

strategy and conventional fundamental frequency switching strategy are used. It is clear that the percentage difference, with respect to the average module power, decreases with higher level MCVSI. The advantage of the proposed equal power sharing scheme is most conspicuous on configurations with fewer levels. This could occur when some of the modules have failed during fault tolerant operation.

### B. Harmonic Compensation

As demonstrated in Section III, the use of a fundamental frequency switching scheme at each module causes third order etc.

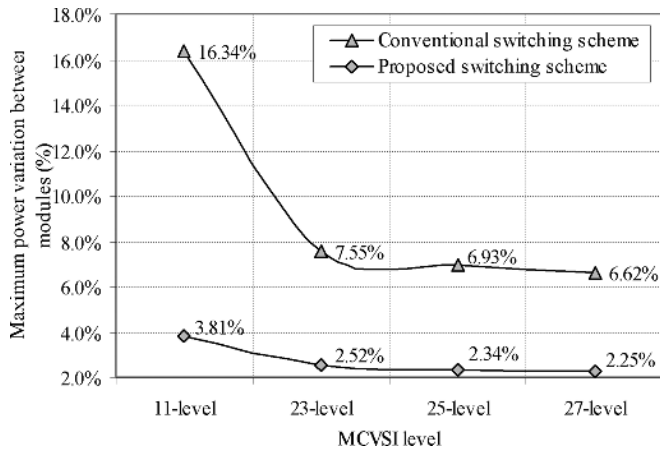


Fig. 12. Maximum power variation between modules with different MCVSI levels.

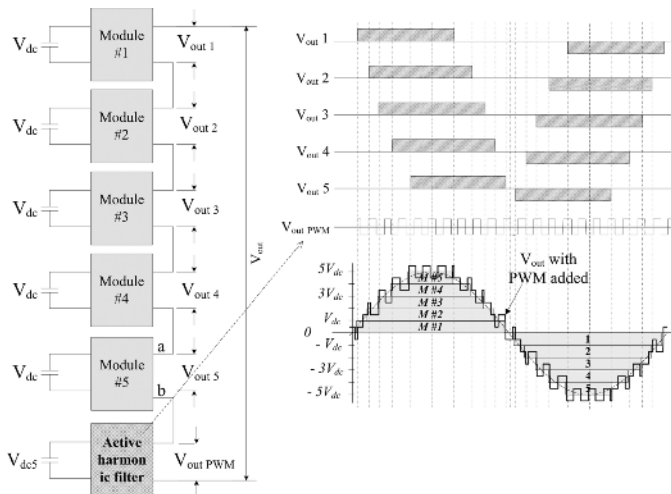


Fig. 13. Conventional hybrid MCVSI (PWM active harmonic filter added).

harmonics on the output ac side of the MCVSI. The switching strategy for equal power sharing affects the amplitudes of the harmonics but would not remove the mechanism by which the harmonics are generated. In a transformer-less configuration, harmonic filters would be required to suppress these harmonics. An active harmonic filter may be more suitable as the harmonic contents are close to the fundamental frequency. The use of a passive filter would increase the risk of resonance.

A hybrid MCVSI, incorporating an active harmonic filter cascaded with other modules of the MCVSI, as shown in Fig. 13, could be used to eliminate the ac side harmonic distortion. However, an active filter module, which operates at higher switching frequency ( $f_{sw}$ ), causes higher switching losses and results in higher electrical stresses leading to higher failure rate. It is worst in the situation where high level ac side harmonic distortion is required to be filtered out. Failure of the active filter module will have serious consequences as the entire system has to be shut down for repair and replacement, defeating the objective of a modular design.

An improved equal power sharing MCVSI switching strategy has been developed in this study. The proposed switching strategy integrates the active harmonic filtering action into the

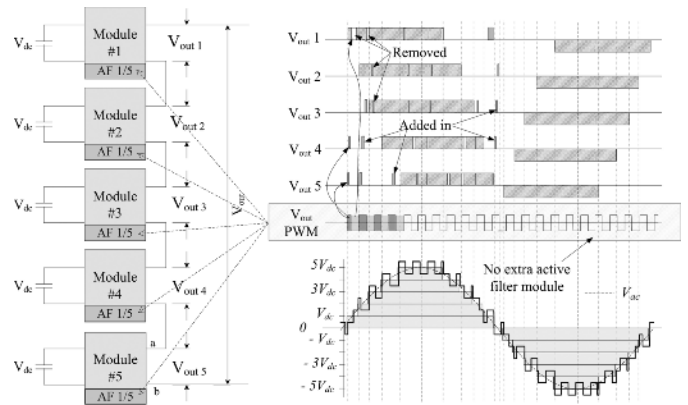


Fig. 14. Block diagram of the proposed MCVSI and its switching waveforms.

ordinary MCVSI modules that would otherwise operate at the fundamental frequency, as shown in the Fig. 8. In such integration, all modules in the same phase share the load real power as well as the switching burden/losses for active filtering. The concept of the proposed switching strategy is shown in Fig. 14.

In such a way, no dedicated module is required for harmonic filtering as the duty of active filter is shared by all modules in the same output phase. A set of three-level PWM carrier signals with frequency  $2f_{sw}(m-1)^{-1}$  and consecutive phase shifts by an increment of  $4\pi(m-1)^{-1}$  will be assigned to each of the modules, where  $f_{sw}$  is the overall switching frequency of the active filter and  $m$  is the number of the output voltage levels. An error signal generated by the control loop, which responds to the distortion of the output phase voltage, is used as the common reference to all the modules to compare with the phase shifted carrier signals, which determines the extra switching action required to compensate the harmonic distortion. Referring to the generalized control waveforms shown in Fig. 15, if a module is in “ON” state, i.e., outputting a positive or negative dc link voltage, additional “notches” can be caused to reduce the average output voltage in the corresponding direction. Similarly if the module is in “OFF” state, i.e., ideally outputting 0 V, additional pulses can be produced in the appropriate direction to modify the overall output voltage. As a result, the effect of the dc link voltage variation is compensated by the additional pulse width modulation. In general the required compensation to the output voltage is relatively small, additional “notches” or “pulses” are also small and have little impact on the power sharing objective that is achieved by the basic fundamental frequency switching function previously described. Since the active filtering duty is shared by all the modules, the increase of switching frequency is only marginal.

## V. EXPERIMENTAL VALIDATION

The proposed control concept has been experimentally evaluated on a relatively small scale laboratory test rig as shown in Fig. 16(a), with block diagram shown in Fig. 17.

Each converter module consists of a power board and a local control board as shown in Fig. 16(b). The power board includes the active and passive elements for two rectifiers, one H-bridge inverter, the dc link, and some measuring and protecting elements. TMS320F2808 DSP is the core of the control board



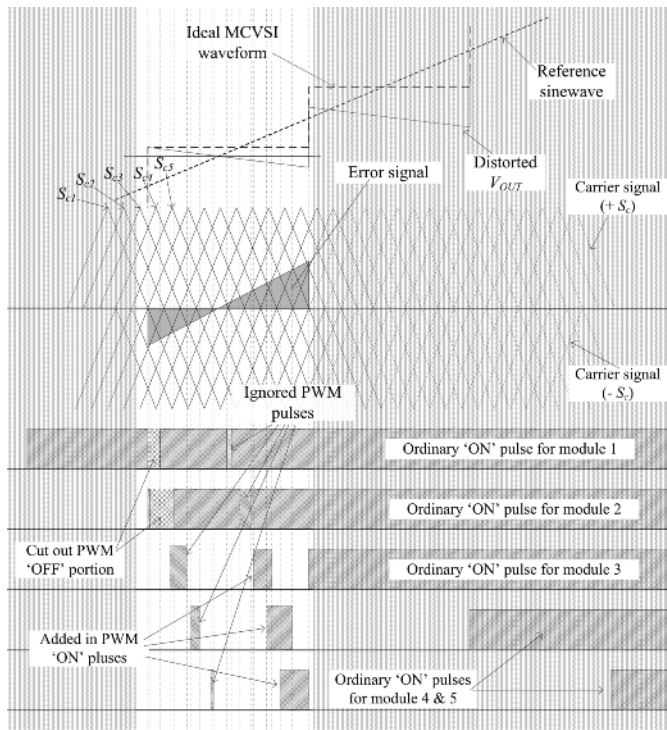


Fig. 15. Generalized graphical presentation of the proposed control algorithm.

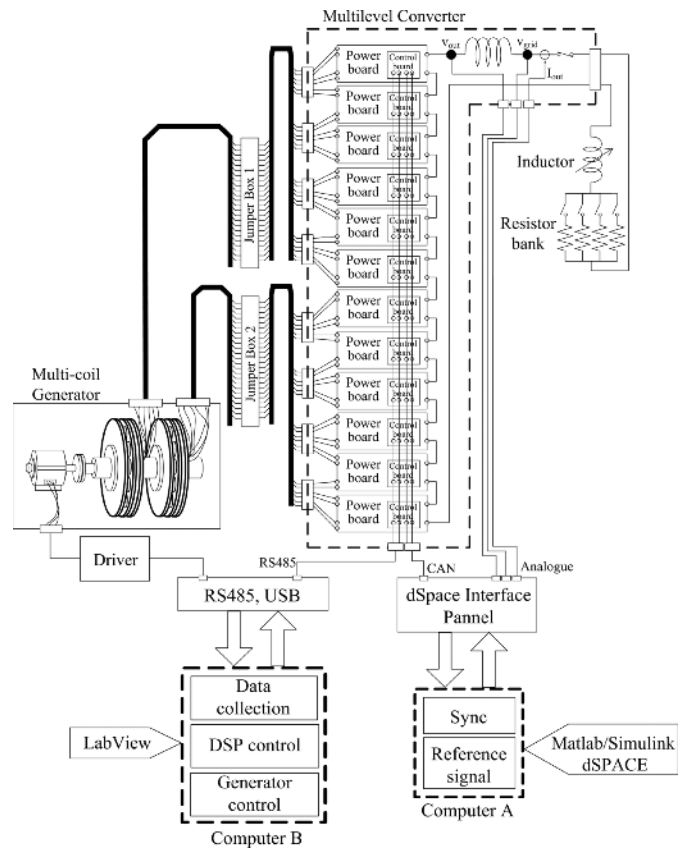


Fig. 17. Block diagram of laboratory test rig.

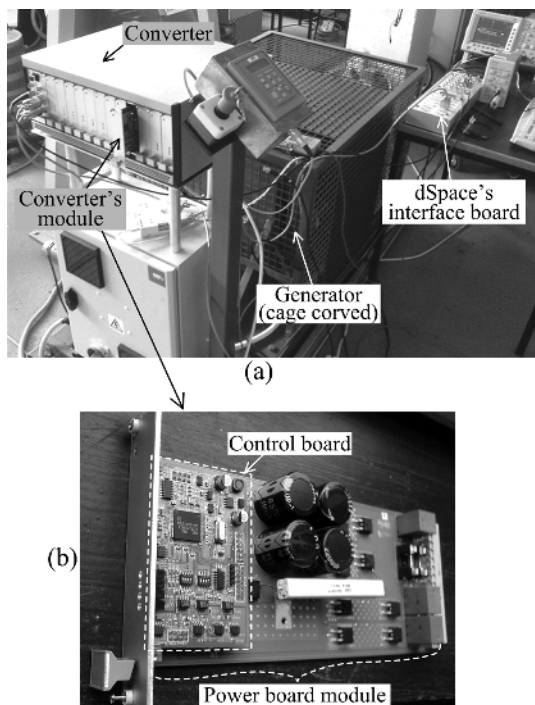


Fig. 16. (a) Experimental setup (2.5 kW, 230 V) and (b) converter's module.

which generates the gating signals for the rectifiers and inverter. The control board also provides monitoring and communication functions. A DS1103 dSpace real time control system, which can be programmed in the Matlab/Simulink environment, is the high level master controller which communicates to the 12 converter modules via a CAN bus. The main function of the dSpace

controller is to ensure the synchronization of all modules, to control the harmonic compensation and to control the output real and reactive power. CAN communication, which is based on the series communication protocol, has been implemented in order to minimize the data connections between individual modules and the master controller unit with deterministic time delay ( $< 200 \mu s$ ) which can be compensated through close loop control for the output power. The feature of CAN allows a single central controller to communicate with multiple modules, 12 in this case, that are connected in series along the CAN network with only a single two-way twisted pair cable. In addition, the advantages in terms of noise rejection and data transferring speed also encouraged the use of CAN in the prototype. The wind turbine is emulated using a multi-coils axial flux permanent magnet generator driven by an induction motor in torque control.

The proposed power sharing control scheme is tested under various output power factor conditions. Fig. 18 shows the per-phase output voltage and current for  $PF = 1$  and  $PF = 0.55$ , respectively. Power sharing profiles of the conventional fundamental frequency switching scheme and the proposed switching scheme, at different power factors, are shown in Fig. 19. It is shown that, in agreement with the simulation result, the proposed switching scheme gives much better power sharing characteristics compared to the conventional switching scheme.

Figs. 20 and 21 show the inverter output voltage, its harmonic spectrum and the control error signal before and after implementing the harmonic compensation scheme that was described

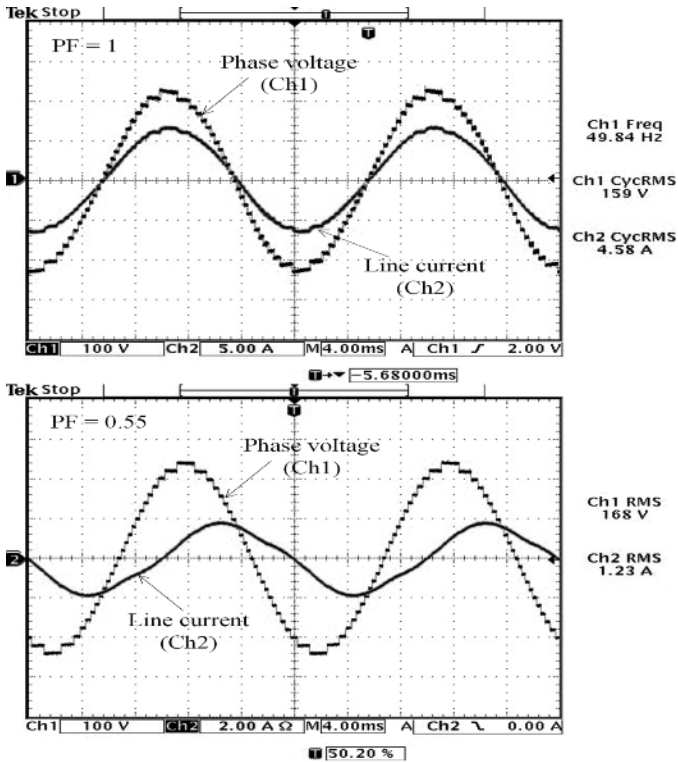


Fig. 18. Inverter output voltage and current.

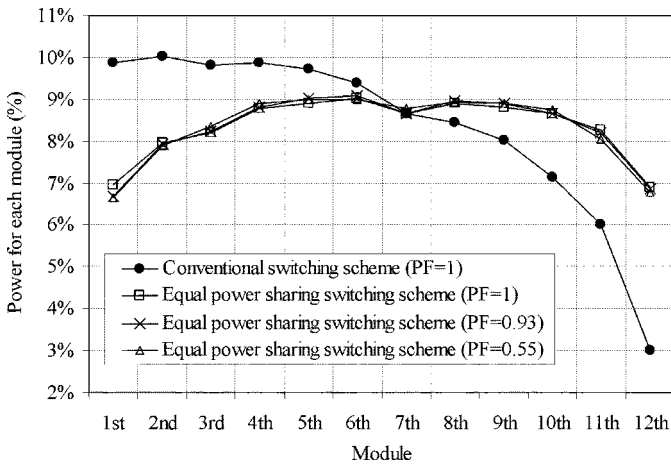


Fig. 19. Power sharing profile of a 25-level multilevel inverter, with different switching schemes and power factors.

in the previous section. It is observed that the proposed compensation scheme has significantly reduced the dominant third order harmonic (150 Hz) voltage, from 2.34 V to 0.58 V. PWM switching effects can be seen in the output phase voltage. Although the experiment was carried out on a system that had been significantly scaled down, it serves the purpose to verify the control algorithm. Further simulations are carried out in the next section to evaluate the proposed concept and the obtained conclusion on a 1.8 MW system.

### VI. HARMONIC ANALYSIS OF FULL SCALE SYSTEM

The additional simulation is based on a multi-coil PM generator supplying power into an 11 kV 3 phase system without

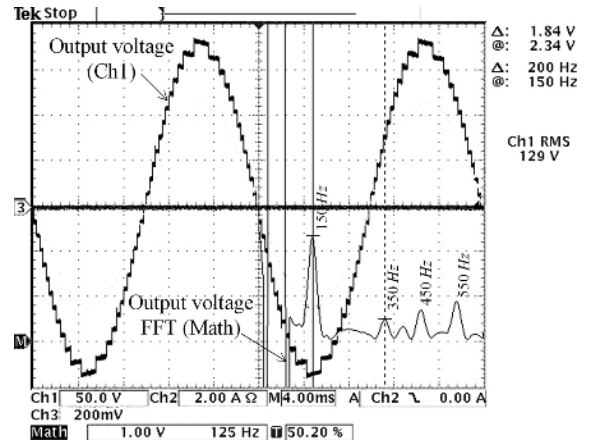


Fig. 20. Output voltage and its spectrum without harmonic compensation.

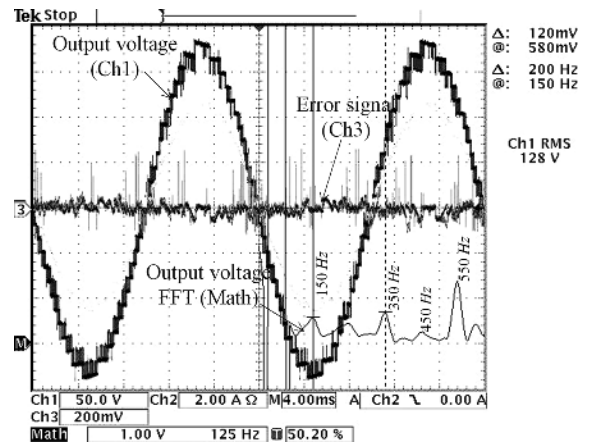


Fig. 21. Output voltage, its spectrum and error signal for harmonic compensation.

TABLE III  
FULL-SCALE SIMULATION SETUP PARAMETERS

|                            |                        |
|----------------------------|------------------------|
| Generator                  | 72 coils               |
| Rated inverter voltage     | 11 kV, 50 Hz, 3 phases |
| MCVSI level                | 25-level per phase     |
| Rated power                | 1.8 MW @ PF = 1        |
| Grid coupling impedance    | 0.5 + j4.71 Ω          |
| D.c. link capacitor        | 2200 μF – 8800 μF      |
| Module switching frequency | 50 Hz – 600 Hz         |

the use of step-up transformer. The parameters of the full-scale set up are listed in Table III. An MCVSI was used to set up the output voltage and control the power delivery. Pairs of active rectifiers are configured in such a way as to eliminate the low order harmonic components on the dc side of each module.

Figs. 22 and 23 show the output phase voltage and line current of the fundamental switching MCVSI with two dc link capacitance values. The effect of limited dc link capacitance is clearly seen. The harmonic distortion levels of these waveforms are compared later in Fig. 29.

In order to ensure the stability of feedback control on the output power, it is necessary to limit the output harmonic currents, mainly the third order harmonic. As a result, low dc link capacitance values should be avoided. 3800 μF is the minimum

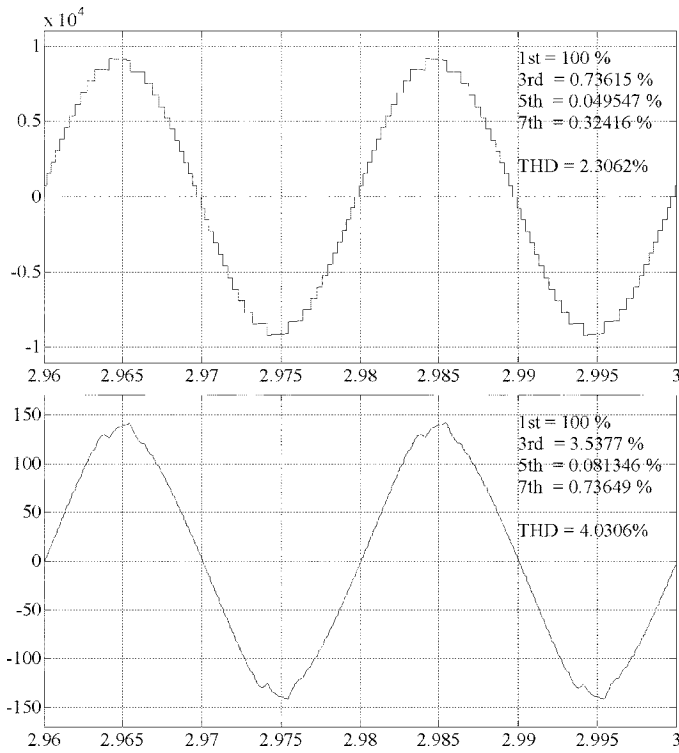


Fig. 22. Output phase voltage and line current of 25-level MCVSI with 8800  $\mu\text{F}$   $C_{dc}$ .

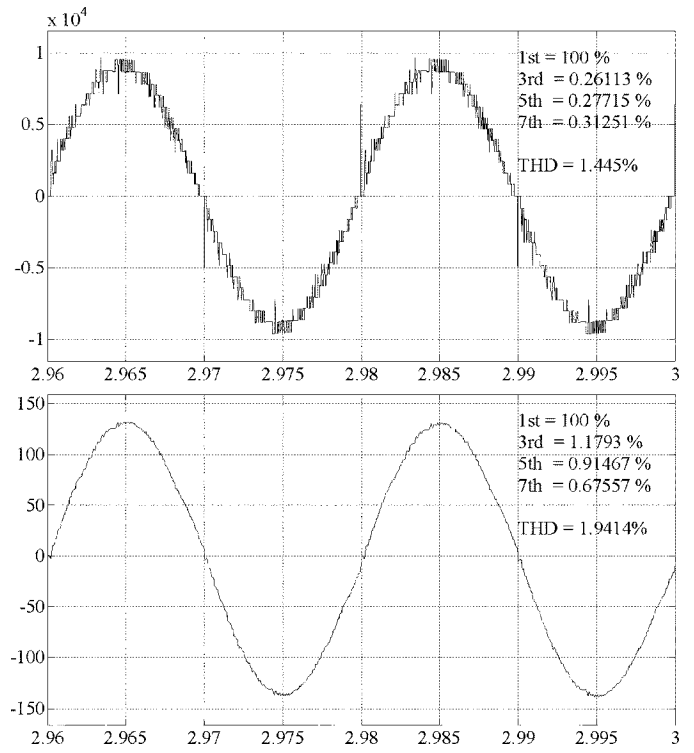


Fig. 24. Output phase voltage and line current of the proposed 25-level Hybrid-MCVSI with 8800  $\mu\text{F}$   $C_{dc}$ .

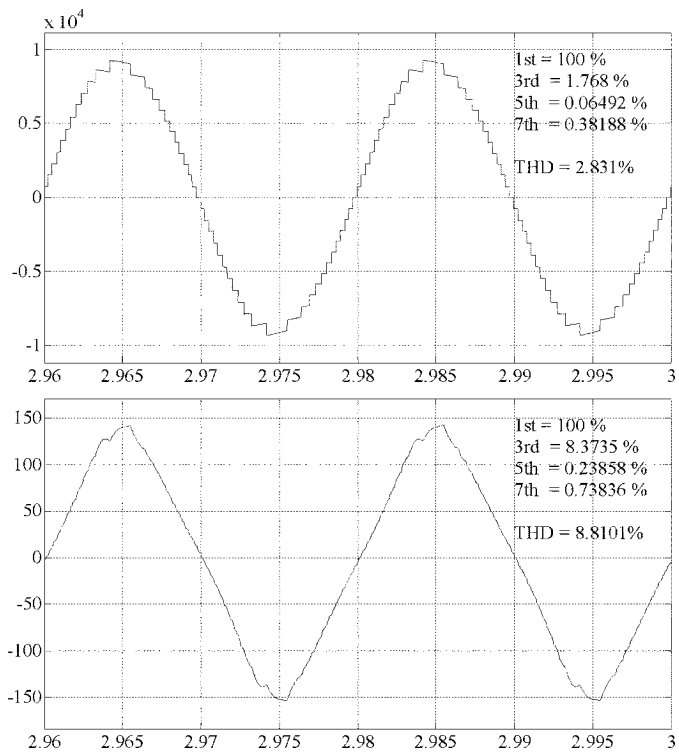


Fig. 23. Output phase voltage and line current of the 25-level MCVSI with 3800  $\mu\text{F}$   $C_{dc}$ .

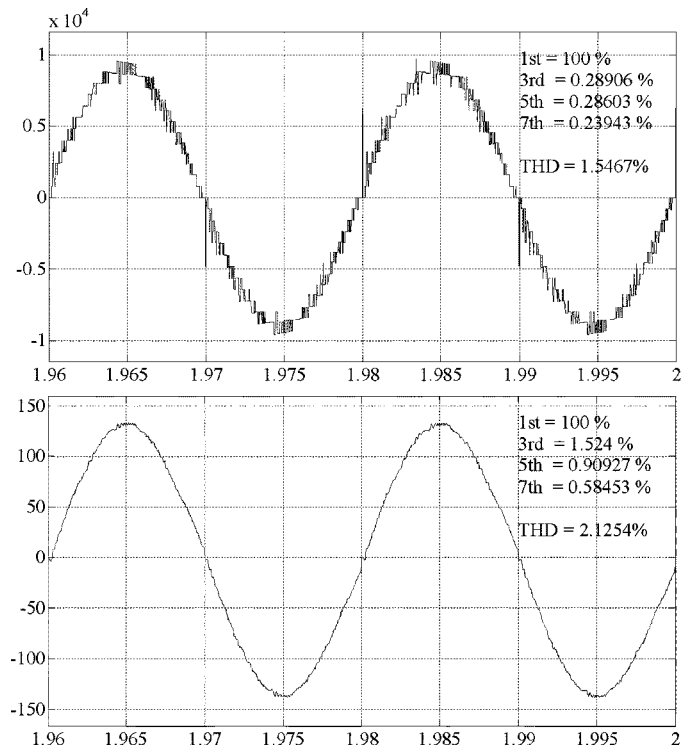


Fig. 25. Output phase voltage and line current of the proposed 25-level Hybrid-MCVSI with 3800  $\mu\text{F}$   $C_{dc}$ .

for the conventionally switched MCVSI. As indicated in Fig. 23, approximately 9% third order harmonic was generated.

Figs. 24 and 25 show the output phase voltage and the line current of the proposed 25-level MCVSI (with the same capac-

itance values as in the previous simulation). With the proposed inverter switching scheme, the ac side harmonic content produced by the inverter has been significantly reduced. Referring to Fig. 26, a reduction of the third order harmonic component

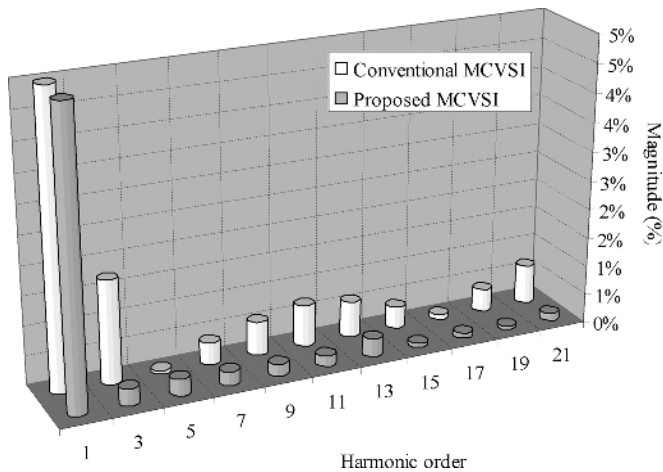


Fig. 26. Comparison between conventional and the proposed MCVSI output harmonic content (based on  $C_{dc} = 3800 \mu\text{F}$ ).

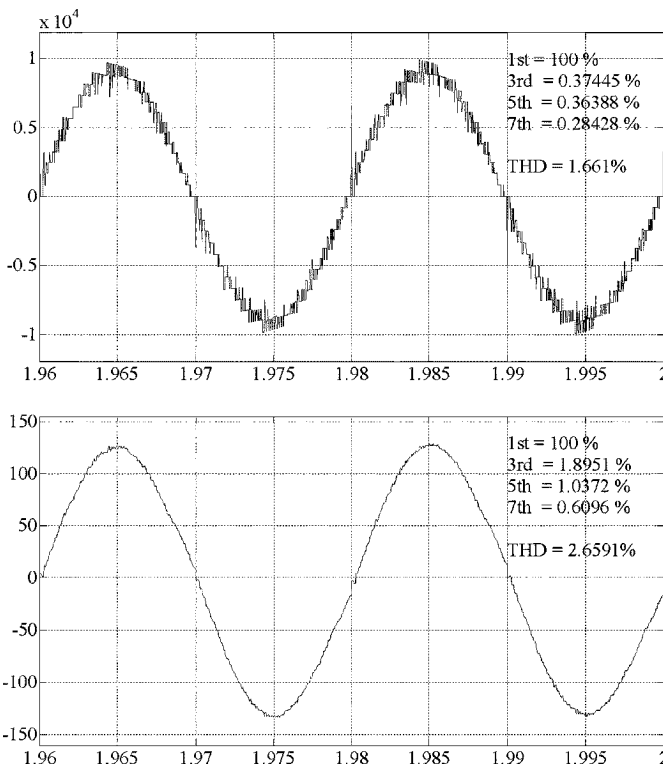


Fig. 27. Output phase voltage and line current of the proposed 25-level Hybrid-MCVSI with  $2200 \mu\text{F}$   $C_{dc}$ .

by over 80% has been obtained. The same figure shows that the overall harmonic distortion index has been significantly improved. As a result, the dc link capacitors can be further reduced to save the cost, as long as the ripple current rating is not exceeded. In this simulation, the dc link capacitance was further reduced to  $2200 \mu\text{F}$  to demonstrate the performance of the proposed switching scheme. The output voltage and line current produced by inverter with this capacitance are shown in Fig. 27. As previously mentioned, the proposed MCVSI control scheme stops harmonic current flow being modulated between the dc and ac sides of the MCVSI. DC link voltage from one of the modules of the 25-level MCVSI modules is shown in Fig. 28.

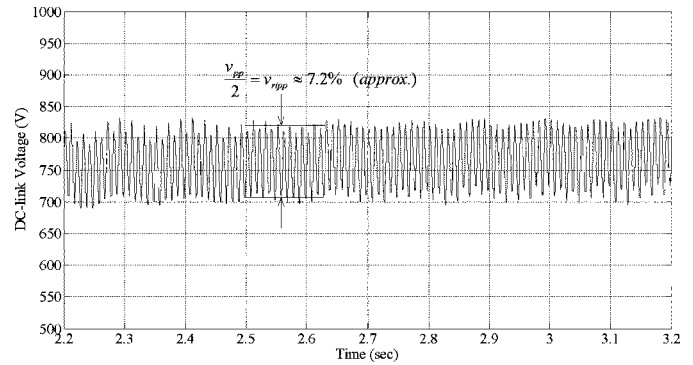


Fig. 28. DC link voltage of the middle module of the proposed 25-level Hybrid-MCVSI ( $C_{dc} = 2200 \mu\text{F}$ ).

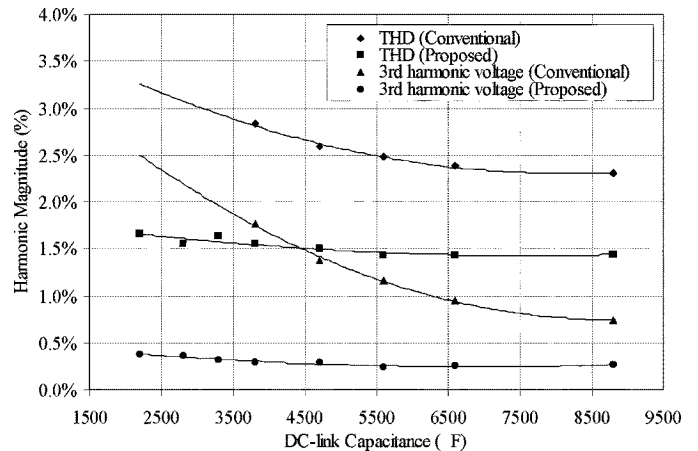


Fig. 29. THD and third order harmonic voltage of the conventional and proposed MCVSI with various dc link capacitance values.

Approximately 7.2% voltage ripple is present when such a low capacitance is used. With the proposed switching scheme, despite the presence of high-level dc link harmonics, a clean output voltage could always be produced.

The THD of the inverter output voltage and the third order harmonic voltage based on various dc link capacitances are contrasted graphically in Fig. 29. The graph shows the improvement brought about by the proposed MCVSI switching scheme. Fig. 30 shows the power sharing profiles of the conventional and proposed MCVSI. The proposed switching strategy maintains the inter-modules power variation within 2.5% for a 25-level MCVSI, while 11.5% power variation is observed with the conventionally switched MCVSI.

## VII. CONCLUSION

This paper describes a modular power electronics solution for a transformer-less wind energy conversion system, which could deliver lower cost, high reliability, fault-tolerance for lightweight, direct drive air-cored or iron-cored slotless generators for large wind turbines. The features and application of the multilevel cascaded voltage source inverter are analyzed in this paper. The requirement of equalized power sharing between levels has been identified and resolved using a new switching strategy which also compensates the inherent harmonic interaction in the converter system.

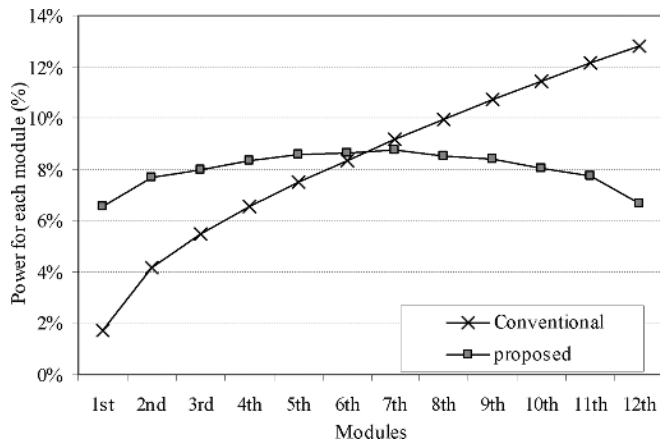


Fig. 30. Power sharing profiles of the conventional and proposed switched MCVSI.

Three-phase star connection of the converter modules is possible to emulate a synchronous generator for protection purposes. Increasing the dc link capacitance of each converter module could improve the harmonic performance, but capacitors are costly and often come with relatively large physical sizes. The proposed switching scheme combines the fundamental frequency and multilevel PWM switching strategies. By equally distributing the PWM duties to all the modules of the MCVSI, high switching stresses are avoided. This is made possible by the low frequency phase shifted PWM duty cycles synthesized in each module, resulting in a high overall switching frequency viewed at the output of the inverter, which is sufficient to perform overall harmonic elimination. Simulations and experiments are carried out to evaluate the performance of the proposed technique, and the results are promising.

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