A MULTIPHASE SERIES-RESONANT CONVERTER WITH A REDUCED NUMBER OF THYRISTORS AND COMMON GROUNDS FOR INPUTS AND OUTPUTS

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Abstract. Multiphase series-resonant (SR) power converters provide a flexible way to transform power between a utility grid and a multiphase load or source. The current implementations all suffer from a high component count, which makes the use of these converters unattractive from an economical point of view.

A new topology for multiphase SR converters has been proposed in [1] in a simulation context. This topology uses half the number of power semiconductors compared to the existing multiphase SR converters.

The present paper addresses the implementation of the new topology in a prototype converter. Simulation data and measured waveforms are shown, and a comparison is made between the new and the existing topologies. It is shown that the economical gain due to the reduction in component count is offset by a lower power rating.

Keywords. Power electronics; control systems; inverters; series resonant converters; three-phase; AC-to-AC power converter; reversible power flow; thyristors; reactive power generation.

1 Introduction

Series-resonant (SR) techniques have been used for a long time to attain low switching losses in DC-DC power converters. The low switching losses make it possible to use high switching frequencies while keeping, at the same time, the conversion efficiency high. During the last decade the use of series-resonant (SR) techniques has spread out into the field of multiphase applications [2, 3, 5, 6]. The converters which have been presented in the literature feature several interesting properties, including:

- Smooth input- and output voltages and - currents,

- adjustable power factor at the input of the converter, including unity,

- absence of low-frequency filters, thus reducing weight,

- common grounds for inputs and outputs, thus reducing high-frequency interference, and facilitating 'clean' measurements,

- easy parallel operation of multiple modules, and

- expandability to any number of inputs or outputs.

In these applications one resonant L-C tank is time-shared between the input- and output terminals of the converter. The topology of the power circuit which is often used makes it necessary to connect both sides of the resonant tank to the terminals of the converter. For AC operation, we need to achieve current flow in two directions, and therefore the number of semiconductor switches needed for multiphase AC applications equals four times the total number of terminals. For a three-phase to three-phase converter 24 switches would be needed. Clearly, this number compares badly to the number of active devices which is needed to build a PWM bridge.

In this paper we will present a modified multiphase series-resonant converter topology, in which only one side of the resonant circuit can, by means of a switch matrix, be connected to the input- and output terminals of the converter. The other side of the resonant tank is connected to a common neutral. The number of active semiconductors (SCR thyristors in our case) in this topology reduces to 12, which clearly is an advantage as compared to the 24-thyristor alternative.

2 Circuit topologies

The 'new' circuit topology can be thought to be derived from the 'classic' topology which has been presented in [5, 4]. Simplified schematics of both the 'old' and the new power circuit topology have been depicted in figure 1.

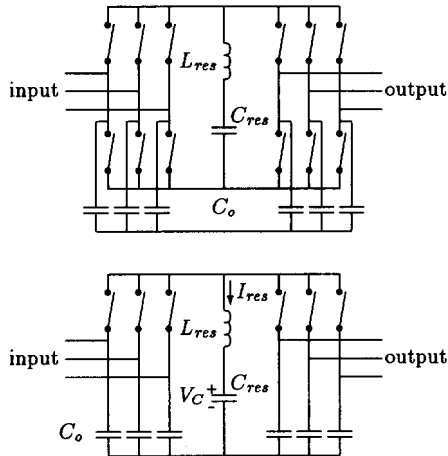In figure 1 every switch represents the combination of two antiparallel thyristors and their snubber circuits.

Fig. 1: Topologies of two power circuits
a: (upper) The 'old' circuit
b: (lower) The new circuit

Fig. 2: Signal shapes for one resonant sine wave
a: (upper) I_{res}: Current through L_{res}
b: (middle) V_C: Voltage across C_{res}
c: (lower) I_{res} vs. V_C

The operation of the circuit in figure 1a has been verified in [5, 6, 4, 7]. A slightly different version of the circuit in figure 1b has been presented in a simulation context in [1].

3 Operation during one resonant pulse

3.1 State-plane description

The operation of the power circuit of figure 1b is most easily demonstrated starting from the situation where the voltage across the resonant capacitor (V_C) is at its maximum value. We will assume that the magnitude of this peak capacitor voltage is larger than any of the input- or output voltages. Furthermore we will assume that the value of the filter capacitors (C_o) is much larger than the value of C_{res}, which implies that the source and load of the converter can be modeled as ideal voltage sources.

Current flow in the circuit starts with the closing of one of the six switches. With the assumptions above, the direction of the resonant current is dictated by the sign of V_C, i.e. I_{res} will become positive if V_C was negative and vice versa. For brevity, we will only consider the case of a negative initial value for V_C in the following. The case for positive V_C can be treated in a completely analogous way.

Without further intervention, the resonant current I_{res} will develop as a positive sinewave. At the moment this current becomes zero again, the thyristor switch will turn off, and V_C will have been mirrored in the voltage of the terminal whose switch has been closed.

Figures 2 a) and b) show the development of the resonant current (I_{res}) and capacitor voltage (V_C) against time. When these two variables are plotted against
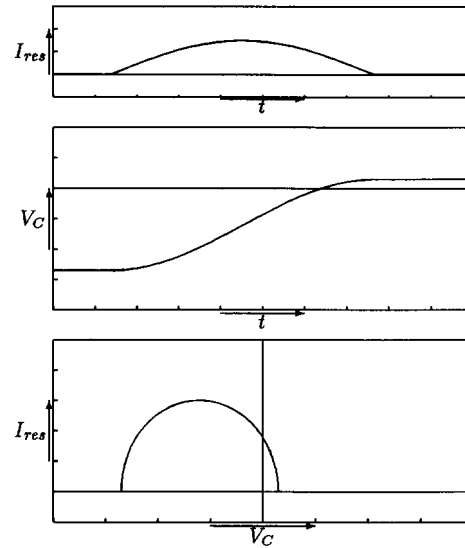
each other in the so-called state-plane [8] the trajectory shows up as an ellipse, or, with proper scaling, as a circle. This circle has been depicted in fig. 2c. The centre of this circle is located at $(V_{LC}, 0)$, where V_{LC} indicates the voltage applied to the resonant circuit. Geometrically the "mirroring" of the capacitor voltage in V_{LC} is quite obvious.

3.2 Energy considerations

For continuous operation of a multiphase resonant converter, it has been argued in [6] and [7] that V_C should be exactly inverted after every resonant half cycle. In this way it is guaranteed that the initial conditions for the next resonant half cycle are (apart from a trivial inversion) identical to those of the cycle which has just been finished.

If the capacitor voltage is exactly inverted after every resonant half cycle, the net energy supplied to the resonant circuit needs to be zero. This implies that we need to apply two voltages of opposite polarity in sequence to the resonant circuit. The reader may want to compare this need to the situation in the well-known buck-boost converter, where two voltage polarities are used to constrain the energy in the main inductance.

A proper choice of the moment of turnover (t_1) from the 'first' to the 'second' terminal voltage permits to precisely control the final value of V_C. If the two terminal voltages involved satisfy some auxiliary constraints, the reachable range for V_C at $I_{res} = 0$ in-

cludes the inverse of the initial value of V_C. Figure 3 shows the influence of a varying moment of turnover from the first to the second current segment on the shape of the resonant current (fig. 3a) and on the capacitor voltage (fig. 3b). The state-plane portrait of the operation of the converter for this case has been drawn in figure 3c.
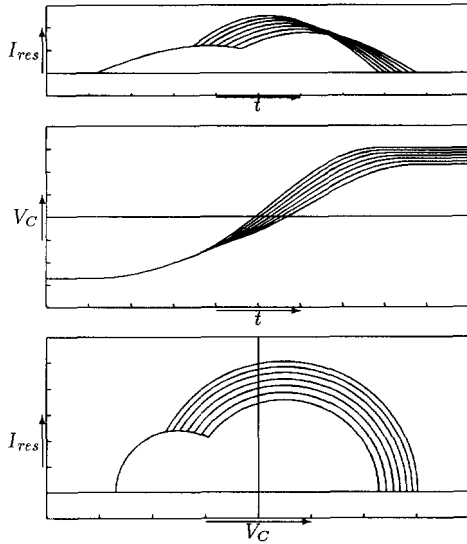

Fig. 3: Signal shapes for a resonant sine wave composed of two current segments for varying turnover time t_1
a: (upper) I_{res}: Current through L_{res}
b: (middle) V_C: Voltage across C_{res}
c: (lower) I_{res} vs. V_C

The trajectories in fig. 3c are each composed of two circle segments. The first circle is centred around the first voltage (V_{LC1}) applied to the resonant tank, and the second segment is centred around V_{LC2}. If the values for V_{C0}, V_{C2}, V_{LC1}, and V_{LC2} are supplied, the construction of the trajectory is straightforward. Clearly, the proper moment for turnover is indicated by the intersection of the two circles.

3.3 Predictor circuit

For the real-time control of the peak capacitor voltage (V_{C2}) we need to determine the instant in time where the two circles of the state plane trajectory intersect. In this converter we have used the following method.

The value of the capacitor voltage at the instant of turnover (V_{C1}) can be derived analytically from the equations describing the circuit behaviour. Skipping the derivation, which can be found in [6], this value

is given by:

$$V_{C1} = \frac{V_{C2}(V_{C2} - 2V_{LC2}) - V_{C0}(V_{C0} - 2V_{LC1})}{2(V_{LC1} - V_{LC2})} \quad (1)$$

where V_{C0} equals the initial value of the capacitor voltage, and V_{LC1} and V_{LC2} indicate the voltages applied to the resonant circuit during the first and second current segment, respectively. Note that if no disturbances are present, then

$$V_{C0} + V_{C2} = 0 \quad (2)$$

which simplifies equation 1 somewhat. However, we have used the complete equation for our control setup.

The value of V_{C1} in equation 1 can be computed in real-time, and compared to the actual (measured) value of the capacitor voltage. As soon as the latter crosses the value of V_{C1}, the turnover to the second current segment is initiated.
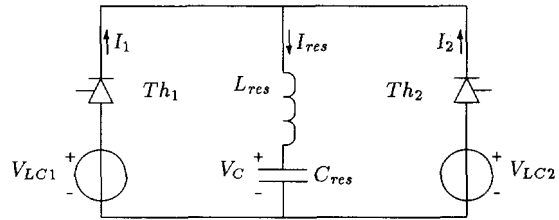
3.4 Commutation

Fig. 4: The part of the power circuit of figure 1 which is active during one resonant half cycle

For the duration of one resonant half cycle, the active part of the circuit of figure 1b can be drawn as in figure 4. For convenience, in figure 4 the first voltage (V_{LC1}) applied to the resonant circuit has been drawn at the left, and the second voltage (V_{LC2}) at the right. However, these voltages can correspond to any of the terminals (input or output) in figure 1b.

If SCR thyristors are used for the power semiconductors, the sequence of voltages applied to the resonant circuit is subject to the laws which govern the commutation of current from one thyristor (Th_1 in figure 4) to the other (Th_2). Inspection of the circuit shows that if I_{res} is positive, V_{LC2} needs to be more positive than V_{LC1}, in order to be able to turn off Th_1.

The currents in the two voltage sources show infinitely steep transients at the instant of turnover. For physical thyristors, these steep current slopes would lead to high turn-on and turn-off losses. Also, high levels of EMI (electromagnetic interference) may be expected. Therefore, in the real circuit commutation inductances are placed in series with the thyristors in order to smoothen the current transients somewhat. It needs to be noted that these

inductances have not been incorporated in the circuit model on which the predictor operation has been based. As a consequence, deviations in the peak capacitor voltage can occur.

3.5 Current control

With the sign conventions of figure 4 the currents in both voltage sources flow in the same direction as I_{res}. Clearly, during the next resonant half cycle I_{res} will flow in the opposite direction. This implies that at least two (other) terminals should be available which can handle this direction of current flow. We will come back to that matter in the following section. For every half cycle a finite amount of charge is transported to two out of the six terminals of the converter. For the next current pulse other terminals can be chosen, which implies that in time every terminal can be supplied with the desired amount of charge. A control loop is needed to adjust the charge transfer process in order to arrive at the desired current flow in every terminal.

The control system which we have used consists of a modified ASDTIC controller [3, 9] for every terminal of the power circuit. In this controller, every terminal is associated with an ASDTIC error signal which is defined as follows:

$$\text{Err} = \int (i - i_{ref})dt \qquad (3)$$

The sum of the rectified ASDTIC errors, which can be interpreted as an overall error signal, is used to trigger the generation of a new current pulse.
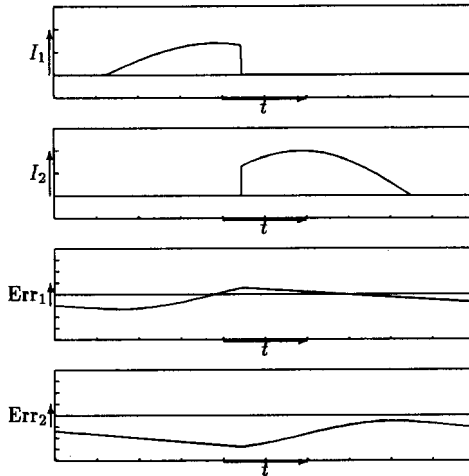

Fig. 5: Signals in the control system

Some signals in the modified ASDTIC control system have been shown in figure 5. The upper traces show the currents in the two voltage sources of fig. 4. The

lower traces show the corresponding ASDTIC error signals. The figure shows that due to the displaced charge of the current pulse the two ASDTIC signals are restored to a position closer to zero.

4 Selection of terminals

The flow of current in the resonant circuit is initiated when the overall error signal, composed from the individual terminal error signals, crosses a certain bound. However, in *which* terminals the current is going to flow is still to be decided. From the previous discussion two items are of special importance here:

- The currents in both terminals which will be serviced during this particular resonant current pulse will flow in the same direction as the resonant current, and

- In order to be able to keep the peak capacitor voltage at a predictable level, the voltages on these two terminals need to oppose each other.

Of course, the charge transported by a resonant current pulse needs to be used to lower the overall error signal. Therefore a selection of terminals according to the sign and magnitude of their individual error signals is appropriate.

4.1 Strict polarity check

For the situation depicted in figure 5, it obviously would be wise to service those terminals with the most negative error signal first.

If we were to adhere strictly to this polarity criterion, the minimum number of terminals for a converter would appear to be 4. Two out of these terminals would operate with positive current flow, and be serviced during the positive resonant half cycles, and the other two would be serviced during the negative half cycles.

Closer inspection of the circuit operation would indicate that proper operation of a 4-terminal converter would hardly be feasible. Due to the exact inversion of the capacitor voltage the net energy consumption of the converter over a resonant half cycle is zero. Therefore both the two 'positive' and the two 'negative' terminals are subject to an energy constraint, which for the 'positive' pair can be formulated as follows:

$$I_{+1} \times U_{+1} + I_{+2} \times U_{+2} = 0 \qquad (4)$$

and similarly for the 'negative' pair. I_{+1} here denotes the current in the first 'positive' terminal, etc.

Furthermore, due to Kirchhoff's current law the sum of the currents flowing into the converter over one complete resonant cycle needs to be zero. Consequently, this also applies to the average current over any time span:

$$I_{+1} + I_{+2} + I_{-1} + I_{-2} = 0 \qquad (5)$$

Three constraints applied to four currents implies that only one current can be chosen freely in this situation: the other three can then be found using the constraining equations.

In the (more interesting) case of a three-phase to three-phase converter, we would expect to have three degrees of freedom (six terminals - three constraints). These three degrees can be used to select the wave shapes of the three output currents, the input currents would then be defined by the constraints. It follows that in this situation we are not able to select the shape of the input currents: the system has too many constraints to achieve this. This conclusion was confirmed by a simulation of this system: although the output currents conformed reasonably well to their prescribed (sine) wave shapes, the input currents showed a ragged appearance. The reader may want to compare this result with the simulation data given in [1].

4.2 Loose polarity check

Inspection of the operation of the simulated converter revealed that as a consequence of the strict polarity check the control system spent a large percentage of time waiting for one of the terminal voltages or - current references to pass through zero. For the controller with a strict polarity check, a signal being at +1 or -1mV makes a large difference. However, a human observer would interpret both values to be 'close to zero'.

Trying to mimic this observation in the control system, it was decided to loosen the polarity check. For example, for a positive half wave of the resonant current, we would first select the terminal with the most negative or least positive error signal. Then, on the remaining terminals with opposite polarity of the voltage, we would again perform a similar selection. In some instances this schedule could for example lead to positive current flow in a terminal with an already positive error signal, thus in fact worsening the situation for this individual terminal. However, for the complete converter system the total error is still lowered. Contrary to the setup with a strict polarity check, the operation of the complete system does not stall any more because we might for example have only one terminal with positive current flow. Simulation of this setup showed superior performance. It was even shown to be possible to operate a three-terminal converter in this way.

4.3 Algorithm

Similarly to the system which has been discussed in [6], we have used a sequential two-pass selection circuit here. During the *first pass*, the terminal with the most positive (least negative) or most negative (least positive) error signal, depending on the direction of the resonant current (polarity of V_C), is selected. The *second pass* is used to select a second terminal from the remaining terminals with an opposing voltage.

After the selection process, the thyristor which is going to conduct during the first current segment can be fired. Turnover to the second current segment is initiated when the Vcpeak-predictor circuit indicates that the cross-over point between the two trajectories of figure 3 has been reached. The second current segment is terminated when the resonant current again reaches zero. After an appropriate turn-off time, the circuit is ready for the next current pulse.

5 Simulation

In order to test the intended operation of the power circuit and its control, a simulation needed to be set up. Due to the similarity of the 'new' circuit to its 'old' counterpart, it was decided to re-use the software which had been written for that circuit [6]. It was found that only minor modifications were needed in the analog sections of the simulation. However, the new selection algorithm made it necessary to reprogram the digital part of the circuit.

The operation of the circuit starting at zero initial conditions has been depicted in figure 6. In figure 6,
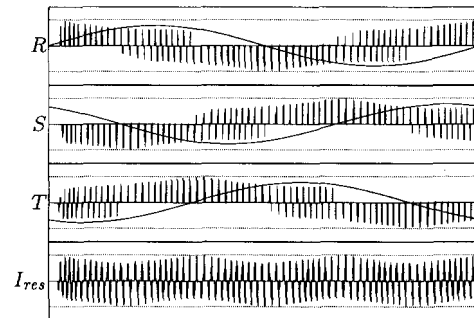

Fig. 6: Simulation of the operation of the new circuit configured as a reactive current compensator. Upper traces: unfiltered current and voltage in terminal R, S, and T respectively, Lower trace: current in the resonant tank. The simulated time span is 20 ms.

the converter is configured as a three-phase reactive current compensator. The upper traces show the current pulses flowing in the three input terminals and the associated voltages. The current pulses show a typical 90 deg. phase shift when compared to the corresponding voltage.

Figure 6 shows that around the 'zero crossings' the currents are composed of alternating positive and negative pulses. This kind of behaviour would not be compatible with a strict polarity check.

Figure 7 shows the operation of the system configured as a three-phase to three-phase converter. The simulated input frequency is 35 Hz, the frequency of the output voltages is 50 Hz. The traces in figure 7 show the division of resonant current pulses over
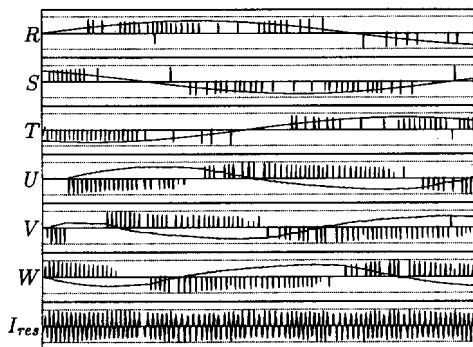
Fig. 7: Simulation of the operation of the new circuit configured as a three-phase AC to three-phase AC convertor.
Upper traces: unfiltered current and voltage in terminals R, S, and T (inputs) and U, V, and W (outputs) respectively,
Lower trace: current in the resonant tank.
The simulated time span is 20 ms

the input (R, S, T) and output (U, V, W) terminals. Due to the larger number of degrees of freedom, the alternating pulse pattern which was shown in figure 6 is practically absent here.

In the simulation, the converter is loaded with 3 resistors of 75Ω in a star configuration. Through simulation experiments it was found that this is approximately the maximum resistive load which can be powered for this configuration. At a rated line voltage of 380 V (rms), this corresponds to an output power P of:

$$P = \frac{380^2}{75} = 1925W. \qquad (6)$$

It is interesting to note that the 'old' power circuit configuration (see figure 1a) was able to power a threefold load (25Ω in star, see [6]). The main reason for this difference is rooted in the fact that in the new power circuit only one side of the resonant tank is used to supply current to the terminals. Another reason lies in the handling of reactive output power. The old power circuit was able to transfer power between two terminals and supply current to the third in one resonant half cycle. The new circuit needs a complete resonant cycle to accomplish the same.

6 Measurements

For the experimental verification of the new concept, a prototype converter needed to be constructed. The primary goal of the experiments being to show the operation of the new control system on real hardware, it was decided to recuperate an existing circuit. The prototype circuit therefore does not feature the highest possible efficiency for this configuration, but in our assessment this is not a serious drawback.

Table 1 lists the most important parameters of the prototype circuit.

L_{res}	148 μH
C_{res}	2 μF
C_o	90 μF
L_c	20 μH
thyristors	SKFT60/12DT

Table 1: Parameters of the prototype circuit

As has been discussed in section 3.4, commutation inductances (L_c) were placed in series with the thyristors in order to limit the di/dt values applied to these components. A more thorough description of the power circuit can be found in [6].

In order to convert the old into the new topology, two major changes were called for:

- The two lower rails in figure 1a needed to be connected together, and

- it needed to be made sure that the lower row of switches would never be activated.

The digital part of the control electronics was implemented using programmable logic devices (EPLD's), which made the latter change rather straightforward. With these, and some minor changes in the analog control electronics, we obtained a configuration according to the topology of figure 1b.

6.1 Three-phase operation

Figure 8 shows the operation of the prototype converter configured as a three-phase reactive current compensator.

The measured signals in figure 8 show good agreement to the simulation results in figure 6. Differences lie mainly in fast transient effects, which were not modeled in the simulation which yielded figure 6.

6.2 Three-phase to three-phase operation

Figure 9 depicts some waveforms in the system operating as a three-phase AC to AC converter. The input frequency is 50 Hz, the converter generates an output voltage at 25 Hz.

7 Conclusions

The operation of a prototype of series-resonant converter with a new topology has been presented. The new topology uses only half the number of thyristors compared to older topologies. This advantage is offset by a relatively low power handling capacity of this topology. The converter is capable to generate or consume reactive power at both input and output ports.
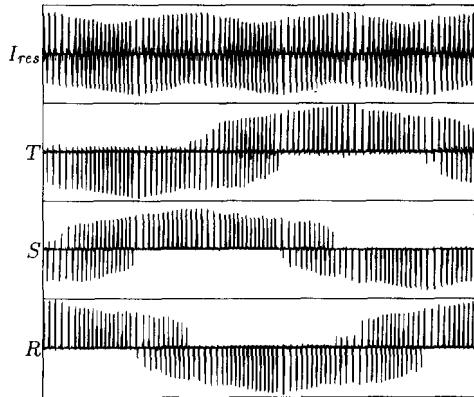
Fig. 8: Currents in the prototype of the new circuit operated as a reactive current compensator
Upper trace: current in the resonant tank.
Lower traces: unfiltered currents in terminal T, S, and R respectively.
The full range of every trace is -52.4 to 52.4 A.
The time scale covers 20 ms.

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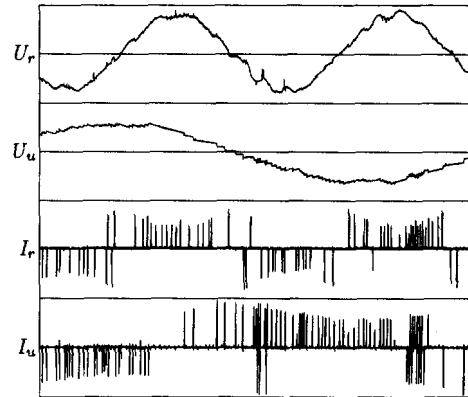
Fig. 9: The prototype of the new circuit operated as a three-phase AC to AC converter.
Traces (from high to low):
U_r: voltage on input terminal R
U_u: voltage on output terminal U
I_r: current through input terminal R (unfiltered)
I_u: current in output terminal U (unfiltered)
The full range of the voltage traces is -240 to 240 V, the current traces range from -52.4 to 52.4 A.
The time scale covers 40 ms.

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