A Multiply-by-3 Coupled-Ring Oscillator for Low-Power Frequency Synthesis

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***Abstract*—A frequency-synthesis technique which extracts the Nth harmonic from an N-stage oscillator is presented. This technique enables significant power savings in the prescaler of a frequency synthesizer. The maximum achievable voltage swing from such an oscillator is estimated. To study this technique, a multiply-by-3 circuit with two 180°-coupled single-ended three-stage ring oscillators has been fabricated in 0.24-μm CMOS, designed to work in the 902–928-MHz ISM band (U.S. and Canada). It provides two outputs: one at the normal operating frequency of the oscillator and the other at three times that frequency. The circuit can work at voltages as low as 1.3 V, while consuming 210 μA of current.**

***Index Terms*—Frequency synthesizers, oscillators, phase-locked loops, prescalers, radio transceivers, wireless personal area networks.**

I. Introduction

NEW WIRELESS applications are emerging where power is the overriding concern. For applications such as wireless personal area networks (WPANs) and wireless integrated sensor networks (WINS), there is great interest in designing fully integrated low-power transceivers. One of the circuit building blocks which consumes a significant amount of power in the analog front-end is the prescaler in the frequency synthesizer. The prescaler takes the high-frequency output of the synthesizer and divides it down to the frequency of the reference crystal oscillator. Since most synthesizers use flip-flop-based digital prescalers, their power consumption scales with the output frequency.

The entire prescaler is usually a cascade of smaller ones, rather than just one lumped block. The greatest power consumption takes place in the input prescaler, which operates at the highest frequency. Efforts have been made to use current-mode digital gates [1] and analog injection-locked oscillators to reduce the power consumption in the input prescaler [2]–[4].

This paper presents a technique which aims to circumvent this entire problem. Using this technique, an N-stage ring oscillator running at a frequency ω_0 provides two outputs: one at ω_0 and the other at a multiplied frequency, $N\omega_0$. As shown in Fig. 1(a), the burden of frequency division on the prescaler in phase-locked loops (PLLs) is reduced, since the output at ω_0 drives the prescaler to close the loop, while the output at $N\omega_0$ is used as the final output of the PLL. This can result in significant power savings in the prescaler. This technique is similar to the one presented in [5], but extracts the multiplied frequency signal directly from a convenient node within the oscillator. No external edge combiners are required.

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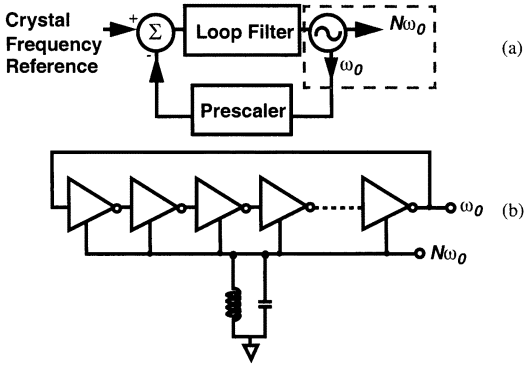

Fig. 1. (a) New oscillator. (b) Single-ended implementation of the oscillator.

II. Principle of Operation

Consider an ordinary *LC* voltage-controlled oscillator (VCO) with an nMOS cross-coupled pair operating at ω_0. It is well known that the common-source node of cross-coupled pair moves at $2\omega_0$, thanks to nonlinearities. This oscillator can also be viewed as a single-ended two-stage oscillator with *LC* tank loads. Extending this idea, we can build a multiply-by-N oscillator if we use N identical stages and connect the sources of all the devices together. In Fig. 1(b), we have a single-ended N-stage ring oscillator to generate outputs at ω_0 and $N\omega_0$. Instead of using a current source, we use an *LC* tank to filter out additional harmonics, and provide a dc ground. Due to the phase relationship among the voltages and currents of the different stages of the ring oscillator, only harmonics of $N\omega_0$ appear at the high-frequency output.

As the ring oscillates, current pulses are generated by all stages as the gates of the transistors are driven high (Fig. 2). As a result, these current pulses are in phase with the gate voltages of each stage of the ring. We are interested in the current pulse train that is injected from the ring into the resonator. If the natural free-running period of the N-stage coupled ring oscillator is $T = 2\pi/\omega_0$, then N identical, equally spaced pulses are injected into the resonator from the ring during this interval, in the absence of stage mismatch. It is clear from Fig. 2 that the period of the injected pulse train is T/N. Therefore, the voltage generated in the resonator due to the incidence of this pulse train also has a period T/N and contains only harmonics of $N\omega_0$. We shall see that by using a differential implementation of this oscillator, we can largely cancel out the even harmonics, so that ideally only odd harmonics of $N\omega_0$ remain at the differential output. These harmonics may be far enough away to be significantly filtered by an integrated *LC* tank. If the ac voltage generated due to this current injection into the *LC* tank is small compared to the voltage swing within the ring itself, the operation of the ring is not greatly affected by using this technique.

Due to device size and threshold mismatch among the oscillator stages, the current pulses injected into the resonator will

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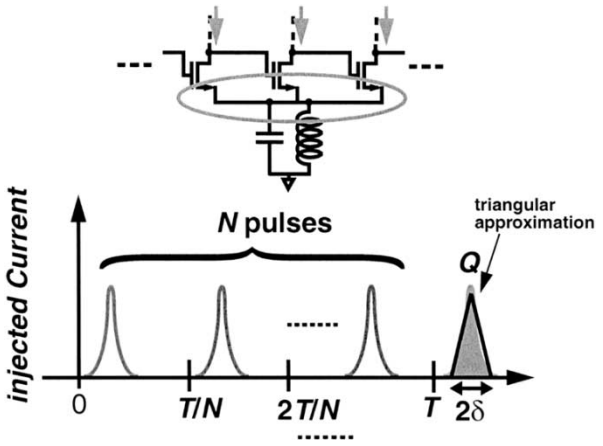

Fig. 2. Injected current pulse train.

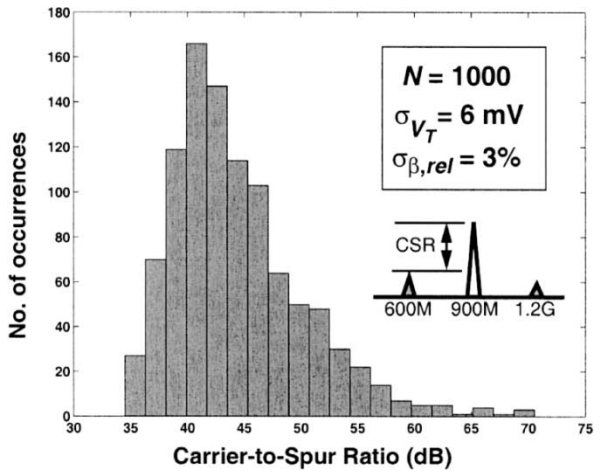

Fig. 3. Monte Carlo simulation results for spur generation due to nMOS device mismatch.

not be identical, leading to spurious tones at ω_0 and its harmonics in the output spectrum. Tones far from resonance may be significantly filtered, but tones at frequencies $(N-1)\omega_0$ and $(N+1)\omega_0$ could be potentially troublesome. To study the effect of device mismatch, Monte Carlo transient simulations are carried out on a single-ended multiply-by-3 ring oscillator with a high-frequency output at 900 MHz. The adjacent spurious tones are at frequencies 600 and 1200 MHz. Fig. 3 plots the distribution of the simulated carrier-to-spur ratio at the high-frequency node of the oscillator for 1000 samples. The V_T and β values of all nMOS devices in the oscillator are assumed to be independent Gaussian-distributed variables with standard deviations of 6 mV and 3% (relative), respectively. The *LC* tank used for this simulation has a quality factor of 3. According to Fig. 3, spur suppression better than 35 dBc should be readily achievable by following careful layout practices. If this VCO is used as the local oscillator (LO) in a receive chain, these spurs would downconvert the unwanted signals and noise from 600 and 1200 MHz bands. Since the spurs are relatively far from the carrier frequency, band preselect filtering before the mixer, used in conjunction with further on-chip filtering of the LO, can be used to ensure sufficient noise and interference suppression.

III. Output Amplitude Versus Current Consumption

This technique can save significant power in the prescaler since the PLL loop is closed around the lower frequency output of the oscillator. However, the voltage swing at the high-frequency node may be significantly smaller than the swing at the low-frequency output. In this section, we compare the output signal amplitude for a given current consumption at the high-frequency output of the oscillator versus that in an ordinary *LC* oscillator in the current-limited regime. Consider the current pulse injected into the resonator with period T/N, where $2\pi/T = \omega_0$. Assume that each current pulse has a total charge Q and can be approximated with a triangular pulse of base 2δ and height Q/δ (Fig. 2). In steady-state operation, all the charge that is injected into the *LC* tank is drawn directly from the power supply. Therefore, the dc current consumption for the entire oscillator $I_{\rm DC}$ is NQ/T. For the periodic triangular waveform, the magnitude of the Fourier coefficient of current at the fundamental frequency of $N\omega_0 = 2N\pi/T$ is

$$|c_1| = \frac{NQ}{T} \cdot 2 \left[\frac{\sin\left(\frac{N\pi\delta}{T}\right)}{\left(\frac{N\pi\delta}{T}\right)} \right]^2. \tag{1}$$

Using $I_{\rm DC} = NQ/T$, and assuming that the tank impedance is R_P, the voltage amplitude at $N\omega_0$ due to this current is

$$|V_{\rm mult}| = 2 \left[\frac{\sin\left(\frac{N\pi\delta}{T}\right)}{\left(\frac{N\pi\delta}{T}\right)} \right]^2 I_{\rm DC} R_P. \tag{2}$$

For an *LC* oscillator operating at $N\omega_0$ and biased with current $I_{\rm DC}$, the current injected into the resonators is nearly a square wave, and the maximum differential voltage generated at the terminals of the *LC* tank is $(4/\pi)I_{\rm DC}R_P$ in the current-limited regime. Comparing with (2), we see that the voltage swing achieved at the multiplier node is quite comparable to the swing in an *LC* oscillator in the current-limited regime. The amplitude at the multiplier node depends on the sharpness of the current injection and the resulting dc current consumption. The sharpness of the injection is determined by the nonlinear characteristic of the devices. For $\delta \to 0$, we get sharp current impulses injected into the *LC* tank and the voltage generated at the high-frequency output of the multiply-by-3 oscillator approaches $2I_{\rm DC}R_P$. For $\delta = T/4N$, the voltage produced is $(4/\pi)^2 I_{\rm DC}R_P$, which is still larger than the *LC* oscillator. For a circuit with $R_P = 600\,\Omega$ and $I_{\rm DC} = 150\ \mu$A, using $\delta = T/4N$ in (2), we find that the expected voltage swing is roughly 145 mV. In transient simulations, we observe a swing of nearly 100 mV at the multiplier node. By comparison, the maximum swing the current-limited *LC* oscillator could achieve for the same tank impedance and current consumption is 114 mV.

The amplitude of the signal does not grow indefinitely with current consumption. For larger voltage amplitudes, the operation of the nMOS transistors is affected due to the large voltage swings at the common-source node, and the shape of the current pulse train becomes less sharp. Simulations indicate that it is difficult to achieve single-ended voltage amplitudes greater than about one-tenth of the power supply voltage at the multiplier node. If larger voltage amplitudes are desired, narrow-band voltage transformers [10] can be used at the cost of larger area, but very little additional power.

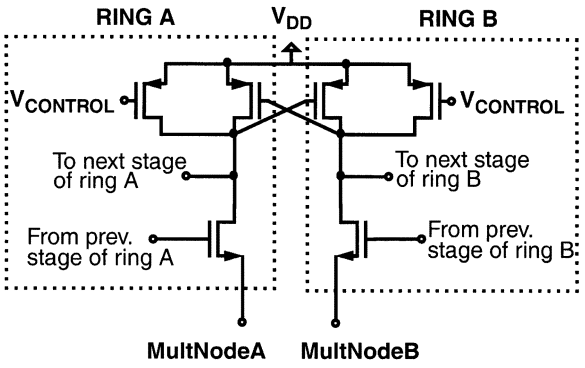

Fig. 4. Differential multiply-by-3 oscillator stage.

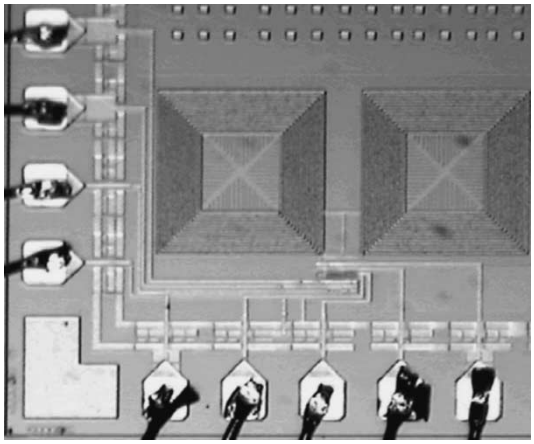

Fig. 5. Die photograph.

IV. Implementation Details

A multiply-by-3 circuit with two 180°-coupled single-ended ring oscillators has been designed and fabricated in 0.24-μm CMOS. For superior noise immunity, we desire differential outputs at both the high- and low-frequency nodes of the oscillator. To achieve this, all stages of both single-ended rings are connected with cross-coupled pMOS pairs to maintain a 180° phase condition between the two rings. Fig. 4 shows circuit implementation of each stage of the circuit, which is similar to [9]. The highlighted box indicates to which single-ended ring each part of the stage belongs. The circuit has two differential outputs with twice the voltage swing on both nodes, at the cost of twice the current consumption. As mentioned earlier, this allows us to cancel out the even harmonics of $N\omega_0$ at the high-frequency output. The multiplier output nodes are shorted together and connected via an *LC* tank to ground. The differential output from the high-frequency nodes connects to the gate of buffers to drive an off-chip 50-Ω load. The normal output of each stage of the ring oscillator is loaded with an identical cell, which is then also buffered to drive an off-chip 50-Ω load. The inductors in the *LC* tank have been designed to maximize the tank impedance at 900 MHz. They consist of three strapped upper metal layers (in a five-metal CMOS epi process) and have an outer diameter of 320 μm. They also have a patterned ground shield to minimize capacitive current loss and to present a well-defined parasitic capacitance. The quality factor Q for the tank is expected to be 3–5. A photograph of the circuit is shown in Fig. 5. The area occupied by the circuit is roughly 0.2 mm^2, of which about 98% is occupied by the inductors.

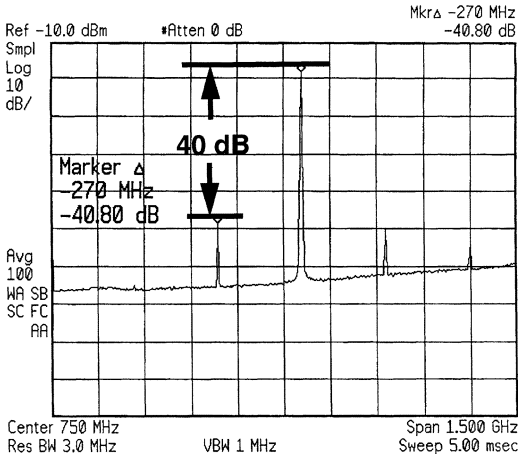

Fig. 6. Output spectrum at the high-frequency node.

V. Measurement Results

The measured output spectrum at the multiplier node of the oscillator is shown in Fig. 6. The main peak of the spectrum has -16 dBm power, and the carrier-to-spur ratio is nearly 40 dB. The buffers to drive the off-chip 50-Ω loads consume 2 mA from a 2.5-V supply.

Fig. 7(a) shows the frequency tuning range of the VCO for different power-supply voltages. If it is to be used in the 902–928-MHz ISM band, the circuit can work at power supplies as low as 1.3 V. Fig. 7(b) shows the current consumption of the oscillator as a function of the control voltage. While operating in the ISM band frequencies at 1.3 V, the oscillator consumes 210 μA of current.

Fig. 8 shows the phase noise at the two outputs of the ring oscillator, measured using an HP4352B VCO signal analyzer. The phase noise plots correspond to a power-supply voltage of 1.3 V and a control voltage of 0.1 V. The high-frequency output was nearly 920 MHz. At frequencies close inband, the phase noise plots flatten due to the 20-kHz loop bandwidth of the PLL-based measurement setup. As expected, the phase noise of the ring oscillator is poor, and the phase noise at the higher frequency output is $20log(3) = 10$ dB worse than the low-frequency output at all frequencies. At an offset frequency of 1 MHz, the measured phase noise is roughly -94 dBc/Hz for the 920-MHz output. The measurement setup was not electromagnetically shielded, and this may be the cause of the unexpected spurious peaks in the data at frequencies around 1–4 MHz.

Table I compares the power consumption in the first divider against various other published examples at 900 MHz. Clearly, we can save significant power by using this circuit, provided we are willing to sacrifice phase noise performance. It is important to note that this is not a limitation of the technique itself, but rather of *RC* ring oscillators in general. Low-power ring oscillators seem well suited for applications which have relaxed performance requirements, but need to consume very little power. If we can spare more power, then we can improve the phase noise of the oscillator as a whole. In addition, this technique can

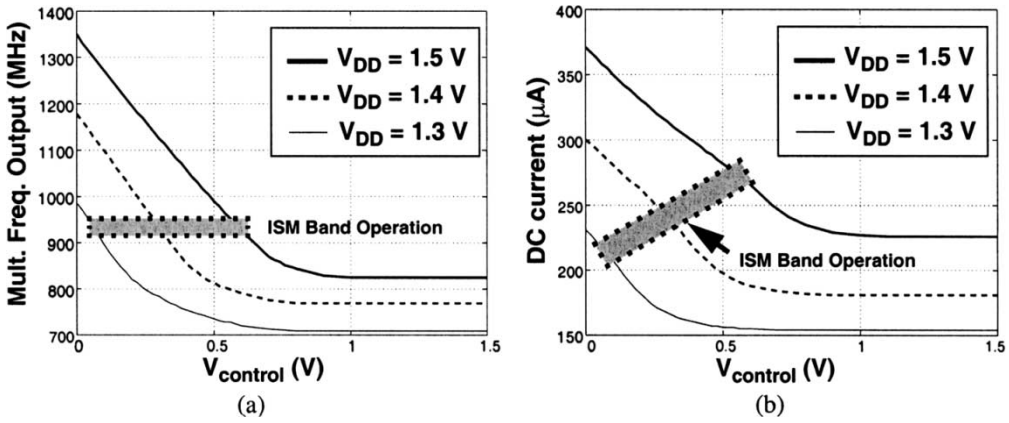

Fig. 7. (a) Tuning range. (b) Current consumption.

TABLE I
INPUT DIVIDER POWER COMPARISON

	This Work	[6]	[1]	[7]	[8]
1st Divider Factor	3	2	2	4/5	2/3
1st Divider Power	0 mW *	1.77 mW	0.25 mW	0.54 mW	2.5 mW **
Free-Running Ph. Noise of VCO	-94 dBc/Hz @ 1 MHz	N.A.	-98 dBc/Hz @ 25 kHz	N.A.	-144 dBc/Hz @ 3 MHz
Technology	0.25μm CMOS	0.6μm CMOS	0.25μm CMOS	0.25μm BiCMOS	0.35μm CMOS
Tank Q Factor	3-5	30	20	off-chip	13
Application	WPAN	WINS	Paging	ISM	GSM

* No divider necessary to get 300 MHz from 900 MHz.
** assuming that half the power consumption of the divider occurs in the first stage.

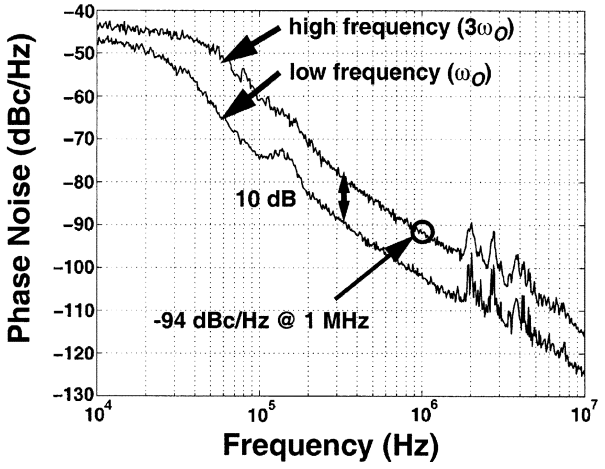

Fig. 8. Phase noise at both outputs.

be applied to multistage *LC* oscillators which have better phase noise properties. Therefore, the technique could be extended to higher performance systems.

VI. CONCLUSION

A technique to extract the Nth harmonic from an N-stage ring oscillator has been described. A major application is in PLLs which perform frequency synthesis. This technique enables significant power savings in the prescaler. It has also been shown that for a given current consumption, the achieved voltage swing at the high-frequency output of the oscillator is comparable to that of an ordinary *LC* oscillator. A three-stage coupled ring oscillator has been designed and tested to operate in the 902–928-MHz ISM band. The circuit is capable of working at low power-supply voltages, while consuming very little current.

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