A Multirate Digital Multicarrier Demodulator: Design, Implementation, and Performance Evaluation

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Abstract—**The new generation of "user-oriented" satellites are conceived to involve a dramatic reduction in the earth station size and complexity. Frequency division multiple access (FDMA) and single channel per carrier (SCPC) in the uplink and time division multiplexing (TDM) in the downlink are employed in the system described here. To interface FDMA in the uplink and TDM in the downlink, multicarrier demodulation (MCD) is required on-board the satellite. The operation of the on-board MCD is the separation of each individual channel and subsequent demodulation.**

The results presented in this paper have been obtained under INTELSAT Contract INTEL-479, which has provided an analysis of the advanced technologies and techniques for on-board frequency demultiplexing and demodulation for low bit rate carriers. The study was constrained by the requirement that new-generation payloads could serve the stations already active in the INTELSAT Business System.

A digital hardware design that implements an MCD that can process three channels at 4.4 Mb/s, or 12 channels at 1.1 Mb/s is described in this paper. The test results have confirmed the MCD feasibility, and further improvements are expected from a semicustom implementation.

I. Introduction

THIS paper outlines some results obtained in the area of low bit rate on-board demultiplexing and demodulation. This work studied the design and proof-of-contract (POC) hardware implementation relative to some peculiar architectures for multicarrier or "group" demodulation (MCD). Specifically, it envisaged the implementation of an MCD for INTELSAT Business Services (IBS), i.e., something flexible enough to accommodate a variable number of low-to-medium data rate SCPC's (single channel per carrier), QPSK-modulated within a standard 83 MHz (gross bandwidth) transponder with 120 Mb/s capacity. Transmission bit rates span from 137 to 4369 kb/s—resulting from 64 to 2048 kb/s IBS information rates upon rate—1/2 convolutional encoding and roughly 6.7% overhead (see Table I). A system requirement was that of constructing an MCD capable of operating over the whole range of data rates indicated above, across any 83 MHz transponder. No network synchronization was required.

TABLE I
IBS Open Network ($n \times 64$)-Kb/s Services

Information Rate (kb/s)	Data Rate Including Overhead (kb/s)	Transmission Rate (kb/s)	Occupied Bandwidth (KHz)	Allocated Bandwidth (KHz)
64	68.3	137	82	112.5
128	136.5	273	164	202.5
256	273.1	546	328	328.5
384	409.6	819	492	585.0
512	546.1	1092	655	765.0
768	819.2	1638	983	1147.5
1536	1638.4	3277	1970	2295.0
1544	1638.4	3277	1970	2295.0
1920	2048.0	4096	2460	2880.0
2048	2184.5	4369	2620	3060.0

One attractive architecture for such business services satellite systems envisages different access methods in the two links, i.e., frequency division multiple access (FDMA) in the uplink and time division multiplexing (TDM) in the downlink [1]–[3]. In this way, the user uplink RF power requirements are proportional to the individual bandwidths—differently from TDMA, which requires power levels proportional to the transponder bandwidth and, to some extent, network synchronization procedures are not strictly required. In the downlink, TDM permits the on-board high power amplifier (HPA) to be saturated or slightly backed-off because of the absence of multicarrier intermodulation.

Such an architecture, therefore, optimizes the system RF power resources; however, it requires a nontrivial on-board access format conversion from FDMA to TDM. The heart of the (regenerative) repeater is then represented by a "multicarrier" demodulator (MCD) that recovers the individual modulating streams of the (N) FDMA uplink carriers; subsequent TDM formatting builds up a higher data rate information sequence to modulate an unique (or few) downlink carrier(s) (see Fig. 1). The inherent attractiveness of this FDMA/TDM system architecture for "user-oriented" satellites is counteracted by hardware difficulties related to MCD implementation,

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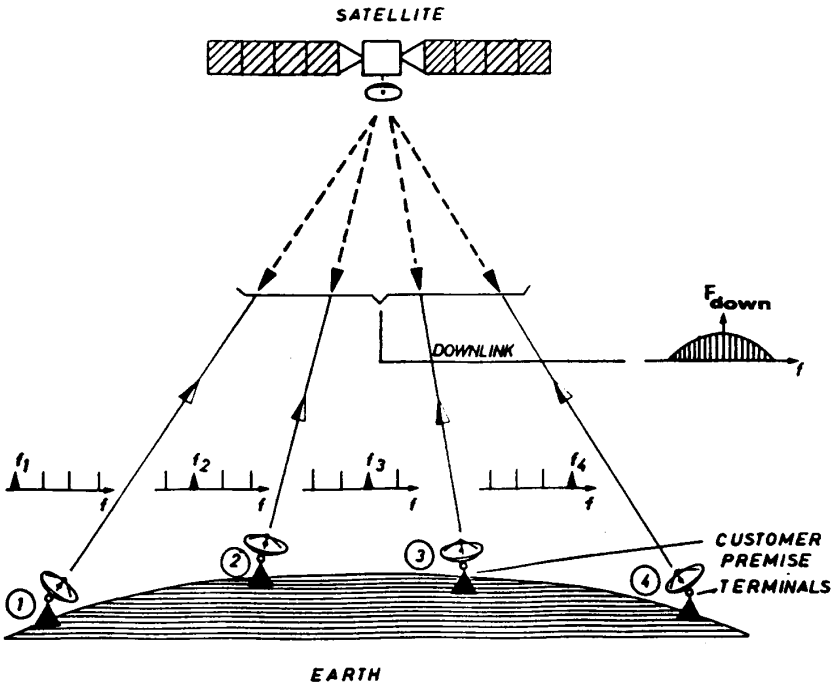


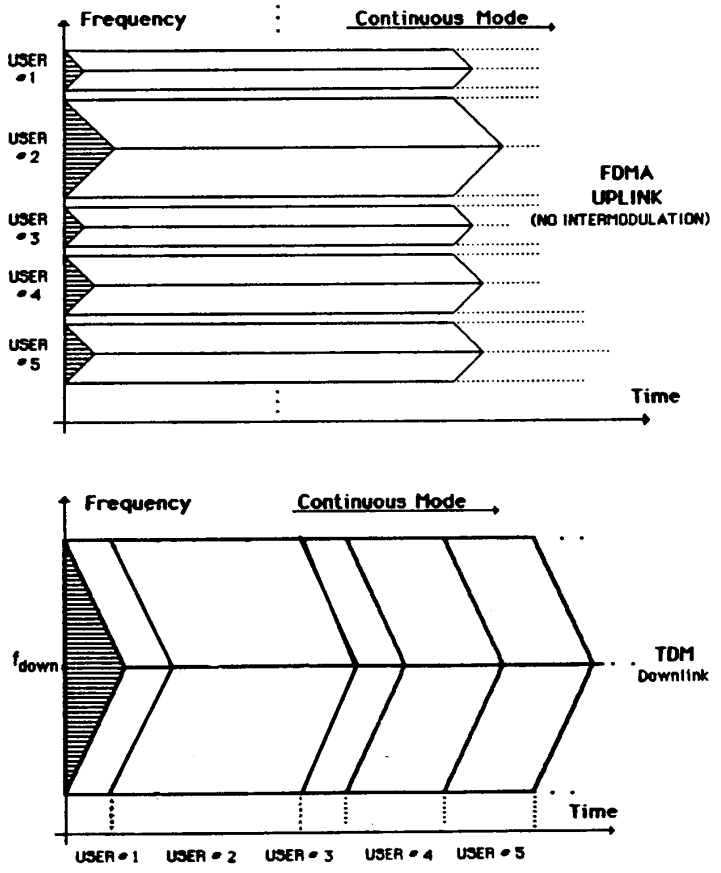


Fig. 1. FDMA–TDM concept.

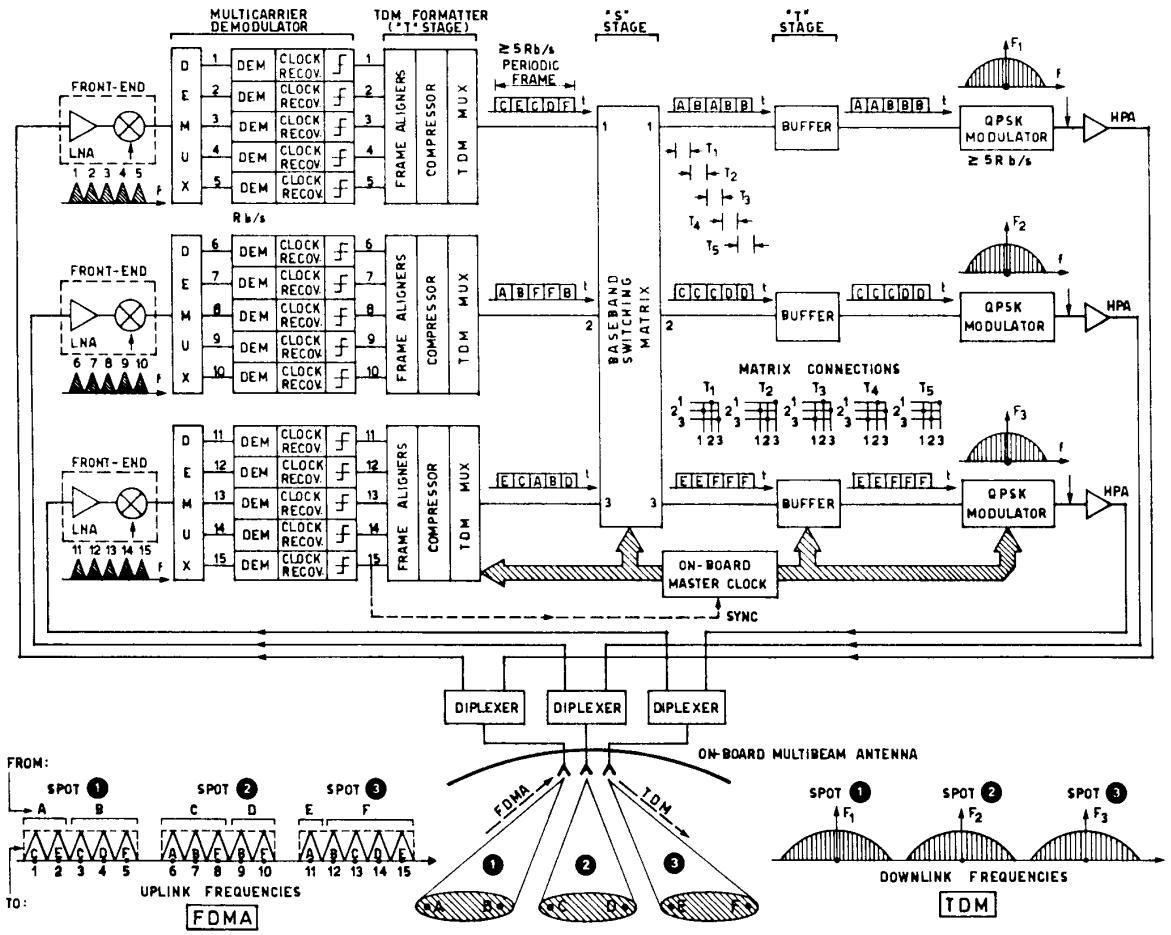


Fig. 2. Transponder block diagram.

which still requires significant mass/power consumption. This can be a limit to the practical (reasonable) feasibility of this type of on-board processing (OBP).

In principle, an N-channel MCD is constituted by an input $1:N$ demultiplexer followed by a bank of N parallel (low-rate) demodulators or a lower number at higher data rate if time-shared among the N outputs from the demultiplexer.

After having illustrated the most attractive architectures/technologies for multicarrier demodulation, some more detailed theoretical aspects are shown in Section II, whereas Section III concentrates on the selected MCD architecture. Section IV summarizes some relevant results of the tests carried out on the proof-of-concept hardware, and some conclusions are drawn in Section V, outlining mass/dc power budgets for alternative technologies suitable to implement a 4.369 Mb/s MCD.

II. Theoretical Aspects

A. Demultiplexer

From a general point of view, the demultiplexing of uplink SCPC's (to be subsequently demodulated) can be implemented using different approaches [4]–[10]. They are often classified as follows: i) per channel; ii) block; and iii) multistage. The per-channel method performs the demultiplexing operation by means of a bank of bandpass filters. Selection of each input signal and its translation to a lower frequency band are achieved by a compound operation of digital filtering and decimation (i.e., decrease of the signal sampling rate). The block method implements the demultiplexing by using a set of digital filters ("polyphase" network) followed by a "block" processor usually of the FFT type that processes the output signals from the digital filters altogether. The multistage method can be considered as a binary tree of two demultiplexers. Each demultiplexing stage performs lowpass and highpass filtering, with subsequent decimation by a factor of two. From an implementation point of view, some considerations and conclusions can be drawn about the three approaches, based upon both theoretical features and results from previously performed studies [22], [23]:

i) per-channel methods generally have higher computational complexity, smaller finite-precision arithmetic sensitivity, greater flexibility, and smaller control circuit complexity

ii) block methods have lower computational complexity, higher finite-precision arithmetic sensitivity, smaller flexibility, and greater control circuit complexity

iii) multistage methods have computational complexity comparable with that of block methods, finite-precision arithmetic sensitivity, control circuit complexity comparable to per-channel methods, and an intermediate degree of flexibility.

Flexibility may be a critical issue for the demultiplexer. In the IBS applications, different transmission rates are foreseen from 137 Kb/s to 4.369 Mb/s and the multicarrier demodulator will have to operate on many of them during the satellite lifetime, to allow for the reconfigurability of the traffic pattern. The transmission rates are, in general, a multiple of the smallest by factors of 2, 3, 5, and a combination.

If we require the demultiplexer to operate at different rates for a fixed processed bandwith, the number of channels Nc is inversely proportional to the transmission rate. Thus, we can observe that

i) block methods are able to operate only at a fixed value of Nc (i.e., number of points of the block processor), requiring a specialized demultiplexer for each individual transmission rate.

ii) per-channel structures are well suited to variations of transmission rates and number of processed channels Nc. It is only required to vary the filter characteristics (i.e., coefficients) and decimation factor, using only the necessary Nc branches of the structure designed for the highest possible value of Nc (lowest data rate). Moreover, the per-channel methods process channels with different transmission rates within that same demultiplexer, as the Nc paths are substantially independent.

iii) multistage structures have an intermediate degree of flexibility, as it allows variations of the transmission data rate, although limited to powers of two.

From the above considerations, the per-channel method is selected to implement the digital demultiplexer. In particular, the analytic signal approach [4] is considered here. The analytic signal approach relaxes the filter specifications, thus achieving a lower implementation complexity with respect to other per-channel approaches. The principle of operation of the analytic signal method is briefly illustrated. Obviously, we will only consider the conversion procedure from the FDMA to the TDM formats, i.e., the one of interest for the MCD. The digital FDMA signal is sampled at the high rate fu (uplink) and processed in order to obtain Nc SCPC baseband digital signals, each sampled at the low rate fd (downlink). According to the sampled signal theory, in the following the arguments of the frequency domain quantities are considered as exponents of the complex exponential, e.g., $S(fTu)$ means $S(e^{jwTu})$.

The spectrum $S(fTu)$ of the input signal $s(nTu)$, where n is an integer, is shown in Fig. 3(a) for $Nc = 4$. The principle of operation of the analytic signal method is also shown in the block diagram of Fig. 3. The signal is filtered by a complex bandpass filter $Hi(fTu)$, being $i = 0, 1, \cdots, Nc - 1$ is the channel index, ideally defined as

$$\underline{Hi}(fTu) = \begin{cases} 1, & ifd/2 < f < (i+1)fd/2 \\ \text{undefined}, & (i-1)fd/2 < f < ifd/2 \\ \text{undefined}, & (i+1)fd/2 < f < (i+1)fd/2 \\ 0, & \text{elsewhere} \end{cases} \quad (1)$$

the frequency band $[0; fu/2]$, and periodicity with a frequency period fu. The frequency response is sketched in Fig. 3(b) and (c) for the odd and even channels, respectively.

The filters $Hi(fTu)$ can be regarded as frequency-translated version of a lowpass prototype $H(fTu)$, according to the relation

$$\begin{aligned} \underline{Hi}(fTu) &= Hi(fTu) + jHi'(fTu) \\ &= H[(f - iW - W/2)Tu] \end{aligned} \quad (2)$$

where W is the channel spacing and $Hi(fTu)$ and $jHi'(fTu)$ are the conjugate symmetric and antisymmetric parts of $\underline{Hi}(fTu)$, respectively. The quantities $Hi(fTu)$ and $Hi'(fTu)$ are, therefore, the frequency responses of the real and imaginary parts, respectively, of the complex impulse response of the filter $Hi(fTu)$. The filter output is a sampled analytic signal $\underline{si}(nTu)$ at the sampling rate fu, which can be expressed in the frequency domain as

$$\underline{Si}(fTu) = S(fTu) * \underline{Hi}(fTu). \quad (3)$$

The spectrum $\underline{Si}(fTu)$ is reported in Fig. 3(d) and (e). The signal $\underline{si}(nTu)$ is decimated by the factor Nc to produce the complex lowpass signal $\underline{ui}(nTd)$, n integer, sampled at the frequency $fd = fu/Nc$ given by

$$\begin{aligned} \underline{ui}(nTd) &= \underline{si}(nNcTd) \\ \underline{Ui}(fTd) &= 1/Nc \sum_{k=0}^{Nc-1} \underline{Si}[(fTd - k)/Nc] \\ &= \{\underline{Si}[(fTd - k1)/Nc] \\ &\quad + \underline{Si}[(fTd - k2)/Nc]\}/Nc \end{aligned}$$

with

$$k1 = i/2 + [1 - (-1)^i]/4, \quad k2 = k1 + (-1)^i. \quad (4)$$

Its frequency spectrum is sketched in Fig. 3(f) and (g) for the odd and even channels, respectively. Now its baseband (i.e., the range of frequency in magnitude not greater than half the sampling frequency) extends to $fd/2$. The complex signal $\underline{Yi}(nTd)$, whose real part is related to the desired demultiplexed digital signal, is given in the frequency domain by

$$\begin{aligned} \underline{Yi}(fTd) &= \underline{Ui}(fTd) * \underline{Gi}(fTd) \\ &= \underline{Si}[(fTd - k1)/Nc] * Gi(fTd)/Nc \end{aligned} \quad (5)$$

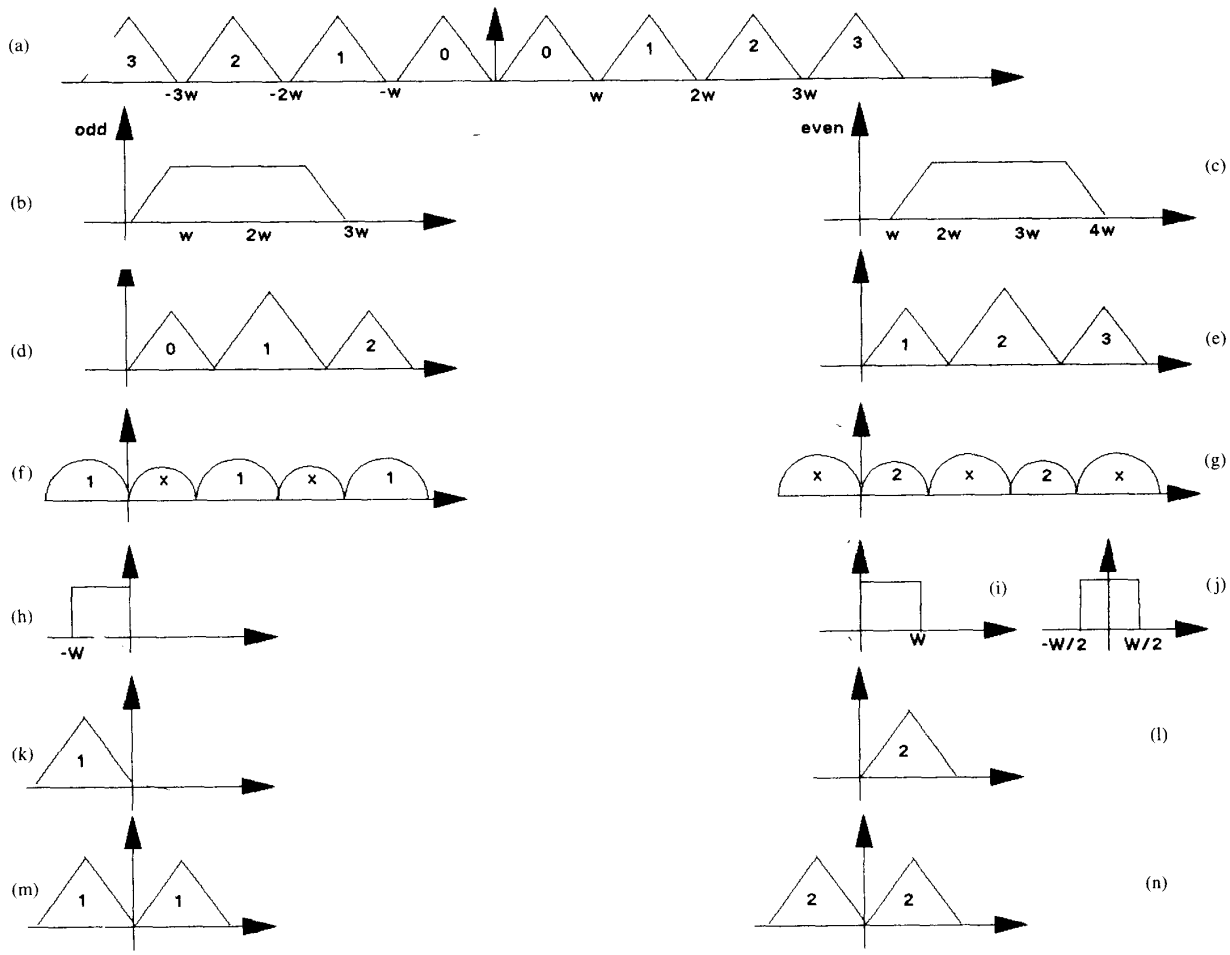


Fig. 3. Frequency dechannelization via the analytical signal method. (a) FDM input signal. (b) and (c) Frequency response of high-rate filters. (d) and (e) Spectra of filtered channels. (f) and (g) Filtered channels after decimation. (h) and (i) Low-rate channel filters. (j) Lowpass prototype. (k) and (l) Complex channel. (m) and (n) Recovered baseband channels.

where the complex $\underline{Gi}(fTd)$ is defined as

$$\underline{Gi}(fTd) = G[(f - (-1)^i W/2)Td]. \quad (6)$$

The ideal frequency response for the filters $\underline{Gi}(fTd)$ is sketched in Fig. 3(h) and (i) for i odd and even, respectively. It is clear they are related, according to (6), to a lowpass prototype filter $G(fTd)$ with a frequency response shown in Fig. 3. It can be noted from (6) that the number of different filters $\underline{Gi}(fTd)$ is actually two: one for the odd channels and the other for the even channels (we retain the filter dependence on the channel index i for notational convenience). The filters $\underline{Gi}(fTd)$ can be expressed by their respective conjugate symmetric part $Gi(fTd)$ and conjugate antisymmetric part $jGi'(fTd)$ as

$$Gi(fTd) = Gi(fTd) + jGi'(fTd). \quad (7)$$

As before, $Gi(fTd)$ and $Gi'(fTd)$ are the frequency responses of the real and imaginary parts, respectively, of the complex impulse response of the filter $Gi(fTd)$. Finally, the real digital signal translated to baseband can be expressed as

$$yi(nTd) = \text{Re}\,\{yi(nTd)\}$$
$$\underline{Yi}(fTd) = 1/2[\underline{Yi}(fTd) + \underline{Yi} * (-fTd)] \quad (8)$$

where $*$ denotes the complex conjugation operator. The output from the demultiplexer, taking in account the spectral inversion for the odd channels, is

$$\begin{aligned} Xi(fTd) &= Yi(fTd + i/2) \\ &= (1/Nc) * s(fTd + i/2) * \{Hi(fTd + i/2) \\ &\quad * Gi(fTd + i/2) - +Hi'(fTd + i/2) \\ &\quad * Gi'(fTd + i/2)\}. \end{aligned} \quad (9)$$

Equation (9) represents the signal of the ith channel correctly translated to baseband and sampled at the low sampling frequency as shown in Fig. 3(m) and (n). The corresponding implementation structure is shown in Fig. 4(b): it only requires processing of real quantities.

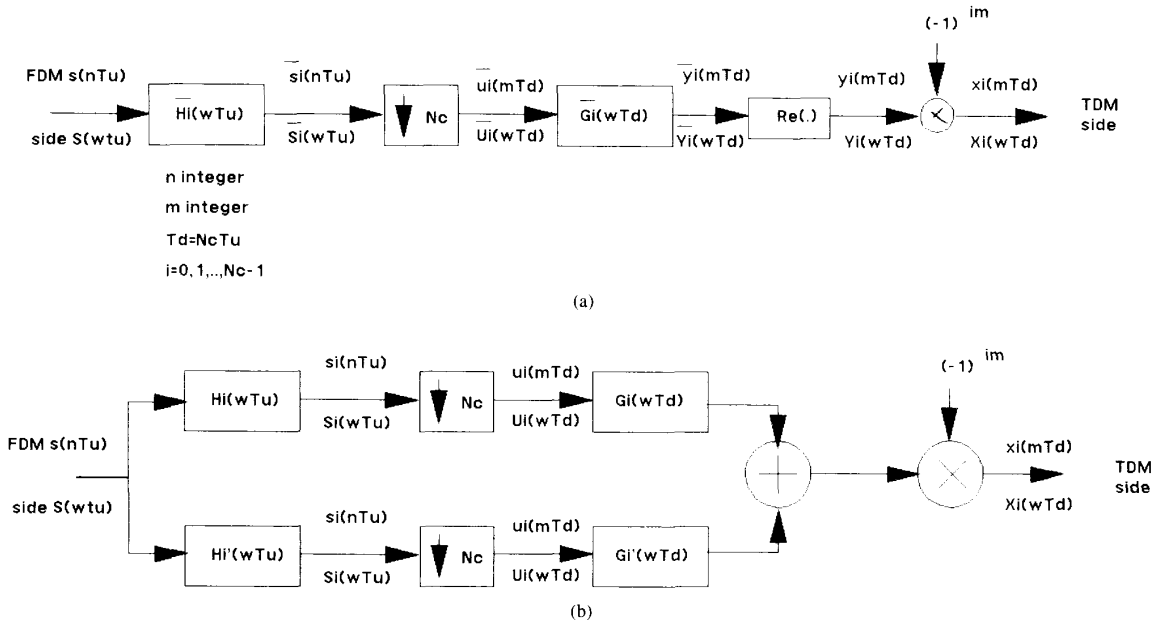


Fig. 4. Analytical signal approach to demultiplexer. (a) Principle block diagram. (b) Implementation block diagram.

It must be pointed out that the analytical signal method has been outlined on the basis of ideal filtering masks; indeed, in real applications there are nonzero transition bands for the filters $Gi(fTd)$ and transition bands wider than W for the filters $Hi(fTu)$. This opportunity gives rise to more relaxed filter specifications and will be fully exploited in the design procedure reported in Section III.

The overall number of multiplications per second and per channel required for the analytic signal approach can be derived as a function of the channel spacing W, the number of channels Nc, and the (one-sided) filtering bandwidth B as

$$\begin{aligned} MAS &= [LH/2 + LG]2W \\ &= kAS\, W^2[W(Nc + 4) - 2B(Nc + 2)]/ \\ &\quad [(W - B)(W - 2B)] \end{aligned} \tag{10}$$

where KAS is defined as

$$KAS = 2/3\ [\text{Log}\ 2/(10\ k1k2)]. \tag{11}$$

From (10), it can be noted that the parameter MAS for fixed Nc and B is a function of W; thus, an optimum, or practically nearly optimum, channel spacing can be chosen in order to minimize MAS.

B. Demodulator

The most demanding parts of the demodulator are the carrier and timing recovery circuits: some useful references are given by [11]–[21]. The choice of these circuits depends on whether the MCD works. This section focuses on a possible implementation structure of the digital receiver which includes the necessary carrier and clock (timing) recovery circuits. In particular, a suitable solution for the carrier recovery is given by the digital version of the one proposed in [9]. Indeed, this carrier phase estimation method achieves a fixed acquisition time and is less sensitive to a finite arithmetic implementation. Simulations have shown that six-bit arithmetic is sufficient to obtain a carrier phase estimate very close to the floating-point implementation. The clock recovery circuit can be efficiently implemented according to the estimation approach proposed in [12]. This is a suitable and simple digital timing recovery circuit, where two samples-per-symbol are required. The estimation algorithm is suitable for both acquisition and tracking modes of operation. Another advantage of this approach is that it is independent of carrier phase offset. Therefore, its acquisition time is not influenced by the carrier phase error.

Fig. 5 illustrates the general structure of the phase estimator considered here. Let the estimation period be TE and let it encompass NE m-ary symbols (each T long), where $TE = NE * T$. Suppose we wish to estimate the phase at the midpoint of the estimation interval and we let $NE = 2N + 1$, where N is the number of intervals before and after the interval where the phase is to be estimated [9] in the presence of additive white Gaussian noise (AWGN) and zero frequency uncertainty. Fig. 5 shows the dotted box eliminated (so that $x'n = xn$, $y'n = yn$) represents the optimal (maximum likelihood) estimator for $m = 1$, which corresponds to an unmodulated carrier. Obviously, if the carrier is phase modulated to one of m discrete phases (m equals 4 for QPSK signals), the above linear estimator is useless since during each successive symbol the phase takes on a different value. Suppose, however, that in the dotted box we insert the two-dimen-

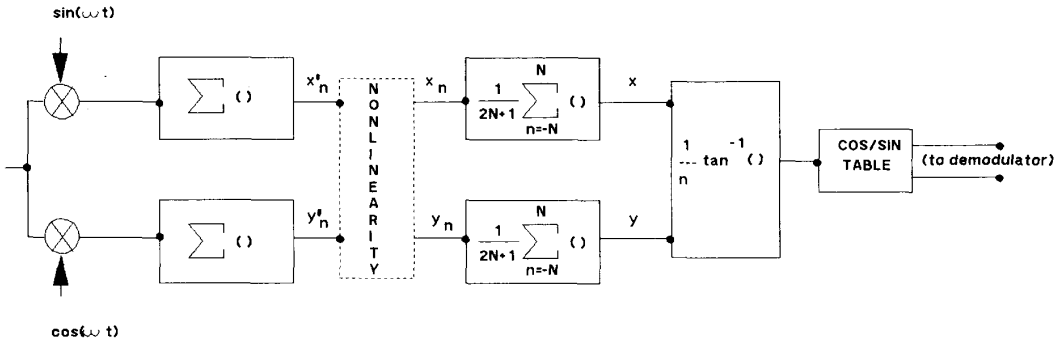


Fig. 5. General structure of nonlinear carrier phase estimator.

sional (complex) nonlinear function

$$x + y = F(a) * e^{jmp} \tag{12}$$

where

$$a = (x^2 + y^2)^2 \quad \text{and} \quad p = \tan^{-1}(y/x).$$

Thus, for each symbol we perform a rectangular-to-polar transformation, a phase multiplication by m, and an arbitrary nonlinear transformation on the module. Finally, we perform a polar-to-rectangular transformation on the result. We avoid describing the nonlinearity in that the practical implementation is a read-only memory, transforming a quantized two-dimensional vector into another such vector.

The implementation complexity of the proposed carrier phase estimator method can be derived as

$$Mv = R \text{ mults/sec}$$
$$Av = (N + 1) + R \text{ adds/sec} \tag{13}$$

where one useful sample per symbol is assumed.

In conclusion, it should be noted that the nonlinear estimation method of a QPSK-modulated carrier phase achieves good estimation accuracy, is less sensitive to a finite arithmetic implementation, and requires a definite (and short) acquisition time equal to NE = $(2N + 1)$ symbols.

The clock tracking system is based on an error detector which requires two samples per symbol. One of the two samples also serves for the symbol strobe (i.e., the sample on which the symbol decision is made). This method has been proposed in [15]. The algorithm is intended for synchronous, binary, and baseband signals, with approximately 40–100% excess bandwidth. The method presented is similar to the approach proposed in [16]. Its major points of differences are: 1) only two samples per symbol are employed, without explicit interpolation; 2) one sample coincides with the decision instant; and carrier signals are handled as well as baseband signals. Refer to Fig. 6 for a block diagram of a typical I–Q receiving modem. A passband signal is demodulated to baseband in a pair of quadrature-driven mixers. The phase of the local carrier must be adjusted to agree with that of the signal. The necessary carrier-recovery branch is omitted from the diagram and is irrelevant to the clock algorithm and discussion. Data filters are required; they perform receiver filtering to shape signal pulses, minimize noise, and suppress unwanted mixer products. Our interest is in sampled receivers. We do not specify the sampling points, other than the filter outputs which are available only in sampled form, as the pair of real sequences $\{y_I(\cdot)\}$ and $\{y_Q(\cdot)\}$. Timing information must be retrieved from these sequences. Symbols are transmitted synchronously, spaced by the time interval T. Each sequence will have two samples per symbol interval and the samples will be time-coincident between the sequences. One sample occurs at the data strobe time and the other sample occurs midway between data strobe times. The index r is used to designate symbol number. It is convenient to denote the strobe values of the rth symbol as $y_x(r)$ and $y_Q(r)$. As a formalism, we denote the values of the pair of samples lying midway between the $(r - 1)$th and the rth strobe as $y_I(r - 1/2)$ and $y_Q(r - 1/2)$. A timing error detector operates upon samples and generates one error sample $u_t(r)$ for each symbol. The error sequences are smoothed by a loop filter and then used to adjust a timing error corrector. The detector algorithm is shown in the following

$$u_t(r) = y_r(r - \tfrac{1}{2})[y_I(r) - y_I(r - 1)] + y_Q(r - \tfrac{1}{2}) \cdot [y_Q(r) - y_Q(r - 1)]. \tag{14}$$

This algorithm is suitable for both tracking and acquisition modes of operation. It is proven in [15] that $u_t(r)$ is independent of carrier phase, so that timing lock can be achieved without depending upon prior carrier phase acquisition. A physical explanation can be ascribed to (14). The detector samples the data stream midway between strobe locations in both the I and Q channels. If there is a transition between symbols, the average midway value should be zero, in the absence of timing error. A timing error gives a nonzero sample whose magnitude depends upon the amount of error, but the slope information necessary for the correction (lead or lag) is missing. To sort out the different possibilities, the algorithm examines the two strobe values on either side of the midway sample. If there is no transition, the strobe values are the same, their difference is zero, and the midway sample is rejected. (No timing information is available in the absence of a tran-

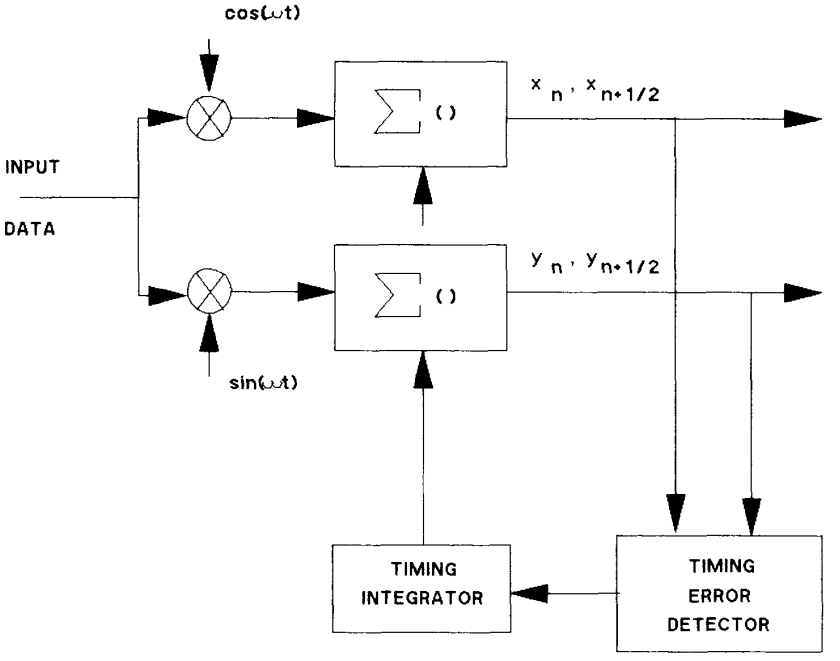


Fig. 6. Timing error detector scheme.

sition). If a transition is present, the strobe values will be different; the difference between them will provide slope information. The product of the slope information and the midway sample provides timing error information. It may be worthwhile to use the signs of the strobe values instead of the actual values. This eliminates the effects of noise. If all data filtering has been performed prior to the strobe point, then the sign of the strobe value is the optimum hard decision on the symbol and the algorithm effectively becomes decision-directed. This expedient is known to improve tracking capability. (But acquisition performance may suffer in a decision-directed operation.) Note that use of the strobe signs, instead of actual values, eliminates the need for actual multiplications in the algorithm—an attractive feature for digital processors. The decision-directed version of the algorithm is very similar to the digital transition tracking loop of Lindsey and Simon [17]. The implementation complexity for the timing error detector, including the interpolator filter used in [12], can be derived as

$$Mc = 16\ R \text{ mults\sec}$$
$$Ac = 16\ R \text{ adds\sec} \qquad (15)$$

where two samples per symbol has been assumed.

III. Architecture

The multicarrier demodulator has been designed using digital techniques. The main functions and algorithms are summarized in Fig. 7.

The FDMA signal sampled at Nyquist rate $(1/Tu)$ is fed to the demultiplexer that implements the "analytic signal" approach discussed above. This approach implies the application of two complex filters: the H filter, which interfaces directly with the FDMA signal, and the G filter which operates at lower rates. Since the G filter operation can be integrated with the spectral shaping performed by the demodulator, only the H filter is shown in the figure.

The 2H filter is followed by a downconverter which translates the complex bandpass output of the H filter (HLM) to a complex baseband signal (HL).

The HL data stream is then provided to the shaping filters in order to optimize the signal-to-noise power ratio. For aliasing reasons, the HL sampling rate $(1/Td)$ is three times the symbol rate $(1/T)$. However, at the output of the shaping filters, the aliasing is removed and a decimation is possible.

The shaping filters compute two complex samples per symbol (WBC and WBT) as required by the clock error detection algorithm. These samples, once the clock is correctly tracked, are taken at the center (WBC) and at the end (WBT) of the symbol. WBC consists of the pair (WBCI, WBCQ), while WBT has the pair (WBTI, WBTQ).

A clock error detector/integrator extracts from WBC and WBT a clock error signal that is integrated and used for timing correction, while the carrier phase detector block provides a carrier phase estimation (PE) extracted from the WBC samples, and subtracted via the phase corrector from the phase of WBC itself.

The output bits pair extracted form a signal called PB and is, in practice, the coupled signs of the WBC components after the phase correction.

The hardware implementation of the digital system was

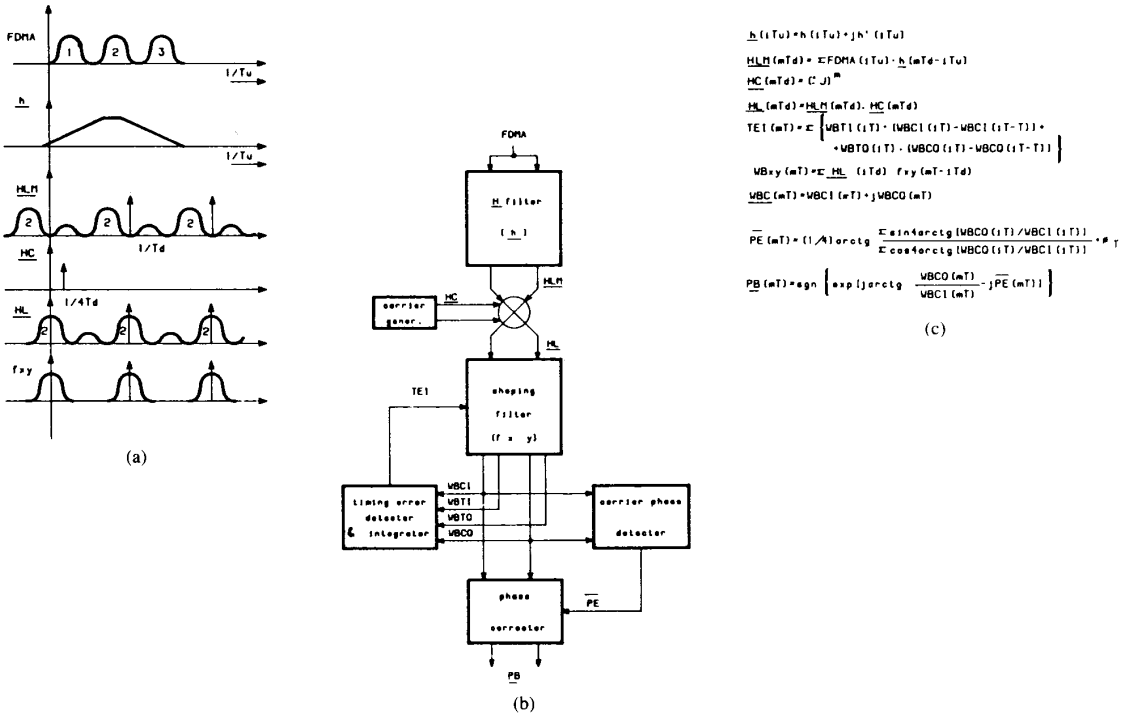


Fig. 7. Multicarrier demodulator. (a) Spectra. (b) Block diagram. (c) Algorithms.

developed to process an FDMA group with up to about 10 MHz bandwidth. The number of channels included in that bandwidth depends on the bit rates, but the system concept is able to process several bit rates and, as a consequence, different numbers of channels, provided that the overall bandwidth is respected and the channels within a group have the same bit rate. The influence of the number of channels is indeed relevant for hardware complexity, mainly in the demultiplexer portion, but this is due to the complexity of the algorithms that, for a given overall bandwidth, increase linearly with the number of channels to be demultiplexed.

The complexity of the demodulator is less dependent on the number of channels, in that the increase in complexity is mainly limited to the control circuity and to memories devoted to the storage of the different channel data.

For the selection of the architectures, the following criteria have been considered:

i) extensive use of parallel and pipeline processing concepts to support the large computation burden

ii) use of MSI and LSI general-purpose circuits to obtain a circuit easily transferable in ASIC's

iii) utilization of large chips, such as multipliers and memories, at maximum speed to optimize the hardware utilization

iv) selection of CMOS technology for all functions (and some interfaces from board to board) to limit power consumption.

The H filter consists of a FIR filter and is implemented as a parallel-out structure shown in Fig. 8 with four multiplier–accumulators (MAC) for HLQ signal computation and four for HLI computation. Each MAC provides a sequence of output samples at 1/4 the required rate, so that four MAC's provide four sequences which, suitably interleaved, give the correct output stream.

Having fixed the FDMA group bandwidth, the H filter architecture is valid bit rates from 137 Kb/s to 4.4 Mb/s, where the processing burden of each channel filter is a weak function of the bit rate.

Each MAC runs at 19.6 Msamples/second input rate and computes from a 12-tap filter for 4.4 Mb/s to a 384-tap filter for 137 Kb/s.

The filter coefficients are stored in suitable programmable read-only memories (PROM's). Several sets of coefficients for different channels and data rates have been included.

The H filter hardware also implements the downconverter and implementation is very easy in that it consists only of multiplication by a term of type $(i)^n$. Since this term has a period of $n = 4$ and four MAC's are used for the H filter, each MAC output must always be multiplied by the same factor $(+1, -1, +i, -i)$ and the implementation is only a matter of sign inversion and/or exchange of real and imaginary components.

The demodulator architecture is shown in Fig. 9. Like the demultiplexer, the demodulator is designed to meet the requirements of the same transmission rates. How-

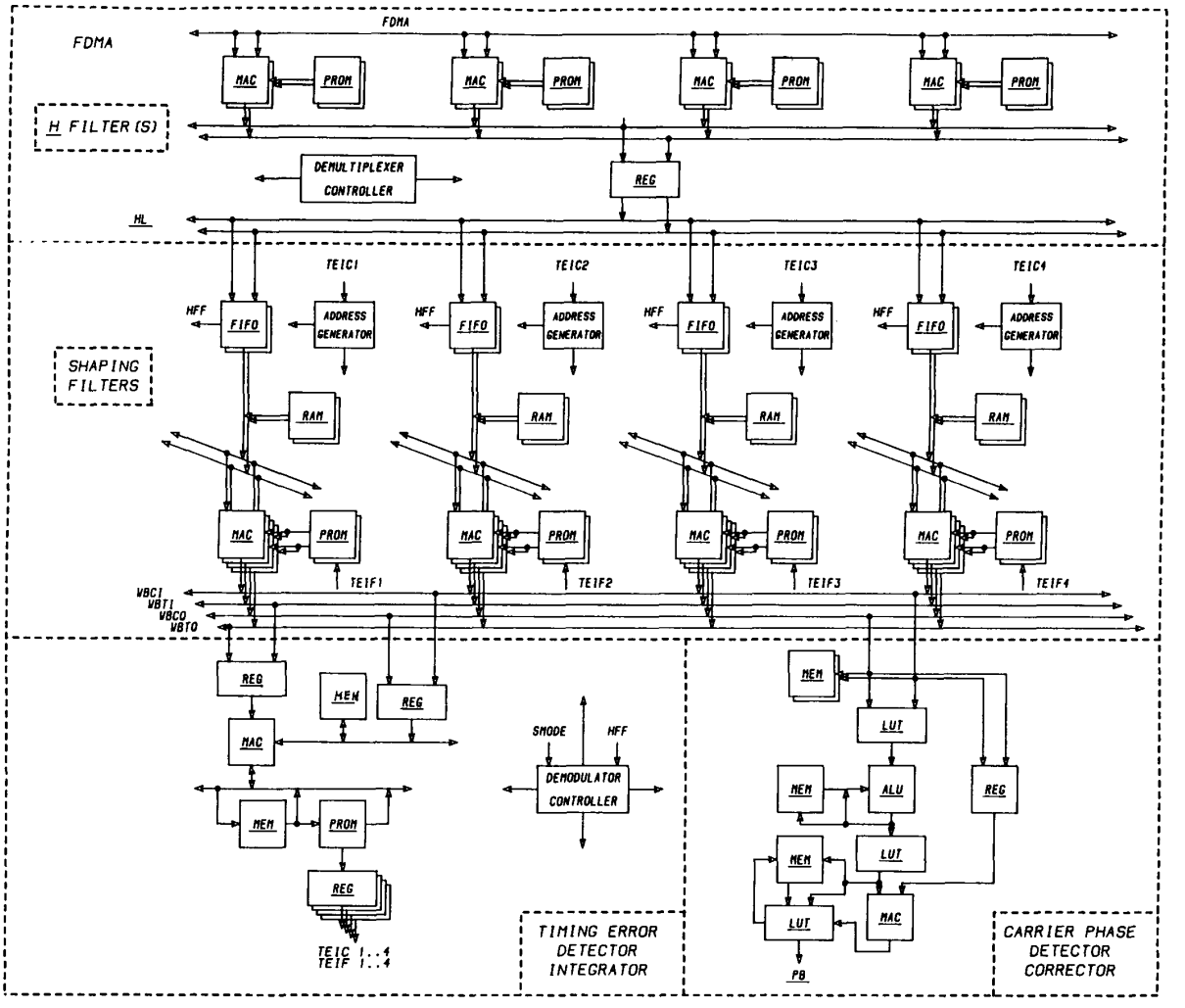


Fig. 8. Digital multicarrier demodulator.

ever, in this case the processing depends almost linearly on the bit rate so that a processor implemented for 4.4 Mb/s can be suitably rearranged in order to simultaneously process two channels at half the data rate, four channels at 1/4 the data rate, and so on.

The system is organized as a set of processing units specialized for the various demodulator functions. These units are coordinated by a demodulator controller in order to provide the synchronization of the activities and to optimize the hardware utilization.

The result of the synchronization is the data stream in the WBxy bus is composed of the interleaved sequences of the channel samples. In this way, as the number of channels increases (and the bit rate decreases) the overall data rate remains constant.

At the highest bit rate, the shaping filters require a multiplication rate that necessitates a parallel-out structure, as used for the H filters. In fact, four processing units working in parallel are used. At the lowest bit rates, the filters require only a fraction of a MAC processing capability. As a consequence, a programmable structure is required, where the MAC's operate in parallel at the highest bit rates and use time sharing at the lowest.

The units below the WBxy bus are devoted to the clock and carrier recovery functions. Since the processing burden required for these functions is smaller, the respective units are shared among the channels for all bit rates and their utilization is maximized.

Some multiplexers (MXR) at the output of the H filters are shown in Fig. 9. They are required for data routing. At 4.4 Mb/s, the same data stream of a single channel is addressed to all of the following processing units, which work in parallel to demodulate a single channel. In case the data rate is halved, two channels are routed toward the four units, which work in pairs on separated data. At 1.1 Mb/s or less, the multiplexers are arranged in such a way that four channels are routed to the four units, which then work independently.

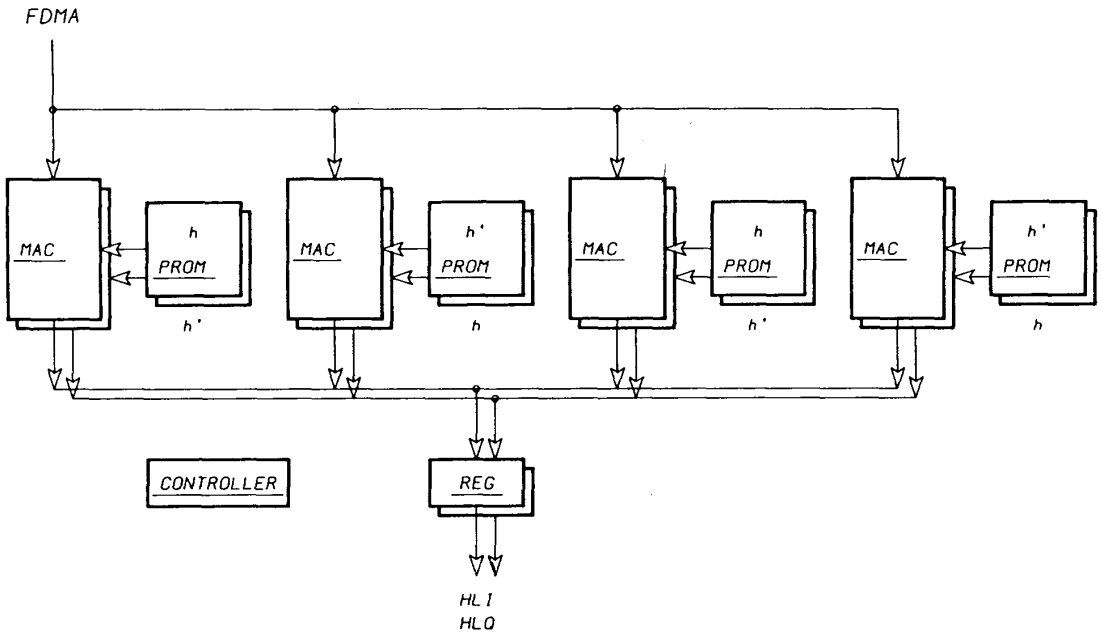


Fig. 9. *H* filter hardware.

Other important devices of the demodulator are data synchronizers. They reside in memory written at the output rate of the *H* filters and read at the input rate of the shaping filters. The output rate of the *H* filters depends on the channel bit rate; however, the input rate of the shaping filters is related to the aggregated bit rate, which is constant. The above memory is divided in two portions: a first in first out (FIFO) and a random access memory (RAM). A dual-port RAM with suitable addressing techniques is best suited.

Data synchronizers are equipped by suitable address generators, which work synchronously in the case of parallel processing and independently in serial processing. Four data synchronizers for the four processing units are implemented.

The data synchronizers are followed by the shaping filter blocks. The shaping filter consists of a 28-tap FIR filter, whose length is independent of the bit rate. The filter is implemented at 4.4 Mb/s as a parallel-out structure with four multiplier–accumulators (MAC) for each processing unit. One MAC per each WBxy data stream is required: it works at 15.7 MHz and performs 8×8 bit operations. As well as for the *H* filter case, in the case of 4.4 Mb/s, each MAC provides a data stream and four streams are interleaved. As mentioned above, at lower bit rates, the level of parallelism is reduced; in the case of data rates less than 1.1 Mb/s, it is converted to time sharing.

A demodulator controller generates most control signals. A number (several tens) of control signals are identified in order to synchronize the different units and subunits for parallel and pipeline processing.

The controller is essentially a microprogrammed structure with a counter which identifies several steps for the initialization of the carrier and clock recovery strategies.

The timing error detector and integrator implements a Type-1 loop and the Gardner algorithm for error detection. The hardware is based on a MAC for the error computation, RAM's for the storage of partial results, and a PROM for the loop gain definition and other control functions. The block provides two outputs: TEIF and TEIC, which are related to the integration of the timing error and are used to correct the timing at the level of shaping filters and data synchronizers, respectively.

Two kinds of timing corrections are required: a fine correction at steps smaller than the input sampling period, which is obtained by shifting the shaping filter response; and a coarse correction at steps of one input sampling period, which is obtained by modifying the input samples sequence of the shaping filter. The fine correction is obtained by addressing the TEIC signal to the PROM, which stores several sets of shaping filter coefficients. These sets differ from each other by the delay of sampling instants, which implies an equivalent delay in the output signal sampling instant.

The coarse correction is obtained from the TEIC data, which are fed to the data synchronizer. Depending on the TEIC value, the data provided to the shaping filter are shifted by one sample (anticipated or delayed) with respect to their nominal position. The resulting resolution of the algorithm is 1/24 of the symbol period.

In order to reduce the acquisition time and hangup effects in the presence of a suitable acquisition pattern (which can be important in the case of burst operation), an open loop procedure to estimate the sample nearest to the optimum is activated.

The carrier phase detector and corrector implements the phase estimator proposed by Viterbi [10] equipped by a suitable quadrant tracker, and performs the phase correction via I and Q components rotation. The unit is based on a RAM for the storage of the input data to be provided to the mean value (15-tap) filters, a RAM for the computed mean values of I and Q components, a RAM for the corrected symbol, an arithmetic logic unit (ALU) for mean values computation, lookup tables (LUT's) for the nonlinearities (I and Q components after phase multiplications by 4 and by 1/4, quadrant tracking), and a MAC for phase correction. The main output of this processor is the stream of the recovered bit pair (PB).

In order to evaluate the above systems, a proof-of-concept prototype has been implemented and extensive tests have been performed. It is aimed at verifying the feasibility of the most relevant MCD aspects within the context of the current technology. As a consequence, the proof of concept actually implemented a subsystem that extracts and demodulates one channel out of a set of three adjacent ones. A single 4.4 Mb/s channel or a single 1.1 Mb/s channel out of a 10 MHz (i.e., three channels for 4.4 Mb/s or 12 channels for 1.1 M/s) bandwidth was implemented.

The proof of concept was derived from the complete system by simplifying or eliminating some circuits. First of all, since the MCD demodulates a single 4.4 Mb/s channel, a single H filter has been developed, with several sets of coefficients, in order to select a specific channel out of three. Furthermore, for the demodulator, memories and related address generators for different channel parameters were suppressed.

IV. Test Results

Tests were identified to evaluate the MCD breadboard performances. The complete set was applied to the central channel of each three-channel group processed by the MCD, while some tests were also performed on the other channels. At 4.369 Mb/s, up to three channels numbered from 1 to 3 can be processed. The central channel is the number 2. At 1.092 Mb/s, a 12-channel capacity is foreseen. The channels are numbered from 1 to 12, where the 3rd, 4th, and 5th channels can be processed. The central channel is now number 4.

All tests were performed under the following conditions, unless otherwise stated:

- central channel
- nominal frequencies
- pseudorandom data
- Viterbi's algorithm filter length = 15
- nominal bit clock recovery loop bandwidth.

The tests included:

- implementation loss
- loss versus carrier frequency offset
- loss versus clock frequency offset
- loss versus wordlengths
- loss versus amplitude variation
- loss versus adjacent channel interference
- acquisition time
- power consumption.

A. Description of Test Bed

The MCD Test Bed setup, used to measure the BER performance of the MCD breadboard, is shown in Fig. 10.

An HP 3325 A synthesizer provides the required clock signal to an HP 3762 A data generator. This produces the data sequence and clock which are fed to the FDMA generator for modulation of the central channel. Adjacent channels are modulated by a pseudorandom data generator. The ALCATEL synthesizers and FDMA signal generator produce the required IF carriers of about 140 MHz which are modulated by input data. It can produce a maximum of three modulated carriers simultaneously. The HP 3708-A Noise Test Set is used to introduce noise in the channel under test, and to perform E_b/N_o measurements.

The demodulated serial I and Q data and the recovered clock signal are sent to the HP 3763-A Error Detector for a BER test. An RMS voltage meter is used to monitor the baseband output amplitude of the MCD.

A digital-to-analog converter and oscilloscope (not shown in Fig. 10) are used for acquisition time measurements.

B. Implementation Loss

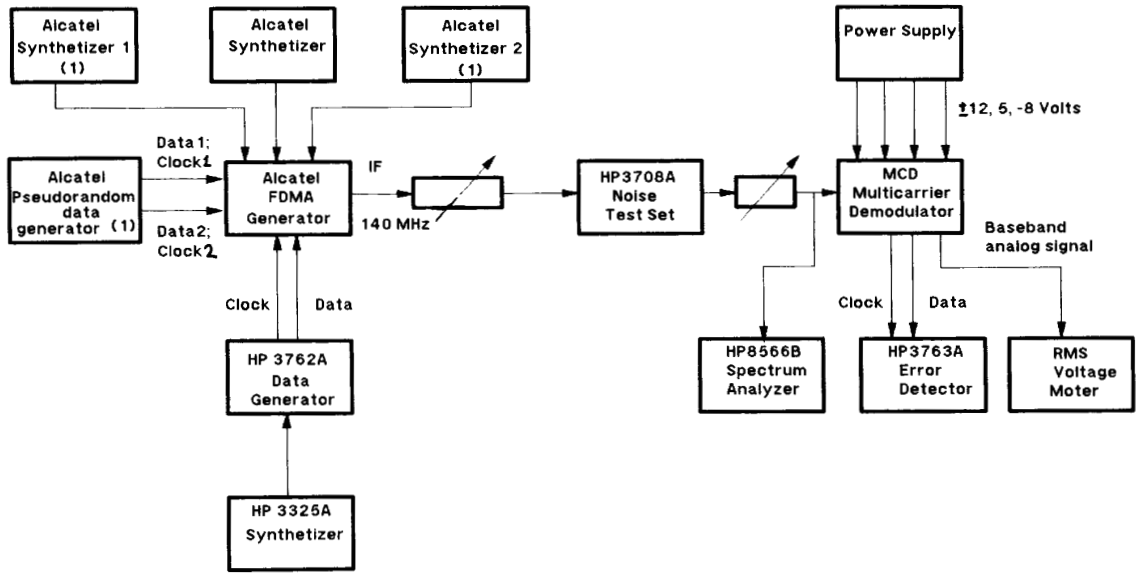
Fig. 11 shows the implementation losses in condition of nominal values for the system parameters.

From the results, we can observe that

- in the case of bit rate = 1.1 Mb/s, the MCD performances of channels 3 and 4 are very similar
- for the 4.4 Mb/s case, the MCD performance for channel 2 is better than the other two edge channels, in that channels 1 and 2 suffer from relevant distortions from antialiasing filtering. However, the additional loss of the edge channels is limited (less than 0.7 dB for all cases)
- E_b/N_o values under 7 dB have been excluded since, at these values, the carrier recovery technique suffers significantly from cycle slip problems. For these values, data-differential encoding/decoding becomes necessary.

C. Loss Versus Carrier Frequency Offset

The sensitivity to the carrier frequency offset is shown in Table III. The extra loss is negligible for carrier frequency offsets within 80% of the frequencies recalled in the table, and then increases very rapidly. The performances of the tree channels are similar. The carrier frequency offset range without noise is approximately doubled when reducing the filter length from 15 to 7, but remains nearly unchanged at $E_b/N_o = 10$ dB. At filter length 7 and $E_b/N_o = 8$ dB, the cycle slip problem is present.

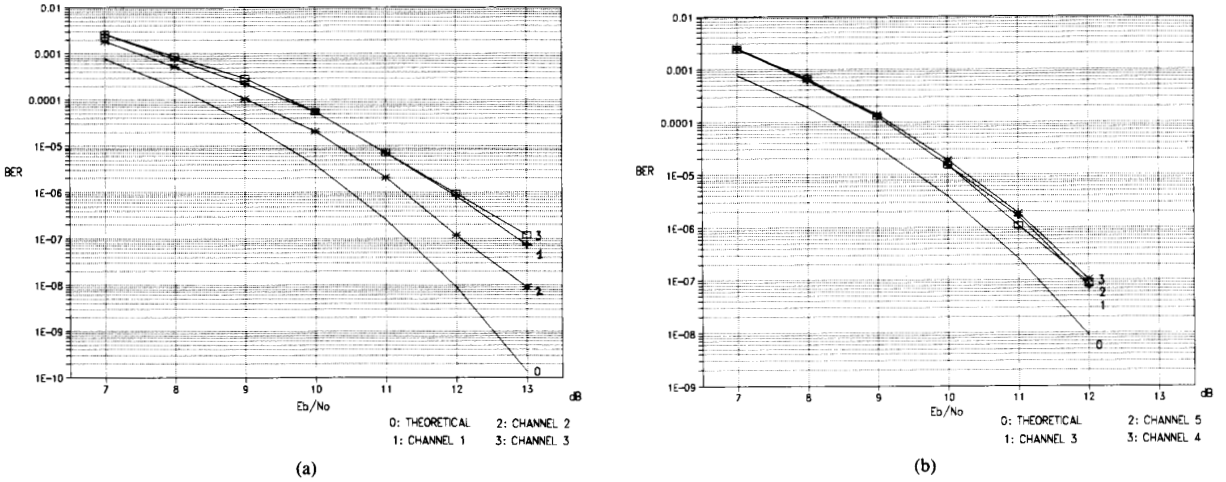


(1) Only for test of adjacent channels interference.

Fig. 10. Test setup for MCD BER test.

TABLE II
LOSS VERSUS E_b/N_o

E_b/N_o (dB)	Loss (dB)					
	Bit Rate = 4.4 Mb/s			Bit Rate = 1.1 Mb/s		
	Channel 1	Channel 2	Channel 3	Channel 3	Channel 4	Channel 5
7	1.1 ;SL	0.75 ;SL	1.1 ;SL	1.0 ;SL	1.05 ;SL	1.0 ;SL
8	1.0 ;SL	0.7 ;SL	1.1 ;SL	0.8 ;SL	0.85	0.9
9	1.1	0.65	1.3	0.75	0.8	0.75
10	1.25	0.75	1.25	0.6	0.7	0.6
11	1.25	0.75	1.25	0.65	0.7	0.5
12	1.4	0.75	1.45	0.6	0.7	0.7
13	1.6	1.0	1.75			



(a) (b)

Fig. 11. MCD performances at: (a) 4.4 Mb/s and (b) 1.1 Mb/s.

TABLE III
FREQUENCY OFFSET RANGES

Data Rate (Mb/s)	E_b/N_o (dB)	Experimental Values (KHz)	
		$2N + 1 = 15$	$2N + 1 = 7$
4.369	HIGH	26	43
	10	15	16
	8	15	SLIPS
1.092	HIGH	7.5	14.4
	10	4.0	3.5
	8	3.5	SLIPS

D. Loss Versus Clock Frequency Offset

An example of degradation behavior dependent on the clock frequency offset is shown in Fig. 12 for 1.1 Mb/s, E_b/N_o = 10 dB, and three loop bandwidths; there is no relevant difference from channel to channel.

It has been verified that the clock frequency range is highly sensitive to the signal amplitude, in that the loop bandwidth depends on the open loop gain. In fact, a 25% increase of the clock frequency range has been measured when the noisy baseband signal amplitude is increased by 10%.

E. Acquisition Time

The acquisition time has been defined as the time required by the timing error of the bit clock recovery loop to decrease from the initial error to the steady-state value within one correction step (1/24 of the symbol period). The timing error is observed on an oscilloscope by converting digital data (TEIC, TEIF) into an analog signal by a digital-to-analog converter.

Measurements have been carried out in different conditions: pseudorandom and alternate data, E_b/N_o = 8 dB and without noise, two different bit rates, and two different values of loop bandwidth.

For each condition, the worst case over about 50 measurement repetitions are collected in Table IV.

F. Loss Versus Word Lengths

An additional MCD loss has been measured when limiting the quantization bits number of data and filtering coefficients of one of the following sections: *H* filter, data synchronizer and shaping filter, carrier phase estimator, and clock error detector. Word lengths have been reduced by suppressing LSB's. The additional loss is referred to as the nominal situation, i.e., to the following quantization levels:

- 8 bits for the *H* filter, synchronizer, shaping filter, and accumulator of the carrier phase estimator;
- 6 bits elsewhere.

Experimental results are presented in Table V. The table shows an increasing loss at the increase of E_b/N_o, where the quantization error dominates the noise effects. The *H* filter and clock error detector are less sensitive to the quantization bits number, and the shaping filter is the most sensitive unit.

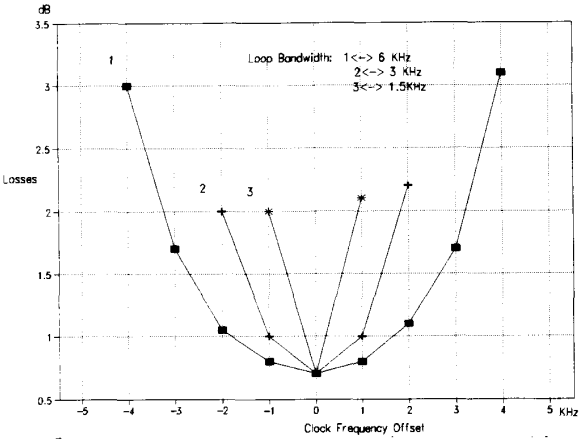


Fig. 12. MCD losses versus clock frequency offset (1.1 Mb/s, E_b/N_o = 10 dB).

TABLE IV
CLOCK RECOVERY ACQUISITION TIME

Data Rate (Mb/s) & Type	E_b/N_o (dB)	Experimental Values (Symbols) For Loop Bandwidths of	
		6 KHz	3 KHz
4.369	HIGH	100	200
ALTERNATE	8	130	260
4.369	HIGH	500	870
PN	8	500	1300
1.092	HIGH	40	80
ALTERNATE	8	80	150
1.092	HIGH	130	220
PN	8	300	440

G. Loss Versus Baseband Noisy Signal Amplitude Variation

The loss variation is smaller than 0.3 dB when measured at E_b/N_o = 10 dB and the baseband noisy input signal ranges from 225 mVrms to 375 mVrms at 4.4 Mb/s, and from 150 mVrms to 275 mVrms at 1.1 Mb/s. But the performance degrades rapidly outside this window, so that an automatic gain control system is needed in case a dynamic range higher than 5 dB is required.

The loss versus baseband signal amplitude performances for the three channels are very similar.

H. Loss Versus Adjacent Channel Interference (ACI)

The degradation due to the ACI interference increases the loss up to 1.9 dB when $C/I = -6$ dB at 4.4 Mb/s, and 0.2 dB when $C/I = -6$ dB at 1.2 Mb/s.

I. Power Consumption

Table VI recalls the details of the breadboard power consumption. The breadboard uses Advanced CMOS

TABLE V
ADDITIONAL LOSS VERSUS THE WORD LENGTHS

Word Lengths (Bits)	H-H^1 filters			Synchronization and Matched Filter			Carrier Phase Estimator			Bit Clock Recovery Loop		
	ΔL (dB) @ E_b/N_o (dB)											
	8	10	12	8	10	12	8	10	12	8	10	12
8	0	0	0	0	0	0	0	0	0	/	/	/
7	0	0	0	0.2	0.2	0.3	0.1	0.1	0.1	/	/	/
6	0	0	0.4	0.3	0.6	1.1	0.2	0.2	0.3	0	0	0
5							0.8	0.9	1.3	0	0	0.1
4										0	0	0.15
3										0	0.1	0.2
2										0.1	0.15	0.4
1										0.4	0.9	∞

Bit rate = 1.092 Mb/s

TABLE VI
POWER CONSUMPTION AT 4.4 Mb/s

UNIT	WATTS
Analog input interface	10.6
Analog-to-Digital Converter	10.8
H filter	6.4
Demodulator	12.6
TOTAL	40.4

TABLE VII
TECHNOLOGIES COMPARISON

Technology	Transmission Rate		Maximum Number of Channels at Rate		Parameters for a 4.4 Mb/s MCD		
	MIN (b/s)	MAX (b/s)	MIN	MAX	Channels (N)	Power (W)	Weight (Kg)
Digital Standard Chips	137 K	4.4 M	96	3	3	80	15
Digital Semicustom CMOS	137 K	4.4 M	96	3	3	13	1
Integrated Acoustooptic	3.2 M	4.4 M	36	24	24	15	1.5
Surface Acoustic Waves	137 K	4.4 M	60	22	22	40	7

Logic (ACL) circuits except for interfaces, which are bipolar. The extra consumption due to bipolar circuits is estimated to be about 15%.

It is worth noting that the breadboard demodulates a single channel but, for a complete MCD, some circuitry (e.g., analog interface and AD converter) does not need to be replicated. As a consequence, the power consumption expected for a complete MCD at 4.4 Mb/s can be obtained by just adding to the 40.4 W of the breadboard, an additional 4.4 W for two more H filters and demodulators. The result will be then 74.8 W. In the case of 1.1 Mb/s, we should add 11 H filters and two demodulators to obtain 136 W power consumption.

V. CONCLUSIONS

Table VII compares the multirate DSP implementation discussed here with some alternative technologies appli-

cable, at least in principle, to IBS services (137 kb/s to 4.369 Mb/s), i.e., surface acoustic wave (SAW) chirp Fourier transform (CFT) processing and integrated acoustooptics (IAO). SAW CFT multicarrier demodulation can be seen to cover the entire range of IBS data rates with substantially lower dc power consumption compared to the others, including the present DSP solution. However, problems remain with SAW chirp filter size. Several centimeters of circuit space and temperature variation in piezoelectric substrates (94 ppm/°C with LiNbO3), tend to modify the CFT performance. Furthermore, SAW chirp devices, although utilized in military applications, are not yet qualified for space-born utilization.

In summary, this paper has addressed the design and implementation problems related to space-born multicarrier or "group" demodulation (MCD) of a large number of low-to-moderate data rate signals (137 kb/s to 4.369 Mb/s), relevant to (INTELSAT) business services (IBS) exchanged via (regenerative) FDMA (uplink)/TDM (downlink) communication satellites.

Several techniques/technologies have been investigated: digital signal processing, surface acoustic wave devices implementing chirp Fourier transform and integrated optics. Among them, the present paper has illustrated the multirate DSP solution. Mass/dc power budgets for some representative data rates have been indicated, and a comparison has been made with some alternative MCD technologies.

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Daniel Rousset, photograph and biography not available at the time of publication.

Enrico Saggese, photograph and biography not available at the time of publication.