A NANOCHANNEL FABRICATION TECHNOLOGY WITHOUT NANOLITHOGRAPHY

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ABSTRACT

We have developed a new nanochannel fabrication technique using chemical-mechanical polishing (CMP) and thermal oxidation. With this technique, it is possible to control the width, length, and depth of the nanochannels without the need for nanolithography. The use of sacrificial SiO_2 layers allows the fabrication of centimeter-long nanochannels. In addition, the fabrication process is CMOS compatible. We have successfully fabricated an array of extremely long and narrow nanochannels (i.e. 10 mm long, 25 nm wide and100 nm deep) with smooth inner surfaces.

Keywords: Nanochannel, bionanotechnology, CMP, oxidation

1. INTRODUCTION

Nanofabrication of extremely small fluidic structures provides powerful tools for the field of bionanotechnology [1-3]. Nanochannels are essential components in nano-fluidic system. Among the many requirements for the nanochannel fabrication technique are the following: It should be cost effective, able to precisely control channel dimensions, and CMOS-compatible for ultimate integration with microelectronics. Previously, various nanochannel fabrication techniques based either on e-beam lithography, step sidewalls, and laser machining has been reported [4-6]. However, these techniques suffer from several limitations. For example, e-beam lithography-based processes are relatively expensive [4]. The step sidewall approach has limitations in the maximum possible lengths of the nanochannel because of lateral sacrificial etching effects [5]. Finally, laser machining can only produce nanochannels with minimum widths in the range of a few hundred nanometers and the fabrication process is not CMOS compatible [6].
In this paper, we describe the demonstration of a cost-effective nanochannel fabrication technique with precisely controlled dimensions, using a conventional CMOS fabrication process.

2. EXPERIMENTAL

The fabrication process is shown schematically in Figure 2. First, an amorphous silicon layer is deposited over a low-stress silicon nitride film. The Si layer is patterned and etched using RIE. Subsequently, it is oxidized at 1000°C in a dry O_2 ambient. The ultimate

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width of the nanochannel is essentially controlled by adjusting the resulting oxide film thickness [6]. Dry O_2 based oxidation is a well controlled process that can produce SiO_2 films with thickness as low as 5 nm. Figure 1 shows the experimental data obtained for nanochannel width versus oxidation time. The width of the nanochannel is a well behaved monotonic function of the oxidation time.

The depth of the nanochannel is determined by the thickness of the amorphous silicon film. The total length and any meanders in the nanochannels are controlled by the photolithography process. Subsequently, an overlayer of amorphous silicon is deposited on the oxidized film. The overlayer thickness is approximately five times that of the amorphous silicon layer, in order to minimize "dishing" effects. Next, a Chemical Mechanical Polishing (CMP) step is conducted to thin the overlayer down to the oxide layer.

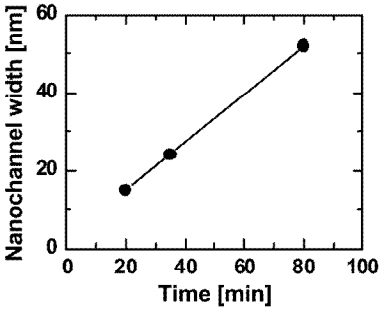


Figure 1. The width of the nanochannel (after removal of the sacrificial oxide) is plotted versus oxidation time for amorphous silicon in 1000°C dry O_2. As seen above it is possible to have nanometer-level precision in channel width through this process.

The slurry used for the CMP process is Chemlox which has about 20:1 selectivity between silicon and silicon dioxide. Following the CMP step, the vertical oxide layer between the amorphous silicon layers is etched in a (10:1) Buffered Oxide Etch (BOE) solution for 20 min. Since this oxide layer is fully exposed (no covering layer to "burrow" under) even a 10 mm long channel takes just 20 min for complete etching. Figure 3 (a) contains scanning electron micrographs of an array of nanochannels after the oxide etch process. A higher magnification image shows a single nanochannel with a width of 50 nm(Figure 3 (b)). The processing also yields smooth inner surfaces for the nanochannels. The surfaces of the nanochannels can be changed from hydrophobic to hydrophilic by means of an additional oxidation step prior to "sealing". It should be noted that during this oxidation step, the nanochannels become even narrower due to the growth of the oxide on the sidewalls. Finally, the nanochannels can be sealed by depositing an overlayer of evaporated gold or PECVD SiO_2. SiO_2 sealing is very attractive option for biomedical applications, because the oxide can serve as a transparent window for

fluorescence detection schemes. The sealing process also results in a reduction of the nanochannel widths due to sidewall deposition. Scanning electron micrographs of Au sealed (Fig. 4) and PECVD oxide sealed (Fig. 5) are shown.

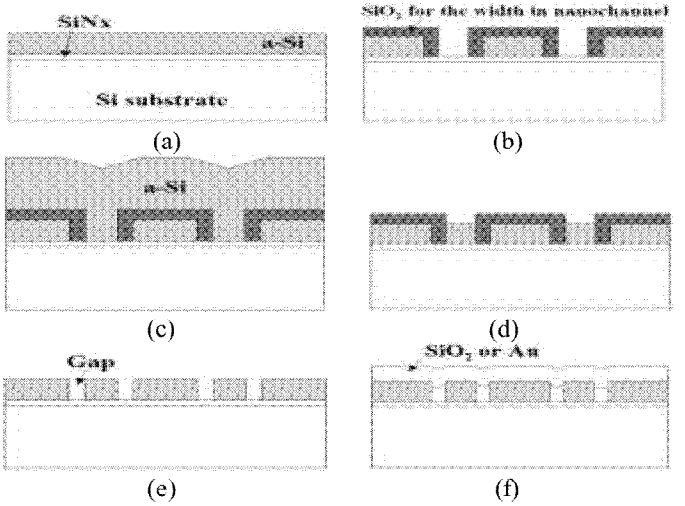
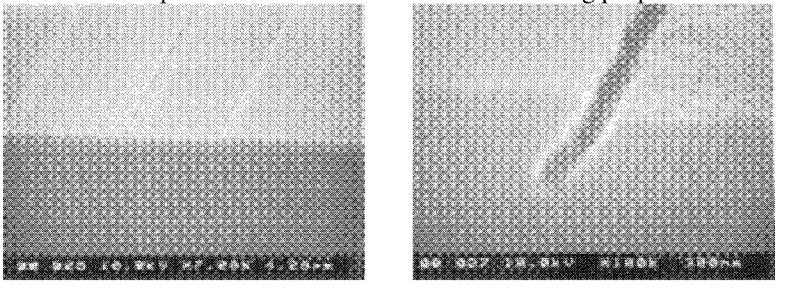
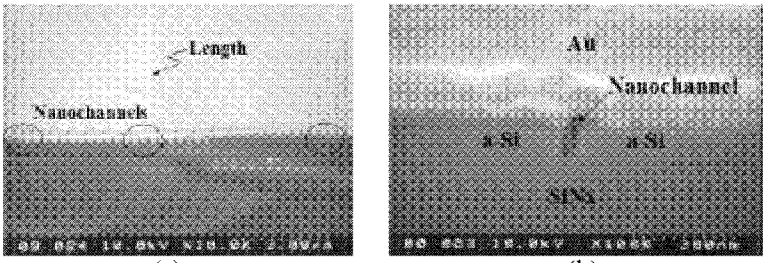


Figure 2 (a) The first step is the deposition of a silicon nitride layer followed by an amorphous Si layer (b) The amorphous Si layer is then lithographically patterned, followed by reactive ion etching (RIE) and dry oxidation to create a sacrificial oxide layer with the desired nanochannel width (c) An amorphous Si layer is subsequently deposited over the patterned structure (d) The amorphous Si layer is thinned using Chemo Mechanical Polishing (CMP) until the sacrificial oxide layer is exposed. (e) The oxide layer is then etched away, creating a nanometer-sized channel. (f) Finally, either an overlayer of either Au or oxide is deposited over the nanochannel for sealing purposes.



(a) (b)

Figure 3. (a) Scanning electron micrographs of an as-etched nanochannel array (b) a higher magnification view of a single nanochannel. The width of the nanochannel is approximately 50 nm.



(a) (b)

Figure 4. (a)Scanning electron micrograph of a nanochannel array with a Au "sealing" overlayer. (b) Higher magnification view of a single, 50 nm wide nanochannel.

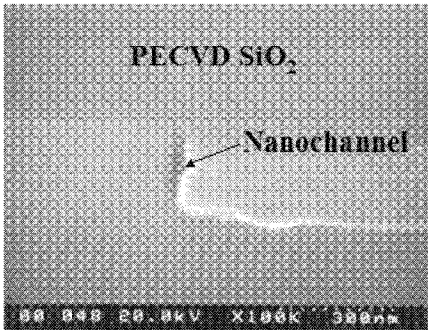


Figure 5. Scanning electron micrograph of a single, 25 nm wide, nanochannel with a PECVD SiO_2 sealing layer. The inner surfaces of the nanochannel are hydrophilic because of the oxide coating on the sidewalls.

4. RESULTS AND DISCUSSION

We have successfully fabricated nanochannel arrays without the use of nanolithograph. Figure 4 (a) contains a scanning electron micrograph of the Au-sealed nanochannel array. The Au overlayer is evaporated using an e-beam evaporation process. Figure 4 (b) shows a magnified view of a single, 50 nm wide nanochannel. The nanochannel is tilted due to lateral etching in the RIE process. The inner surfaces of the nanochannel are hydrophobic since they consist of amorphous silicon. Figure 5 shows a magnified view of a nanochannel sealed with PECVD oxide. The width of the nanochannel is about 25 nm. The narrowing of the nanochannel is caused by the deposition of PECVD oxide on the sidewalls. In addition, the oxide coating renders the inner surfaces of the nanochannel hydrophilic. Compared to the conventional technologies our proposed

technique is capable of making nanochannels that are a few tens nanometer wide, in a cost-effective manner, without the use of nanolithography. There is also no limitation in the nanochannel lengths and the number of meanders. Finally, our process is CMOS-compatible.

5. CONCLUSIONS

We have successfully demonstrated a cost-effective, CMOS compatible, nanochannel fabrication technique capable of producing nanochannels with widths as short as 25 nm. The width, depth, and length can be precisely controlled by the combination of thermal oxidation, deposited amorphous silicon film thickness, and standard photolithography, respectively. The sacrificial SiO_2 layer is etched prior to the nanochannel being sealed, allowing for easy removal of the sacrificial oxide and thus have no limitations on their lengths.

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