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A Neuromorphic Device for Detecting High-Frequency Oscillations in Human iEEG

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Abstract—Among diagnostic biomarkers, high frequency oscillations in human iEEG are used to identify epileptogenic brain tissue during epilepsy surgery. However, current methods typically analyse the raw data offline using complex time-consuming algorithms. We developed a compact neuromorphic sensory-processing system-on-chip that can monitor the iEEG signals and detect high frequency oscillations in real-time using spiking neural networks. To this end, we present an integrated device with an analog front-end that can extract predefined spectral features and encode them as address-events, and a neuromorphic processor core that implements a network of integrate and fire neurons with dynamic synapses. The device was fabricated using a standard 0.18 μm CMOS technology node. The estimated power consumption of the front-end is 6.2 $\mu\text{W}/\text{channel}$ and the area-on-chip for a single channel is 0.15 square millimetres. The SNN classifier provides 90.5% sensitivity and 67.7% specificity for detecting high frequency oscillations. This is the first feasibility study towards identifying relevant features in intracranial human data in real-time on-chip using event-base processors.

Index Terms—Electrophysiological signals, Neural-recording, Event-based processing, Epilepsy, intracranial EEG, Biomarker

I. INTRODUCTION

In surgical treatment of patients with epilepsy, High Frequency Oscillation (HFO) are among biomarkers for the epileptogenic zone [1]. These patterns can be detected in intracranial electroencephalography (iEEG) and aid clinical decisions during epilepsy surgery [2]. In current practice, HFO detection requires storing iEEG for off-line reconstruction and data-analysis on standard computers. This demands high signal acquisition quality, in terms of amplifier Signal to Noise Ratio (SNR), alongside with high-resolution Analog to Digital Converter (ADC) of up to 24 bits [3].

The diagnostic application of HFO would benefit from on-chip and on-line processing. The requirements on ADC bandwidth and resolution can be relaxed by employing multiple detection frequency bands as long as the SNR is sufficient for HFO detection.

In this setting, we propose a neuromorphic device with a front-end signal conditioning stage optimized to detect HFO with minimum power consumption and layout area requirements. Specifically, we present a System-On-Chip (SOC) solution comprising eight analog front-end modules, a multi-core Dynamic Neuromorphic Asynchronous Processor (DYNAP) block [4], and full custom interfacing and biasing blocks integrated in standard 0.18 μm fabrication technology. The front-end amplifies the bio-signals, filters them in specific

frequency bands and converts filter outputs to asynchronous events. The DYNAP block is configured to implement a spiking neural network which receives these events, processes them via its dynamic synapses and neurons, and detects HFO in two different frequency bands.

Since in our approach signal processing is performed on-chip in an end-to-end manner, the stringent requirements that are common for biomedical recording devices are not necessary, provided that the extracted information is sufficient to ensure robust classification.

In Section II we present the building-blocks and diagrams of the analog front-end circuits. In Section III we describe the spiking neural network used for classification, including its training and test procedures, and in Section IV we provide the specifications of the analog front-end circuits, obtained from circuit-level simulations, and neural network classification results on human iEEG data.

II. ANALOG FRONT-END

The analog front-end comprises a Low-Noise Amplifier (LNA), three analog filters and four asynchronous ADCs per channel as shown in Fig. 1(a). The amplifier output is filtered using one low-pass and two band-pass Tow-Thomas second-order filters. Filtered signals as well as the amplified wide-band data are converted to events using asynchronous ADCs [5]. The presented structure is employed alongside with a configurable bias-generator [6] and an address-event representation encoder interfaced to the event-based neuromorphic processor core. The neuromorphic processor core block is based on the design presented in [4]. The layout of front-end and processor core is shown in Fig. 2.

A. Low-Noise Amplifier

The LNA is the most critical block employed in the front-end, which ensures linear amplification and systematic noise suppression. It includes an Operational Transconductance Amplifier (OTA) in capacitive feedback configuration with MOS-Bipolar structure as resistive elements [7].

The LNA structure is desirable for physiological recordings since input coupling capacitors not only reject the inappropriate DC component of the input signals but also present a degree of freedom for gain adjustment. Thanks to the extremely large impedance introduced by using MOS-Bipolar elements ($\approx \times 100 \text{ G}\Omega$), input and feedback capacitors are within reasonable area limitations to be implemented on chip.

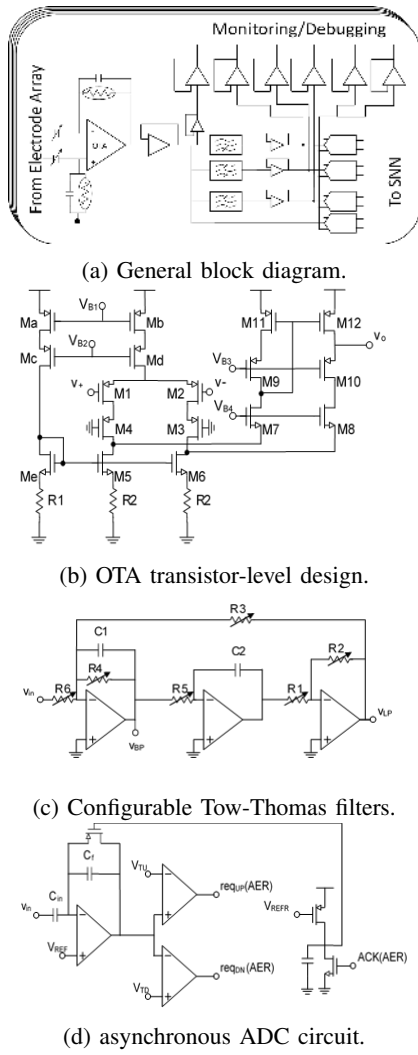


Fig. 1: The analog front-end circuit schematics.

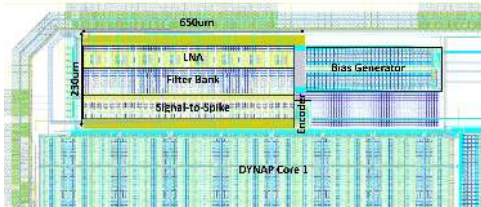


Fig. 2: Physical layout of analog front-end and peripheral circuits alongside with the adjacent DYNAP core

This configuration results in a band-pass frequency response with sub-Hertz lower cutoff frequency making it capable of faithful signal acquisition with minimal baseline distortion.

To confront channel mismatch, an inevitable issue in multi-channel recordings due to electrode placement and fabrication inconsistency, the amplifier employs digitally adjustable gain, which prevents output-node saturation and signal loss.

The OTA employed in this design is a modified folded-cascode amplifier [8] as shown in Fig. 1(b). The design features power efficient biasing scheme for input differential

pair and low flicker noise that is the dominant term in the lower physiological frequency range (10-100 Hz). This is achieved by suppressing the noise generated by NMOS current mirrors implemented in traditional folded-cascode input stage, by implementing source degeneration resistors.

B. Analog Filters

The implementation of the low-pass active filter is shown in Fig. 1(c). It comprises multiple op-amps configured as a Tow-Thomas resonating filter. This circuit consists of a damped inverting integrator, cascaded with another undamped integrator, and an inverter with feedback applied around the entire structure, while $R4$ is optimized for the feedback loop to be stable. An advantage of this circuit, not commonly found in other active integrated realizations, is that it offers independent tuning of quality factor and center frequency [9]. This configuration is chosen over less sophisticated 2nd order counterparts mainly because of the degrees of freedom it provides for fine tuning in case of channel mismatch. Moreover, the architecture presents both low-pass and band-pass outputs without major changes in design layout. It is thus desirable for having an isometric multi-band filter structure layout. The configuration shown in Fig. 1(c) is realized using metal-insulator-metal capacitors and tunable double-PMOS pseudo resistors.

C. Asynchronous ADC

The asynchronous ADC enables the analog front-end to interface with the event-based processing core and translates the input data to a sequence of spikes. Here, each spike corresponds to a polarized, adjustable amount of change in the analog input signal [5]. Depicted in Fig. 1(d), this block comprises an adaptive feedback amplification stage and a set of comparators forming a clock-less delta-modulator that generates “UP” and “DOWN” spikes in response to an adjustable amount of increase/decrease in the signal amplitude. The voltages V_{tu} and V_{td} are thresholds for generating the UP and DOWN spikes. The bias V_{refr} controls the refractory period during which the ADC stays dormant after generating a spike. These three voltages are hyper-parameters that can be optimized to achieve high reconstruction accuracy or block background noise depending on the application. They also determine spike generation rate.

III. SPIKING NEURAL NETWORK (SNN) ARCHITECTURE

To verify that an SNN can indeed reliably perform HFO pattern recognition, we built a simple network that uses spikes generated by the analog front-end as input for a single layer of Integrate-and-Fire (I&F) neurons that project to an output node. The latter is trained as a binary classifier to decide whether the input spike train contains HFO traces within a time window, which we chose according to the typical duration of an HFO event.

We trained the output node via a supervised logistic regression method. The training dataset was taken from the iEEG data [10] described in [1]. This dataset was recorded, as a part of the pre-surgical evaluation, from 20 patients with

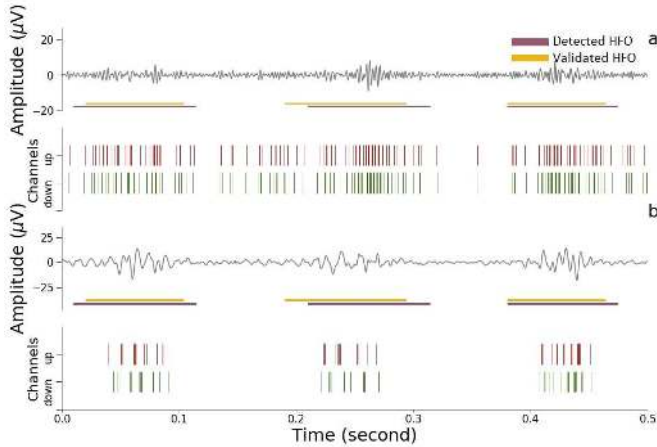


Fig. 3: Three HFO snippets from the iEEG training dataset filtered in (a) FR band and (b) Ripple band. The UP and DOWN spikes accumulate during the HFO. The time windows with detected HFO activity (purple marks) overlap with the validated HFO taken from [1], [10] (golden marks).

intractable epilepsy, 13 of which achieved seizure freedom after epilepsy surgery. This dataset contains validated HFO that predict postsurgical seizure freedom with 57% sensitivity and 100% specificity [1]. To create the iEEG training set, we concatenated a selection of data from [10] into snippets that contained validated HFO embedded in 50 ms baseline activity.

A. HFO detector training/testing procedure

The raw iEEG training data set was filtered in two bands of interest, 80-250 Hz (Ripple band) and 250-500 Hz (Fast Ripple (FR) band) and fed into the ADC, resulting in 4 spike trains (as described in Section II-C). To train the neural network and evaluate its performance, we iteratively divided the data snippets in training (80%) and test (20%) sets and adopted a 20-80% model cross-validation scheme.

In the training phase, the output node was trained using logistic regression. In this particular classification problem, we first calculate the neurons' mean firing rate in the single layer over adjacent time windows of 45 ms. The extracted firing rate of UP and DOWN neurons in FR and Ripple bands were used as "features" for the logistic regression algorithm, in which the validated HFO were the teacher signal. After training, the algorithm should classify whether a time window contained a HFO (output value 1) or baseline (output value 0). Fig.3 presents a classification example for the test set.

To quantify the performance of our HFO detector, we calculated sensitivity and specificity from the contingency table with the following elements. True positive (TP) are windows classified as 1 that overlap with validated HFO, true negatives (TN) are windows where both, detected and validated HFO are 0, false positive (FP) are windows that are classified as 1 where there is no validated HFO and false negative (FN) windows are where the detector outputs 0 and there is a validated HFO.

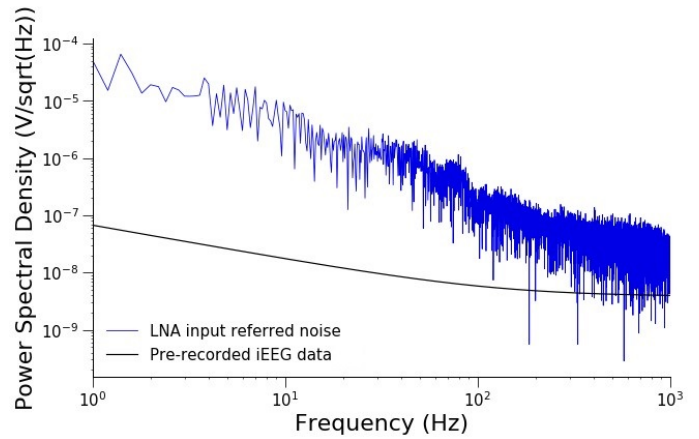


Fig. 4: Frequency spectrum of human iEEG from [10] versus systematic noise of the designed LNA.

IV. RESULTS

A. Analog Front-End Simulation Results

We performed circuit simulations of the analog front-end using a standard $0.18 \mu\text{m}$ technology node. According to the simulation results, the LNA generates $\leq 100 \text{ nV}/\sqrt{\text{Hz}}$ noise throughout the spectrum. This figure scaled down as frequency increased. Thus, Ripple band signal experiences $10 \text{ nV}/\sqrt{\text{Hz}}$ and FR band, $5 \text{ nV}/\sqrt{\text{Hz}}$, as shown in Fig. 4. The circuit level simulations of the LNA revealed a 0.8 Hz-10 KHz bandwidth, 0.7 V/1.8 V output swing and more than 40 dB common mode rejection ratio. This circuit consumed $3 \mu\text{W}$ of power per channel while presenting switchable gain among 20 dB, 32 dB, 36 dB and 40 dB.

Each filter consumed $0.9 \mu\text{W}$ power and the biases were optimized such that low-pass filter cut-off frequency was set to 80 Hz and band pass filters have 80 Hz-250 Hz and 250 Hz-500 Hz bandwidth for Ripple and FR detection respectively observed in Fig. 5. The asynchronous ADC circuit featured adjustable refractory period, minimum inter-spike time-step, allowing spike-rates to vary from 500 Hz to 1 MHz. The least significant delta recognized by ADC is $500 \mu\text{V}$ and static power consumption was 104 nW. The overall hardware specifications are presented in Table I.

B. Network Simulation Results

The network resulted in a sensitivity of 99.5% and specificity of 55.7% for HFO detection in the training dataset. The sensitivity of the network on the test dataset, which consists of five-minutes iEEG recordings not used for training (Fig. 6), was 90.5% and specificity was 67.7% (Table II).

V. CONCLUSION

Employing event-based processing in biomedical pattern recognition and signal classification offers an efficient real-time solution and reduces power consumption, complexity and output data rate in multi-channel recording systems. The compact SOC design and low power consumption makes this

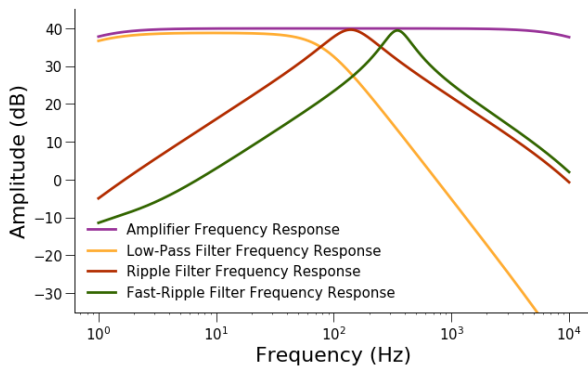


Fig. 5: Frequency response of LNA, low-pass filter, and two implemented band-pass filters

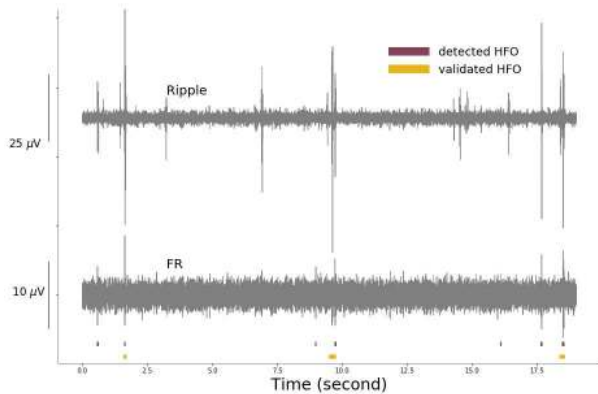


Fig. 6: Continuous iEEG filtered in Ripple and FR band (test set). Our network detected more HFO (purple marks) than there were HFO validated in current practice (golden marks) [1], [10].

TABLE I: Analog Front-End specifications

Feature	Value
Power Consumption	6.2 μ W/ch
In band noise	$\leq 100\text{nV}/\sqrt{\text{Hz}}$
Amplifier Gain (V/V)	10/40/70/100
Amplifier THD	$\leq 1\%$
Overall Gain (V/V)	80/320/560/800
CMRR, PSRR	$\geq 40\text{dB}$
Frequency Range	0.8Hz-10kHz
Band Config	LPF-BPF-BPF-APF
ADC LSB	500 μ V
Spiking Rate	500Hz-1MHz
Number of Channels	8/chip
Supply Voltage	1.8 V

device suitable for the operating theatre where it may support the medical team during epilepsy surgery.

This study is a proof of concept that verifies that a network running in an event-based processor can potentially identify clinically relevant features in human iEEG. Although we present here ongoing work that must be confirmed by more datasets, the promising results from our simple network encourage us to explore more powerful SNN-based computational paradigms for further performance improvements [11].

TABLE II: Classification results in training and test iEEG datasets based on mean firing rate of UP and DOWN spike trains in FR and Ripple bands.

Metrics	Equivalence	Detection in training dataset	Detection in test dataset
Sensitivity	TP/(TP+FN)	99.5%	90.5%
Specificity	1-(FN/(TP+FN))	55.7%	67.7%
Positive Predicted Value	TP/(FP+TP)	57.4%	61.0%
Accuracy	(TP+TN)/(TP+FP+FN+TN)	71.5%	73.9%

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