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Research Article

A New 7-Level Symmetric Multilevel Inverter with Minimum Number of Switches

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Though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. Therefore, a renewed 7-level multilevel inverter topology is introduced incorporating the least number of unidirectional switches and gate trigger circuitry, thereby ensuring the minimum switching losses, reducing size and installation cost. The new topology is well suited for drives and renewable energy applications. The performance quality in terms of THD and switching losses of the new MLI is compared with conventional cascaded MLI and other existing 7-level reduced switch topologies using carrier-based PWM techniques. The results are validated using MATLAB/SIMULINK.

1. Introduction

The term "multilevel inverter" was rooted years ago. Multilevel inverters offer various applications in voltage ranging from medium to high such as in renewable sources, industrial drives, laminators, blowers, fans, and conveyors. Small voltage step results in making the multilevel inverters withstand better voltage, fewer harmonics, high electromagnetic compatibility, reduced switching loss, and better power quality [1].

Cascaded multilevel inverters were developed in the initial stage. Later, diode-clamped MLI'S were developed followed by flying capacitor MLI'S. These three topologies utilise different mechanisms to produce the required output. The topology introduced first, that is, the CMLI, is simply series connection of H-bridges. The diode-clamped MLI uses series capacitor bank whereas, in flying capacitor mli, floating capacitors are used in order to clamp the output voltage [1]. H-bridge inverters have isolation transformers, and then H-bridge cascaded MLIS were introduced to separate DC input sources. But they do not need either clamping a diode or flying capacitors. Absence of voltage imbalance is the main advantage of cascaded mli. Fewer components are used in CMLI compared to diode-clamped and flying capacitor mlis [2–4].

Most of the researches are carried out in cascaded MLI configuration. But still the new trends are involved in the evolution of renewed multilevel inverters. Modifications are made in its inbuilt structure. A 7-level MLI was generated with 9 switches reducing 3 switches from the main conventional CMLI [5]. It offers good results yielding desired a 7-level output with low THD. A 7 level MLI with 7 switches reducing 2 more switches from the previous topology made a far improvement in the investigation of the switch reduction [6]. Yet another topology of 7-level MLI was configured with 4 dc sources and just 6 switches to get 7-level output [7]. The latter made a drastic move in topology development since the THD is low, and gate circuits used to drive the switches are less.

It is mentioned everywhere that simplicity is the main advantage of CMLI to generate 5 levels using 8 switches, 7 levels with 12 switches, 9 levels with 16 switches, and so on [2–4, 8]. It clearly reveals that an increase in levels demands more number of switches. Then the comment on simplicity of CMLI is simply contradictory. Hence, the focus was eyeing on a real solution to this problem, that is, how to simplify the complex circuit. Then arise the concept of "switch reduction". Exploring the existing topologies on basic 7 level, switch reduction was made from 12 switches to 9, gradually to 7 and then to 6.

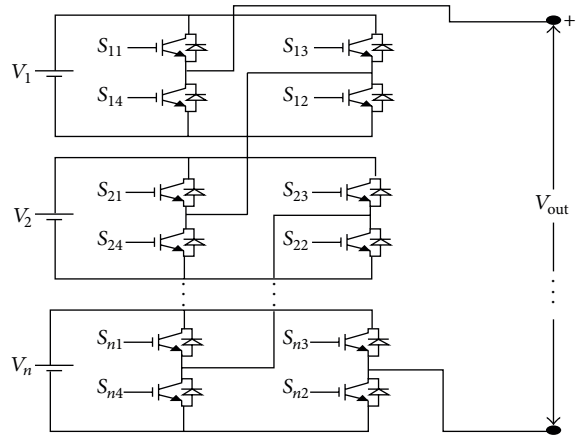


Figure 1: Conventional cascaded n-level MLI.

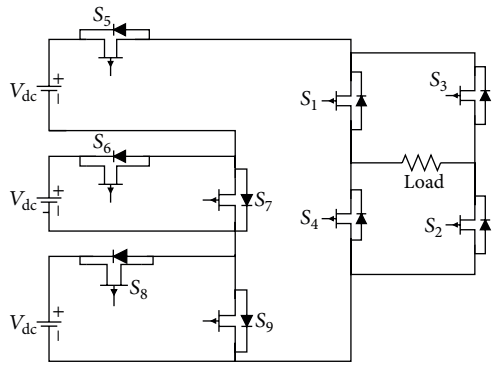


Figure 2: 7-level 9-switch topology.

Aiming at reducing the switches to the maximum possible extent and reducing complexity, the new topology is introduced with 5 switches for 7 levels, and this would be the least possible reduction. The new MLI configuration is made of 5 switches eliminating 1 switch from the existing 6 switches, 7-level topology [7] in a special arrangement with 4 inputs DC sources to generate 7 level output. The less switches we use lessen the cost of circuit building. The circuit credibility is checked without using pwm. Then identifying the effectiveness in working simulated the circuit with PD, POD, and APOD using MATLAB/SIMULINK.

(1) *Conventional Topology*. Using 3 DC voltage sources, 3 H-bridge units each with 4 switches together forming 12 switches in total are used in conventional CMLI which is represented in Figure 1. General expression for output voltage levels, $m = (n + 2)/2$ where n is the number of switches in the configuration. Each Bridge is outputting 3 Levels, $+V$dc, 0, $-V$dc. Cascading 3 Bridges in such a fashion to produce stepped 7 level staircase waveforms.

(2) *Existing Topology*

(a) *7-Level, 9 Switches.* This topology which is shown in Figure 2 is built with 3 dc sources, 1 H-bridge composed of 4 switches and then additional 5 more switches for producing stepped 7 levels, for positive and negative half cycles. Table 1 represent the switching scheme for this topology.

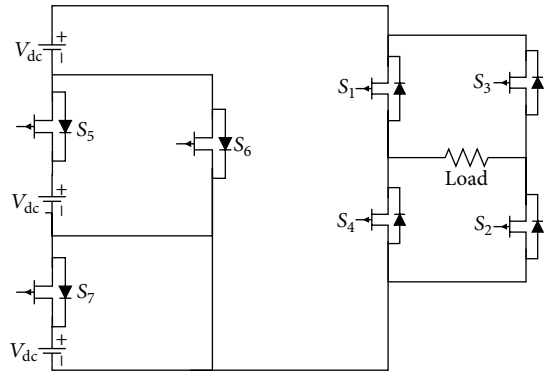


Figure 3: 7-level 7-switch topology.

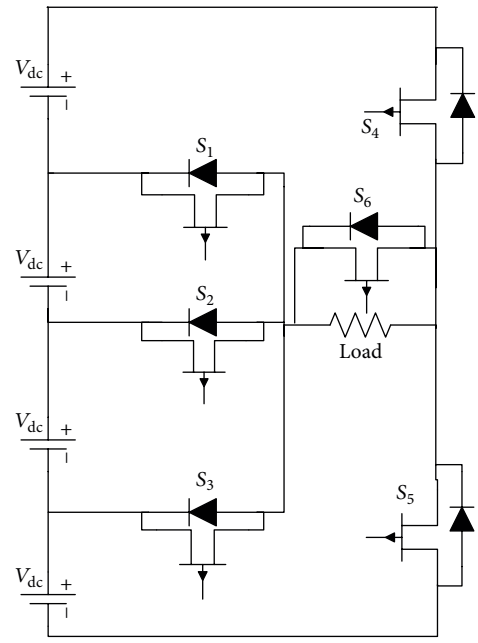


Figure 4: 7-Level 6-switch topology.

(b) *7-Level, 7 Switches.* This topology is made of 7 switches and 3 dc sources and is shown in Figure 3. One H-bridge present in the topology is mainly for polarity change. Here, three switches conduct at a time for level generation. The switching scheme is given in Table 2.

(c) *7-Level, 6 Switches.* This is a special configuration consisting of four dc sources and six switches. One switch across the load is used for zero level. $S1$, $S2$, $S3$ used for level generation and $S4$, $S5$ switches for polarity changing Figure 4 represent the 7-level 6-switch topology and the corresponding switching pattern is given in Table 3.

Table 1: Switching scheme for 7-level 9-switch topology.

SL no.	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output voltage	
1	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	+Vdc
2	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	+2Vdc
3	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	−Vdc
6	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	−3Vdc

Table 2: Switching scheme for 7-level 7-switch topology.

SL no.	S_4	S_5	S_6	S_7	S_1	S_2	S_3	Output voltage
1	ON	ON	ON	OFF	OFF	OFF	ON	+Vdc
2	ON	ON	OFF	OFF	OFF	ON	OFF	+2Vdc
3	ON	ON	OFF	OFF	ON	OFF	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	ON	ON	OFF	−Vdc
6	OFF	OFF	ON	ON	ON	OFF	ON	−2Vdc
7	OFF	OFF	ON	ON	OFF	ON	ON	−3Vdc

Table 3: Switching scheme for 7-level 6-switch topology.

SL no.	S_1	S_2	S_3	S_4	S_5	S_6	Output voltage
1	OFF	OFF	ON	OFF	ON	OFF	+Vdc
2	OFF	ON	OFF	OFF	ON	OFF	+2Vdc
3	ON	OFF	OFF	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	ON	0
5	ON	OFF	OFF	ON	OFF	OFF	−Vdc
6	OFF	ON	OFF	ON	OFF	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	−3Vdc

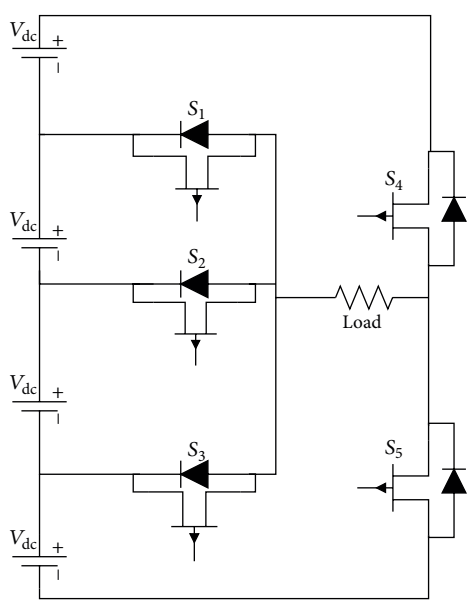


Figure 5: 7-level 5-switch proposed topology.

(3) *Proposed Five-Switch Topology*. The proposed 7 level MLI as shown in Figure 5 is about redesigning of existing 6-switch topology eliminating 1 switch attaining the tag of 5 switch configuration. The circuit thus obtained is the simplest design compared to conventional and all other existing topologies. It consists of four dc sources of 7 levels, for 9-level, 5 dc sources and so on.

Generalised expression for output voltage levels for the new topology proposed is $m = (2 * n - 3)$, where m = number of output voltage levels, n = number of switches $m = (2 * v - 1)$, where v = number of dc sources.

The design of pulse generation circuit makes the topology differ from others so as to obtain the unique pulse pattern to trigger the switches at the proper instant. Switches *S*1, *S*2, and *S*3 need to be compulsorily unidirectional or else the output waveform will get distorted. Reduced switches make the circuit compact and user-friendly. Though the usage of 4 dc sources for the generation of 7-level MLI results in less utilisation of sources, switch reduction benefits in low switching losses. No H-Bridge is used. Just 2 switches play the role of polarity reversal. Table 4 represent the switching scheme for the proposed topology.

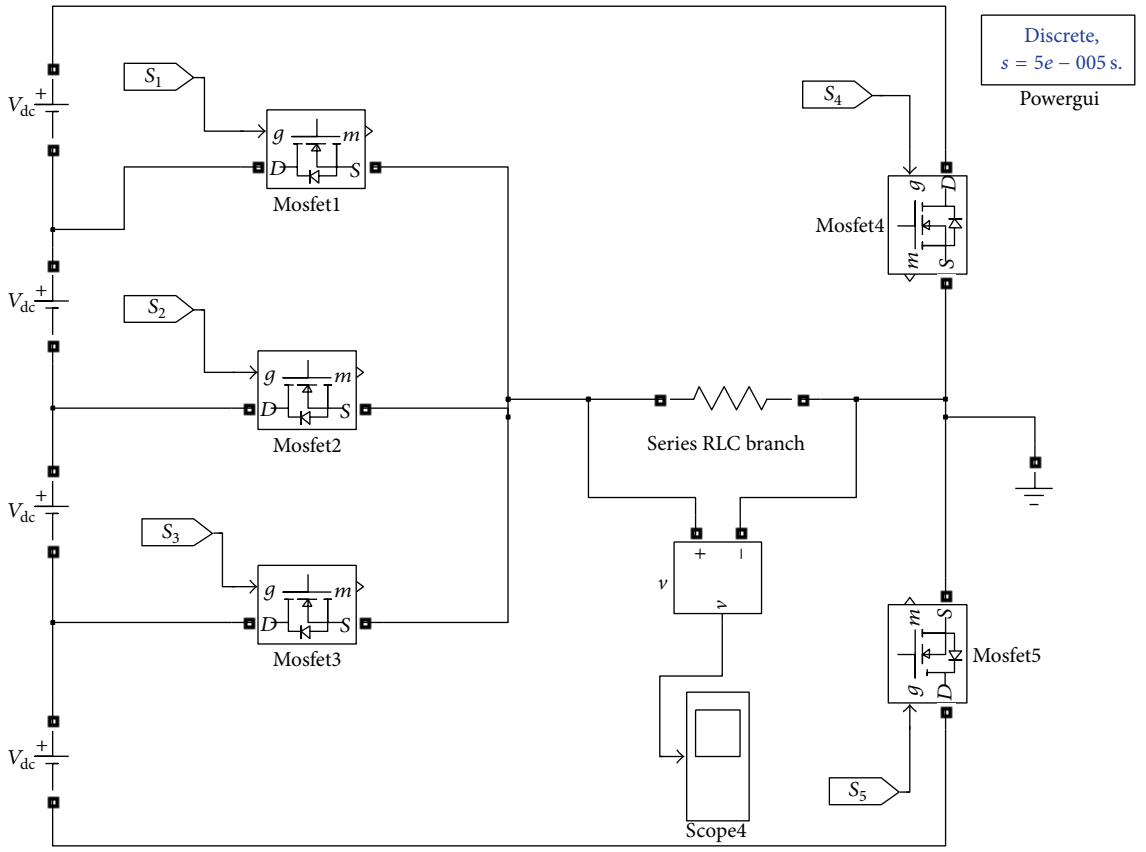
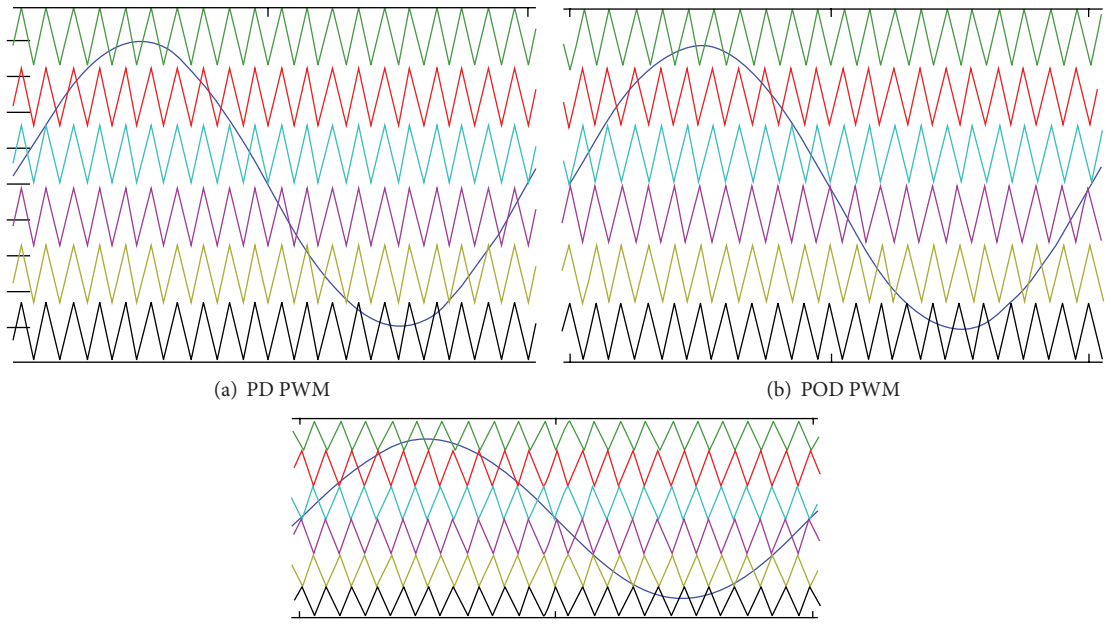


Figure 6: Simulation diagram of proposed topology.



(a) PD PWM

(b) POD PWM

(c) APOD PWM

Figure 7: Carrier alignment of carrier-based pwm techniques.

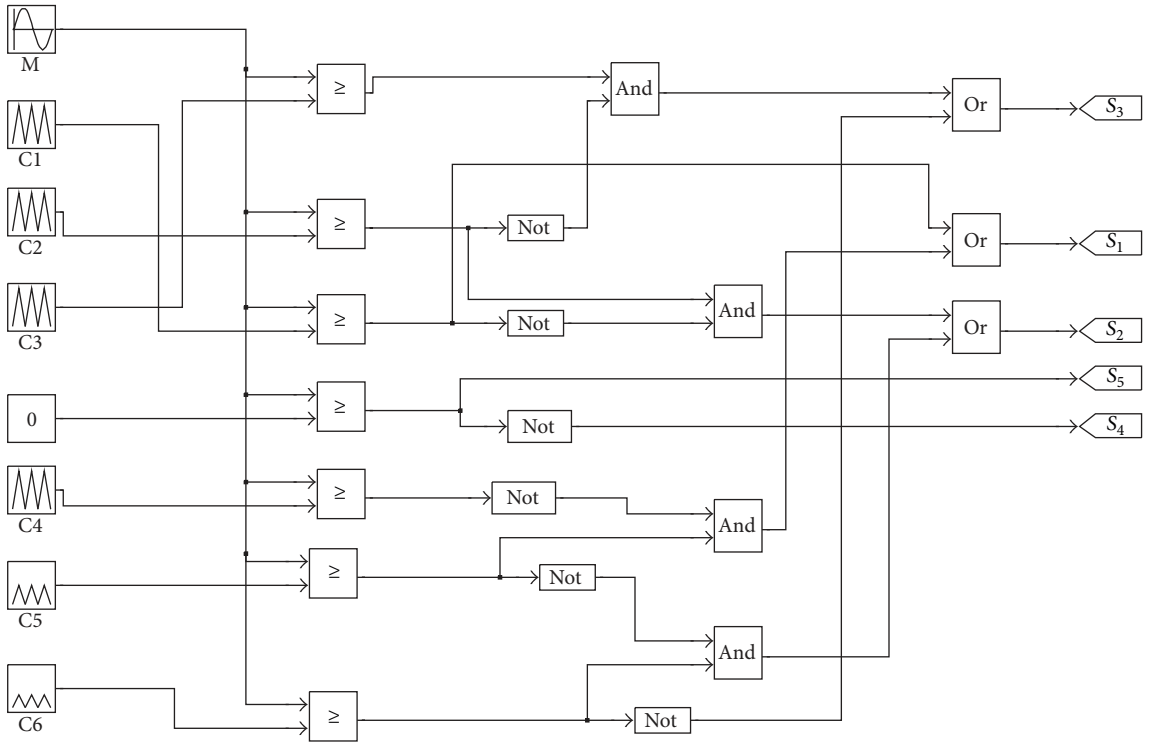


Figure 8: PWM generation circuit.

Table 4: Switching scheme for proposed topology.

SL no.	S_1	S_2	S_3	S_4	S_5	Output voltage
1	OFF	OFF	ON	OFF	ON	+Vdc
2	OFF	ON	OFF	OFF	ON	+2Vdc
3	ON	OFF	OFF	OFF	ON	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	0
5	ON	OFF	OFF	ON	OFF	−Vdc
6	OFF	ON	OFF	ON	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	−3Vdc

2. Simulation Circuit

In the proposed 7-level MLI, the circuit is built of 5 mosfet unidirectional switches. It can also be built with 3 unidirectional and 2 bidirectional switches. The load is resistive with a value of 10 ohms. Four 10-volt symmetric DC input voltages are used Figure 6 represent the simulation circuit of the proposed topology.

Note that in order to obtain the shaped 7-level output without distortion, MOSFET block parameters in MATLAB should vary according to the load used. Here for 10 ohm resistive load, Mosfet block parameters are set as follows:

FET resistance = 0.01 ohms, internal diode resistance = 10 kilo ohms.

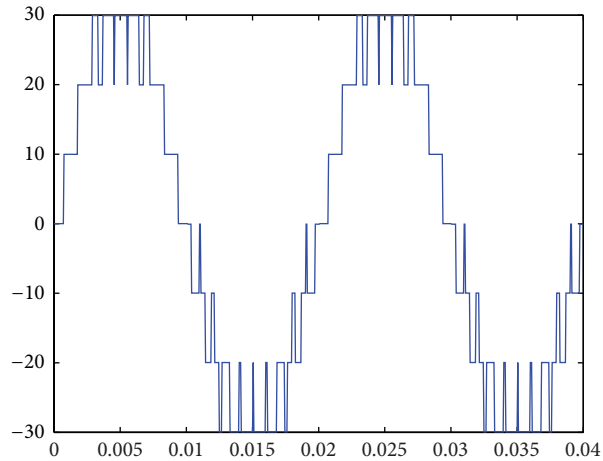


Figure 9: 7-level output of proposed topology.

3. Methodology

The pulse generation is essential in order to trigger the switches with appropriate pulse pattern to produce the desired 7-level output. It is inevitable to analyse which PWM suits the new topology. The simplest PWM technique is the carrier-based PWM (CBPWM) technique. It can be further categorised into level and phase shifting CBPWMs, respectively. Since the phase shifting CBPWM yields more harmonics comparatively, the level shifting CBPWM is preferred over

Table 5: THD content.

PWM technique	Symmetric conventional cascaded 7-level mli (%)	Asymmetric conventional cascaded 7-level mli (%)	7-level, 9 switches (%)	7-level, 7 switches (%)	7-level, 6 switches (%)	Proposed 5-switch 7-level mli (%)
PD	24.26	21.84	—	—	18.08	18.07
POD	23.13	20.22	28.3	14	16.15	16.12
APOD	22.46	19.42	—	—	18.52	18.40

Table 6: Voltage stress in proposed topology across switches.

Parameter	Conventional CMLI	9 switches, 7-level	7 switches, 7-level	6 switches, 7-level	Proposed topology 5 switches, 7-level
Voltage stress	5 V (All switches)	11 V (S5) 10 V (S6) 2 V (S7) 10 V (S8 & S9)	6 V (S3) 6 V (S2) 18 V (S1)	3.33 V (S3) 13.3 V (S2) 23.3 V (S1)	3.33 V (S3) 13.3 V (S2) 23.3 V (S1)

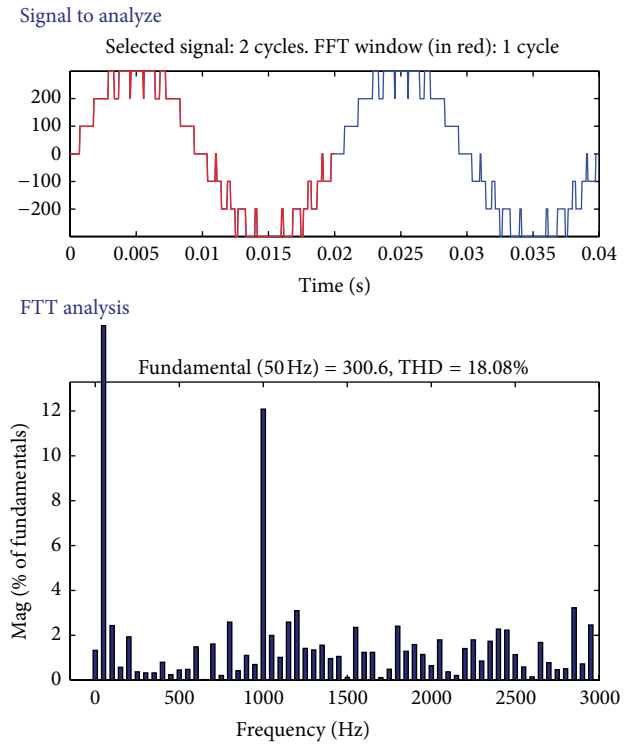


Figure 10: FFT analysis of existing 6-switch topology using PD pwm.

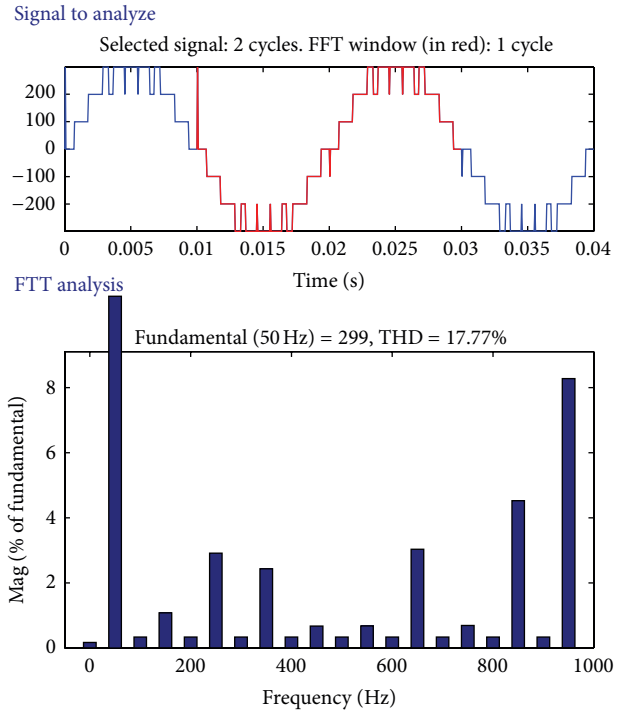


Figure 11: FFT analysis of existing 6-switch topology using POD pwm.

it. Therefore, the new circuit design is analysed with level shifting carrier -based PWMs, that is, PD, POD, and APOD PWMs. Interestingly, it is noted that POD gives lower THD and is found to be the apt PWM for proposed topology. The PWM generation circuit is the heart of the circuitry. One reference sine wave of amplitude 0.8 and frequency 50 Hertz is compared with C1 to C6 triangular carriers of frequency 1 KHz. If m-level needs to be synthesised, $(m - 1)$ carriers are required. Whenever the reference sinusoid exceeds the carrier, instant pulses are generated to trigger the switch to 0N state. Higher triangular carrier amplitude is taken as one.

The carrier alignment for the carrier based pwm technique is shown in Figure 7. In PD or phase disposition technique, $(m-1)$ carriers are aligned in the same direction/phase. In POD or phase opposition disposition for 7-level, 6 carriers are aligned as symmetric mirror images above and below the Zero reference axis. In alternate phase opposition disposition, alternate carriers are in the same phase and neighbouring carriers in the opposing phase.

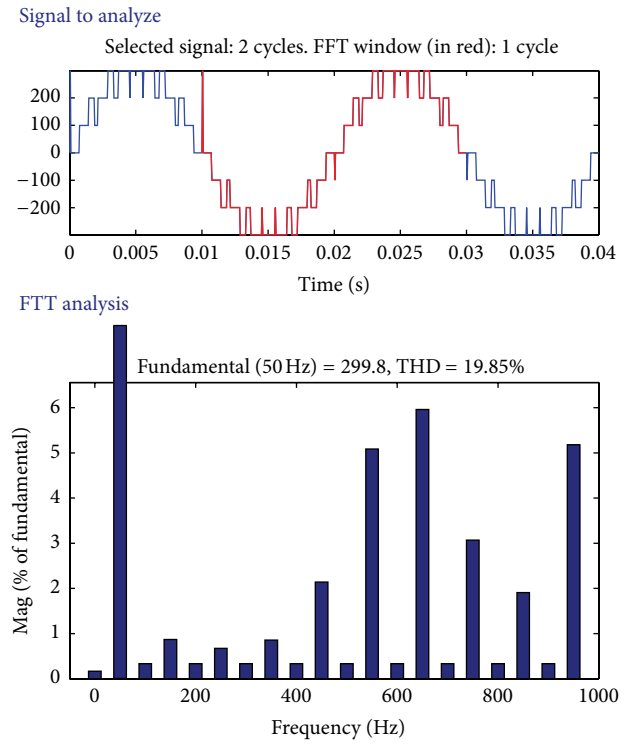


Figure 12: FFT analysis of existing 6-switch topology using APOD pwm.

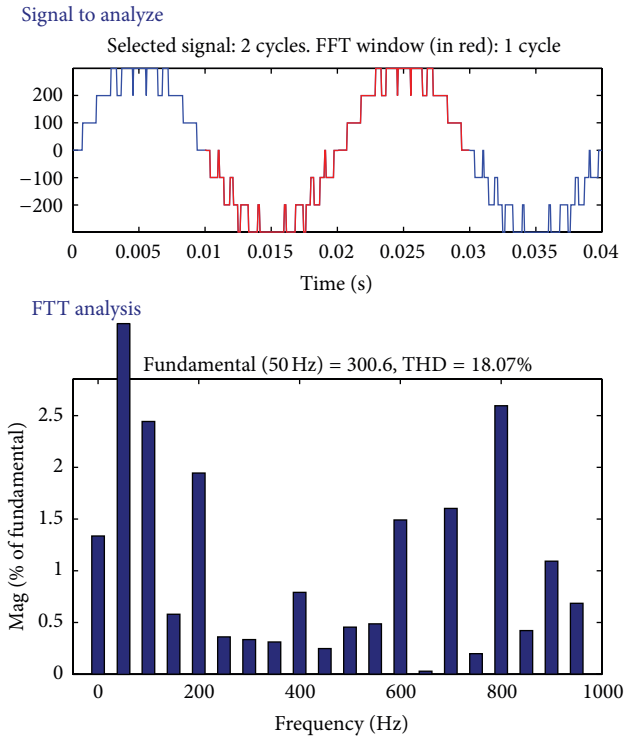


Figure 13: FFT analysis of proposed topology using PD pwm.

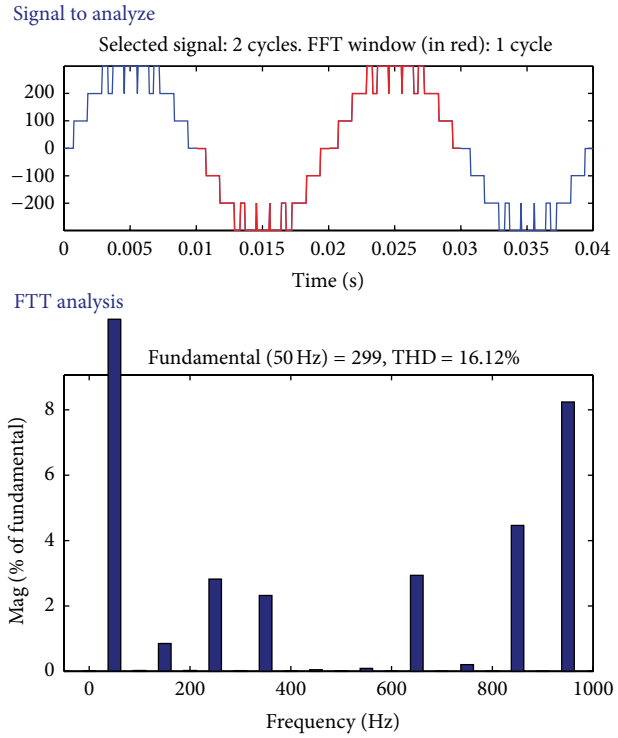


Figure 14: FFT analysis of proposed topology using POD pwm.

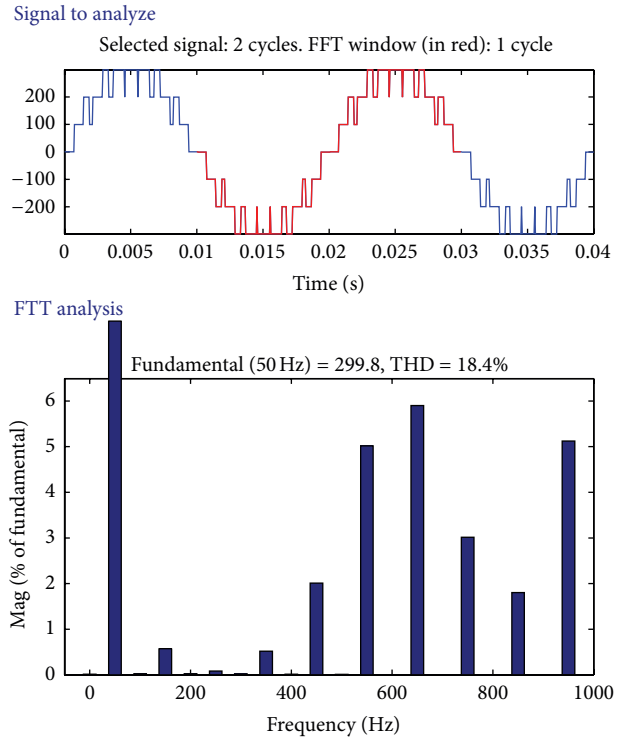


Figure 15: FFT analysis of proposed topology using APOD pwm.

Table 7: Comparison of proposed 7-level mli with other mlis.

Inbuilt structure	Flying capacitor	Diode clamped	Cascaded 7-level	7-level, 9 switches	7-level, 7 switches	7-level, 6 switches	Proposed 7-level, 5 switches
No. of capacitors	14	6	—	—	—	—	—
No. of diodes	—	≥8	—	—	—	—	—
No. of switches	10	10	12	9	7	6	5*
No. of dc sources	—	—	3	3	3	4	4*

4. Pulse Generation Circuit

The pulse generation circuit is given in Figure 8. The reference signal comparing with carrier generating pulse which is then modified feeding to logic gates in order to get the required pattern to trigger the switches at the proper instant. For examples switche S_1 needs to have a pulse so as to obtain $+V$dc and $-3V$dc and S_2 requires $+2V$dc and $-2V$dc. S_3 conducts $+3V$dc and $-V$dc. Also, switches S_5 and S_4 conduct positive and negative half cycles, respectively.

5. Simulation Results

See Figures 9, 10, 11, 12, 13, 14, and 15, and Tables 5, 6, and 7.

6. Conclusion

The 7-level MLI using just 5 switches is successfully introduced simulating the circuitry using MATLAB/SIMULINK and observed a clear stepped 7-level waveform. It is found that the POD-PWM dominates all other PWMs in the proposed configuration. The new design is simple in its outlook with very few components. The novel 7-level mli has lower THD compared to conventional symmetric and asymmetric topologies.

References

[1] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[2] D. Mohan and S. B. Kurub, "Performance analysis of SPWM control strategies using 13 level cascaded MLI," in *IEEE International Conference on Advances in Engineering Science & Management (ICAESM '12)*.

[3] O. L. Jimenez, R. A. Vargas, J. Aguayo, J. E. Arau, G. Vela, and A. Claudio, "THD in cascade multilevel inverter symmetric and asymmetric," in *Proceedings of the IEEE Electronics, Robotics and Automotive Mechanics Conference (CERMA '11)*, pp. 289–295, November 2011.

[4] P. Palanivel and S. S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," *IET Power Electronics*, vol. 4, no. 8, pp. 951–958, 2011.

[5] J. J. Nedumgatt, D. Vijayakumar, A. Kirubakaran, and S. Umashankar, "A multilevel inverter with reduced number of switches," in *Proceedings of the IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS '12)*, pp. 1–4, March 2012.

[6] T. V. V. S. Lakshmi, N. George, S. Umashankar, and D. P. Kothari, "Cascaded seven level inverter with reduced number of switches using level shifting PWM technique," in *International Conference on Power, Energy and Control (ICPEC '13)*, pp. 676–680, February 2013.

[7] R. A. Ahmed, S. Mekhilef, and H. W. Ping, "New multilevel inverter topology with minimum number of switches," in *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON '10)*, pp. 1862–1867, Cairo University, Cairo, Egypt, December 2010.

[8] M. H. Rashid, *Power Electronics: Circuits, Devices and Applications*, Prentice Hall, New York, NY, USA, 3rd edition, 2004.