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A New Active Zero State PWM Algorithm for Reducing the Number of Switchings

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Abstract

To reduce common-mode voltage (CMV), various reduced CMV pulse width modulation (RCMV-PWM) algorithms have been proposed, including active zero state PWM (AZSPWM) algorithms, remote state PWM (RSPWM) algorithms, and near state PWM (NSPWM) algorithms. Among these algorithms, AZSPWM algorithms can reduce CMV, but they increase the number of switchings compared to the conventional space vector PWM (CSVPWM). This paper presents a new AZSPWM algorithm for reductions in both the CMV and total number of switchings in BLAC motor drives. Since the proposed AZSPWM algorithm uses only active voltage vectors for motor control, it reduces CMV by 1/3 compared to CSVPWM. The proposed AZSPWM algorithm also reduces the total number of switchings compared to existing AZSPWM algorithms by eliminating the switchings required from one sector to the next. The performance of the proposed algorithm is verified by analyses, simulations, and experimental results.

Key words: Active Zero State PWM (AZSPWM), Common-Mode Current (CMC), Common-Mode Voltage (CMV), Space Vector Pulse Width Modulation (SVPWM)

I. INTRODUCTION

Most induction and permanent magnet motors are driven by voltage source inverters (VSIs) that can easily manage the voltage and frequency. The development of high-speed switching devices necessitated the high-speed operation of inverter switches. This development reduces motor current and torque ripple, and improves dynamic performance. However, this results in problems with the common-mode voltage (CMV) and the common-mode current (CMC). The high dv/dt of the CMV caused by fast switching increases the magnitude of the CMC, and it generates a variety of problems such as breakdown of the motor winding, damage of the motor bearings, and conductive electromagnetic interference (EMI) noise that results in a nuisance trip of the inverter drive or interference with other electronic equipment in the vicinity.

To solve the CMV/CMC problem, various methods have been proposed [1]. There are several methods for coping with this problem such as using hardware (common-mode chokes [2], 4-phase inverters [3], and filters [4]-[6]) and software (PWM algorithms). Methods using hardware increase the size of the system and incur additional costs. However, methods using software that only changes the switching patterns, are considerably simpler to implement, and do not result in additional size and costs. Hence, research has now been focused on the development of various PWM algorithms for the reduction of CMV, known as reduced CMV-PWM (RCMV-PWM) algorithms [7]-[16].

RCMV-PWM algorithms can be divided into three groups: active zero state PWM (AZSPWM) algorithms [7]-[16], remote state PWM (RSPWM) algorithms [14], and near state PWM (NSPWM) algorithms [12], [14], [16]. In addition, the AZSPWM algorithms can be further divided into AZSPWM1 [7]-[14], [16], AZSPWM2 [13]-[15], and AZSPWM3 [8], [13], [14] algorithms. When these algorithms synthesize the reference voltage vector, the AZSPWM algorithms use three or four active voltage vectors including two active opposite voltage vectors instead of zero voltage vectors. The RSPWM algorithm uses three active voltage vectors that are 120 deg. apart from each other. The NSPWM algorithm uses a group

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of three neighboring active voltage vectors. Since they use different voltage vectors when synthesizing the reference voltage vector, the overall performances and characteristics are different for all of these algorithms. However, the principle for the reduction of CMV is the same and only active voltage vectors are used. By these algorithms, the CMV is reduced from $\pm V_{dc}/2$ of the conventional space vector PWM (CSVPWM) algorithm to $\pm V_{dc}/6$. However, it can be seen that the output phase current ripple and the DC bus current ripple of the inverter are slightly higher than those of the CSVPWM algorithm via theory, analyses, simulations, and experimental results [11], [13], [14].

Among these algorithms, the AZSPWM algorithms also increase the number of switchings compared to the CSVPWM. The number of switchings is a significant index for the heat performance and efficiency of an inverter for motor control. The total number of switchings is divided into the number of switchings in a sector and the number of switchings from one sector to the next. The switching pattern of AZSPWM algorithms is symmetrical, and it is similar to that of the CSVPWM. Hence, the number of switchings in a sector is the same as that of the CSVPWM. However, because the applied voltage vector changes when the reference voltage crosses a sector, switching from one sector to the next occurs. The details are explained in Section IV.

In this paper, the CSVPWM algorithm and the AZSPWM1-3 algorithms are compared and analyzed in terms of the total number of switchings. Then a new AZSPWM algorithm that has a minimum number of switchings and can reduce CMV is proposed. Finally, the CSVPWM and the proposed AZSPWM algorithm are compared in terms of the CMV and harmonic components of the output phase current through simulation and experimental results.

II. BASIC CONCEPT OF THE SVPWM

A three-phase VSI produces eight voltage vectors, as shown in Fig. 1. Among these voltage vectors, V_0 and V_7 are known as zero voltage vectors and those from V_1 to V_6 are known as active voltage vectors. The reference voltage vector, V_{ref} can be synthesized by two zero voltage vectors in combination with two adjacent active voltage vectors depending on the sector. The durations of T_1, T_2 and T_0 during which V_n, V_{n+1}, and V_0 or V_7 act, can be expressed as:

$$T_1 = T_s \cdot M_i \cdot \frac{\sin(60^\circ - \theta)}{\sin 60^\circ}$$
$$T_2 = T_s \cdot M_i \cdot \frac{\sin \theta}{\sin 60^\circ} \quad (1)$$
$$T_0 = T_s - T_1 - T_2$$

where T_s = sampling period, T_1 = the duration of V_n, T_2 = the duration of V_{n+1}, T_0 = the duration of V_0 or V_7, θ = angle of

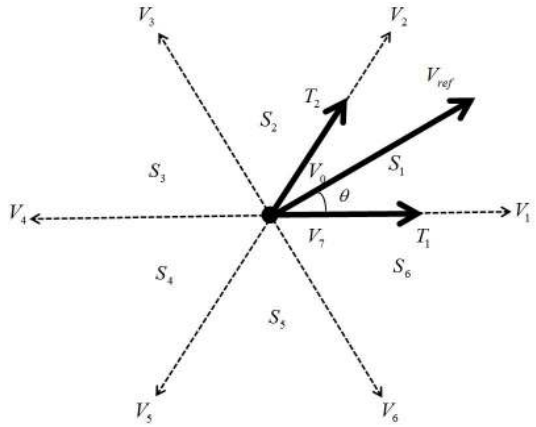


Fig. 1. Voltage vectors of a three-phase VSI.

V_{ref}, and M_i = modulation index given by $3V_{ref}/2V_{dc}$. To minimize the number of switchings and the output voltage ripple, the zero voltage vectors V_0 and V_7 are applied for the same duration, and V_0 is equally applied at the beginning and end of the switching period, and V_7 is applied in the middle of the switching period. The switching patterns for the CSVPWM are shown in Table II.

III. CMV OF THE CSVPWM AND THE AZSPWM1-3 ALGORITHMS

Fig. 2 presents a three-phase VSI controlled motor drive system. The motor is represented by the impedance, Z_m, composed of the resistor, R_m, and the inductor, L_m. The equations of the ac motor are represented as follows:

$$V_{an} - V_{sn} = R_m i_{as} + L_m \frac{di_{as}}{dt} \quad (2)$$
$$V_{bn} - V_{sn} = R_m i_{bs} + L_m \frac{di_{bs}}{dt} \quad (3)$$
$$V_{cn} - V_{sn} = R_m i_{cs} + L_m \frac{di_{cs}}{dt} \quad (4)$$

where V_{an}, V_{bn}, and V_{cn} are the inverter pole voltages; i_{as}, i_{bs}, and i_{cs} are the motor line currents; and V_{sn} is the common-mode voltage.

By adding (2) to (4), the following equation is derived:

$$V_{an} + V_{bn} + V_{cn} - 3V_{sn} = (R_m + L_m \frac{d}{dt})(i_{as} + i_{bs} + i_{cs}) \quad (5)$$

Since $i_{as} + i_{bs} + i_{cs} = 0$ by the three-phase balance condition, the CMV is calculated by:

$$V_{sn} = V_{cm} = \frac{V_{an} + V_{bn} + V_{cn}}{3} \quad (6)$$

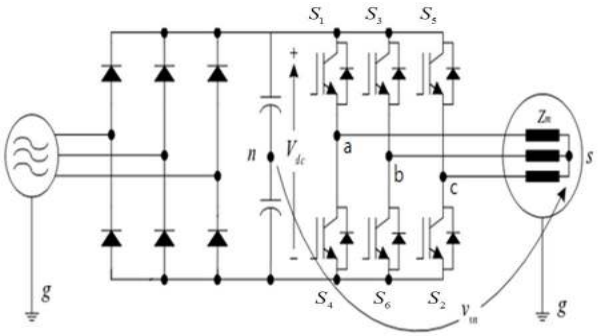


Fig. 2. Three-phase inverter controlled motor drive system.

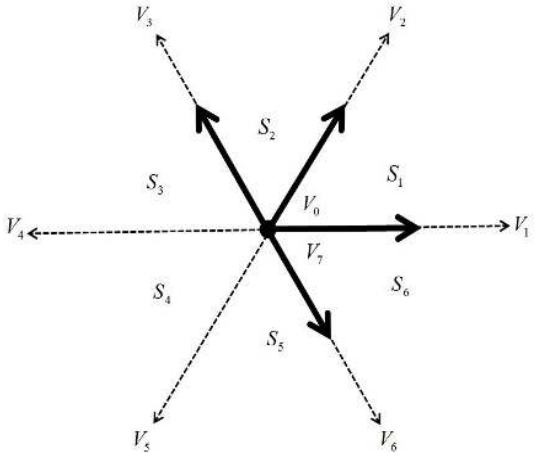
TABLE I
INVERTER POLE VOLTAGE AND CMV BY SWITCHING STATE

Switching state	Inverter pole voltage			CMV
	V_{an}	V_{bn}	V_{cn}	
V_0	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
V_1	$+V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
V_2	$+V_{dc}/2$	$+V_{dc}/2$	$-V_{dc}/2$	$+V_{dc}/6$
V_3	$-V_{dc}/2$	$+V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
V_4	$-V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/6$
V_5	$-V_{dc}/2$	$-V_{dc}/2$	$+V_{dc}/2$	$-V_{dc}/6$
V_6	$+V_{dc}/2$	$-V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/6$
V_7	$+V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/2$

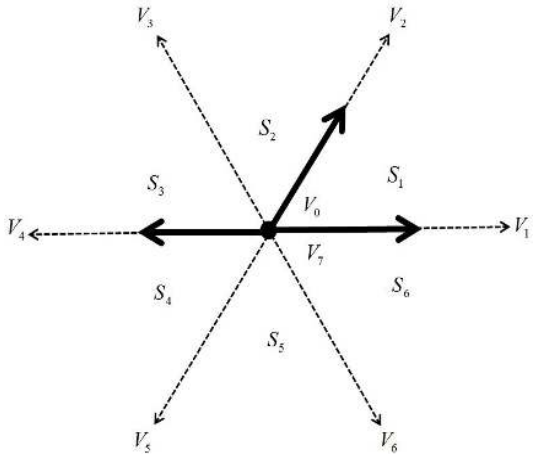
From (6), it is observed that the magnitude of the CMV is dependent on the inverter switching state. Table I shows the magnitude of the CMV corresponding to the eight-switching states of the three-phase VSI. The zero voltage vectors make a CMV of $\pm V_{dc}/2$, and the active voltage vectors make a CMV of $\pm V_{dc}/6$.

In the CSVPWM, two zero voltage vectors and two adjacent active voltage vecto—rs synthesize the reference voltage vector depending on the sector. Therefore, the range of the CMV is $-V_{dc}/2 \leq V_{sn} \leq V_{dc}/2$. In the AZSPWM algorithms, the range of the CMV can be reduced by 1/3 compared to the CSVPWM through the non-usage of zero voltage vectors when synthesizing the reference voltage vector. Therefore, the range of the CMV is $-V_{dc}/6 \leq V_{sn} \leq V_{dc}/6$. The basic concept is to replace the zero voltage vectors by using active 180-phase shifted voltage vectors, without affecting the linear modulation range.

Fig. 3 illustrates the applied vectors of the AZSPWM algorithms when the reference voltage vector is in sector 1, as an example. Instead of using zero voltage vectors, the active opposite voltage vectors are incorporated to synthesize the reference voltage vector. Therefore, the reference voltage vector is only composed of active voltage vectors, as shown in Fig. 3. The switching times of the active opposite vectors in the AZSPWM algorithms are the same as those for the zero voltage vectors in the CSVPWM.



(a) AZSPWM1, 2 algorithms.



(b) AZSPWM3 algorithm.

Fig. 3. Formation of the voltage vectors in space.

IV. ANALYSIS OF THE SWITCHING PATTERNS

The applied vectors can synthesize the reference voltage vector in each sector, regardless of the sequence. However, because the application of the vector causes switching that leads to heat loss, the switching patterns with the least number of switchings should be determined. Hence, this needs to be analyzed in detail. In the SVPWM algorithm, the total number of switchings is divided into the number of switchings in a sector and the number of switchings from one sector to the next. Table II shows the switching patterns for the CSVPWM and AZSPWM algorithms based on the sector, and Table III shows the type and number of switchings for each PWM algorithm considering only the upper switches S_1, S_3 and S_5.

A. Number of Switchings in a Sector

In the CSVPWM algorithm, the switching pattern is selected to make only one switching, considering only the upper switches S_1, S_3, and S_5, when the applied voltage vector changes in a sector. In the case where the reference voltage vector is in sector 1; when the applied vector is changed from V_0 to V_1, S_1 is turned on; when the change is from V_1 to V_2, S_3

is turned on; and when the change is from V_2 to V_7, S_5 is turned on. From V_7 to V_7, all of the switches are maintained; from V_7 to V_2, S_5 is turned off; from V_2 to V_1, S_3 is turned off; and from V_1 to V_0, S_1 is turned off. As a result, in the case of synthesizing the reference voltage vector located in sector 1 during a switching period, the number of switchings in the sector is six (1+1+1+0+1+1+1). The number of switchings in a sector is the same when synthesizing the reference voltage vectors located in sectors 2-6. For the AZSPWM1 algorithm, the same principle as mentioned above is applied, and the number of switchings in a sector is six (1+1+1+0+1+1+1). For the AZSPWM2 algorithm, the number of switchings in a sector is ten (2+1+2+0+2+1+2). Likewise, for the AZSPWM3 algorithm, the number of switchings in a sector is six (0+1+2+0+2+1+0).

B. Number of Switchings from One Sector to the Next

It is noticeable that switchings occur not only in each sector but also when the reference voltage vector crosses from one sector to the next. In the case of the CSVPWM algorithm, when the reference voltage vector crosses from sector 1 to sector 2, there is no voltage vector change from V_0 (the last applied voltage vector in sector 1) to V_0 (the first applied voltage vector in sector 2). Hence, the number of switchings is zero. The changes in the other sectors are the same as above; (from sector 2 to sector 3, sector 3 to sector 4, sector 4 to sector 5, sector 5 to sector 6, and sector 6 to sector 1). As a result, when the reference voltage vector makes one rotation, the number of switchings from one sector to the next is zero (0+0+0+0+0+0). In the case of the AZSPWM1 algorithm, when the reference voltage vector crosses from sector 1 to sector 2, the applied vector changes from V_3 to V_4. Therefore, the number of switchings is one. Based on the same principle, when the reference voltage vector changes from sector 2 to sector 3, sector 3 to sector 4, sector 4 to sector 5, sector 5 to sector 6, and sector 6 to sector 1, the number of switchings is one. As a result, when the reference voltage vector makes one rotation, the number of switchings is six (1+1+1+1+1+1). For the AZSPWM2 and AZSPWM3 algorithms as per the same principle, when the reference voltage makes one rotation, the number of switchings is six (1+1+1+1+1+1).

From this analysis, it is observed that the number of switchings in a sector is lowest in the CSVPWM and in the AZSPWM1, 3 algorithms. In addition, it can be seen that the number of switchings from one sector to the next is lowest in the CSVPWM algorithm. When the reference voltage makes one rotation, the total number of switchings when both the upper and lower switches are considered, can be derived as follows:

$$SW\ No. = \left(\frac{Switching\ Freq.}{Reference\ voltage\ vector\ Freq.} \times SW\ No.\ in\ sector + SW\ No.\ from\ one\ sector\ to\ the\ next \times 6 \right) \times 2 \quad (7)$$

If the reference voltage vector frequency is 100 Hz and the switching frequency is 20 KHz, the total number of switchings in the CSVPWM algorithm is ((20000/100)*6+0*6)*2 = 2400 during 0.01 s. Table IV presents the total number of switchings for each of the PWM algorithms for a period of 1 s. It can be observed that the CSVPWM algorithm has the lowest total number of switchings and that the difference in the total number of switchings increases in proportion to time.

TABLE II
SWITCHING PATTERNS

Sector	CSVPWM	AZSPWM1	AZSPWM2	AZSPWM3	PROPOSED AZSPWM
1	0127-7210	3216-6123	6213-3126	1124-4211	1124-4211
2	0327-7230	4321-1234	1324-4231	2235-5322	1234-4321
3	0347-7430	5432-2345	2435-5342	3346-6433	1344-4431
4	0547-7450	6543-3456	3546-6453	4451-1544	1544-4451
5	0567-7650	1654-4561	4651-1564	5562-2655	1654-4561
6	0167-7610	2165-5612	5162-2615	6613-3166	1164-4611

TABLE III
TYPE AND NUMBER OF SWITCHINGS

	The number of switching in a sector	The number of switching from one sector to the next
CSVPWM	6	0
AZSPWM1	6	1
AZSPWM2	10	1
AZSPWM3	6	1
PROPOSED AZSPWM	6	0

V. PROPOSED AZSPWM ALGORITHM

This paper proposes a new AZSPWM algorithm that reduces the CMV by 1/3 compared to the CSVPWM and reduces the total number of switchings when compared to the AZSPWM1-3 algorithms. The switching pattern for the proposed AZSPWM algorithm is summarized in Table II.

From the analysis of the switching pattern for the proposed AZSPWM algorithm, it can be observed that the number of switchings in each sector is equal to the number of switchings of the CSVPWM and AZSPWM1, 3 algorithms, as shown in Table III.

As explained in Section IV, because the last applied voltage vector of one sector and the first applied voltage vector of the next sector are equal to V_0 for all of the sector crossings, the number of switchings from one sector to the next is zero in the CSVPWM algorithm. Likewise, if these voltage vectors are made equal in all of the sectors, the switching required from one sector to the next can be eliminated. In the proposed AZSPWM algorithm, because the last applied voltage vector of one sector and the first applied

TABLE IV
TOTAL NUMBER OF SWITCHINGS

	SW NO.
CSVPWM	240000
AZSPWM1	241200
AZSPWM2	401200
AZSPWM3	241200
PROPOSED AZSPWM	240000

voltage vector of the next sector are equal to V_1 for all the sector crossings, the number of switchings from one sector to the next is zero as in the CSVPWM algorithm, as shown in Table III. Therefore, the total number of switchings of the proposed AZSPWM algorithm is the same as that of the CSVPWM algorithm, as shown in Table IV.

In addition, as it only uses active voltage vectors when synthesizing the reference voltage vector, the range of the CMV is $-V_{dc}/6 \le V_{sn} \le V_{dc}/6$. As a result, the proposed AZSPWM algorithm can reduce the range of the CMV so that it is equal to that of the AZSPWM1-3 algorithms, and the total number of switchings is equal to that of the CSVPWM, which has the lowest number of switchings. Table II depicts the switching patterns when the last applied voltage vector of one sector and the first applied voltage vector of the next sector are made equal to V_1, as an example. Similar algorithms for V_2, V_3, V_4, V_5 and V_6 can also be derived.

VI. SIMULATION AND EXPERIMENTAL RESULTS

To verify the validity of the proposed AZSPWM algorithm and to compare it with the CSVPWM algorithm, simulation and experimental tests were performed. The simulation was carried out using PSIM9.0 and VISUAL C++, and the hardware setup of the experiment is shown in Fig. 4. The setup consists of a main board (a VSI, a MCU, a gate driver, and a BLAC motor), a DC supply, a simulator, an oscilloscope, and a laptop. An MCU (TriCore277) is utilized to control the motor speed and to program the PWM pulse pattern. The control scheme used in this test is shown in Fig. 5. The BLAC motor used in this test has the following rated values: 1KW, 4N-m, 1500rpm, 8-pole, and 100Hz. It also has the following parameters: R_s, R_r=9.75mΩ, L_s, L_r=31.28uH, and J=39.8Kg.m^2. During the test, the DC bus voltage was 12V, the switching frequency was 20kHz, and the dead time was 80ns. The test was performed under a no-load condition in order to clearly depict the ripple of the output current.

Fig. 6 shows simulation waveforms of the line-to-line voltage and the output current of phase-a in both the CSVPWM algorithm and the proposed AZSPWM algorithm, respectively. It can be seen that the output current ripple of the proposed AZSPWM algorithm is slightly higher than that of the CSVPWM algorithm as expected [11], [13], [14].

In Fig. 7, simulation waveforms of the CMV are presented

Fig. 4. Hardware configuration.

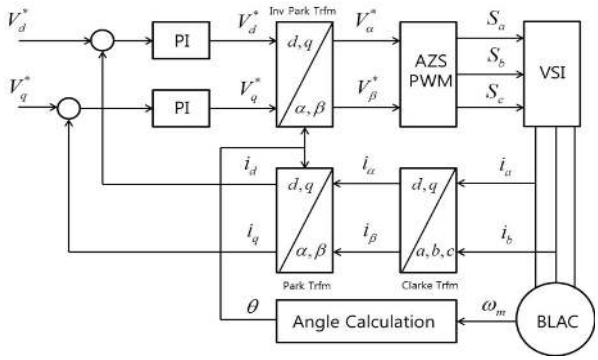
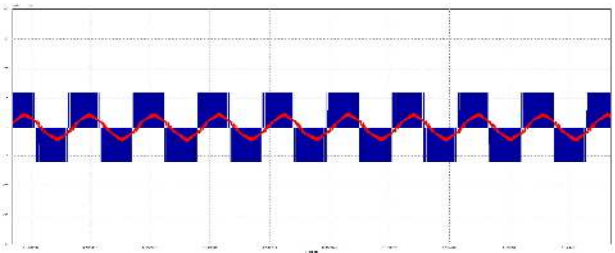
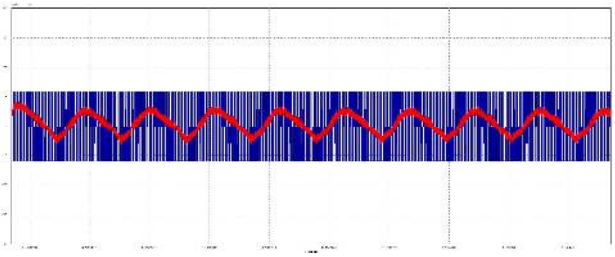


Fig. 5. Block diagram of the vector control scheme.



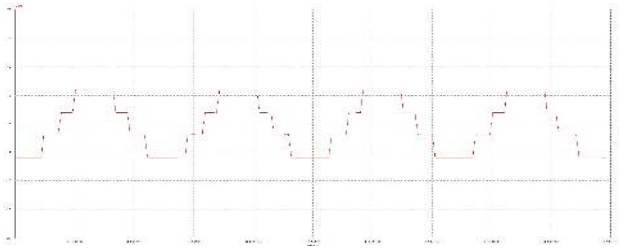
(a) CSVPWM algorithm.



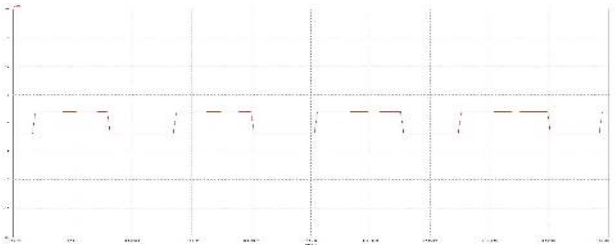
(b) Proposed AZSPWM algorithm.

Fig. 6. Simulation waveforms of the line-to-line voltage (blue, 10V/div, 5ms/div) and output current (red, 10A/div, 5ms/div).

when adopting the CSVPWM algorithm and the proposed AZSPWM algorithm, respectively. When the proposed AZSPWM algorithm is used, the peak value of the CMV decreases from 12V to 4V, which is 1/3 that of the CSVPWM algorithm. When the applied time for one of the two active vectors that form the switching patterns is considerably small in the CSVPWM algorithm, the dv/dt of the CMV could be increased rapidly, leading to an increase in the peak value of the CMC. However, because the pulse of the CMV

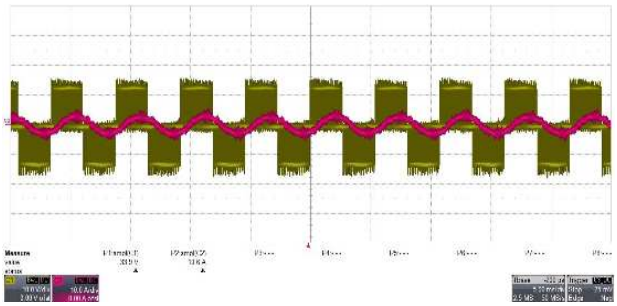


(a) CSVPWM algorithm.

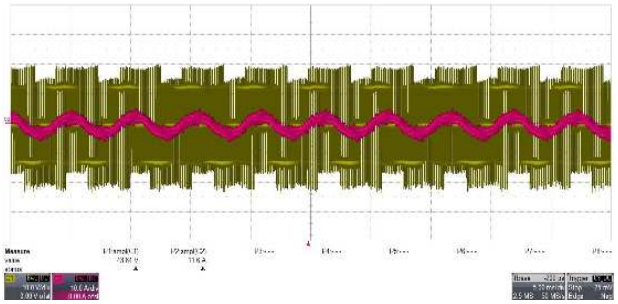


(b) Proposed AZSPWM algorithm.

Fig. 7. Simulation waveform of the CMV (red, 5V/div, 20us/div).



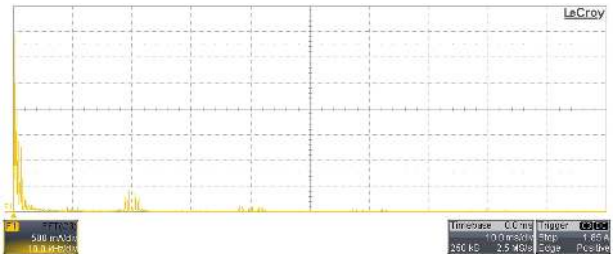
(a) CSVPWM algorithm.



(b) Proposed AZSPWM algorithm.

Fig. 8. Experimental waveforms of the line-to-line voltage (yellow, 10V/div, 5ms/div) and output current (red, 10A/div, 5ms/div).

alternately rises and falls in the proposed AZSPWM, an increase in the dv/dt of the CMV can be prevented. Therefore, an increase in the peak value of the CMC can be prevented in the proposed AZSPWM. Moreover, it is shown that for the proposed AZSPWM algorithm, the number of steps in the CMV is less than that of the CSVPWM algorithm, leading to a reduction in the rms value of the CMC. From these results, it can be observed that the proposed AZSPWM algorithm reduces the peak and rms values of both the CMV and the CMC, leading to a reduction in the EMI noise [17].



(a) CSVPWM algorithm.

(b) Proposed AZSPWM algorithm.

Fig. 9. FFT waveforms of the output current (yellow, 500mA/div, 10kHz/div).

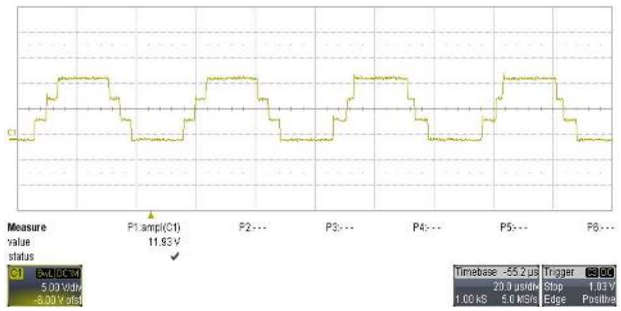
Fig. 8 shows experimental waveforms of the line-to-line voltage and output current of phase-a in the CSVPWM algorithm and in the proposed AZSPWM algorithm, respectively.

Fig. 9 shows FFT waveforms of the output current of phase-a for the CSVPWM algorithm and the proposed AZSPWM algorithm, and the FFT result is summarized in Table V. From Table V, it can be seen that the amplitude of the current at the switching frequency increased from $0.45[A_{peak}]$ of the CSVPWM algorithm to $0.96[A_{peak}]$ of the proposed AZSPWM algorithm. This phenomenon is an expected result, which also occurs in AZSPWM1-3 algorithms [11], [13], [14]. The two algorithms produce on average the same reference voltage vector during a switching period. However, in the proposed AZSPWM algorithm, because two active opposite voltage vectors that are far from the reference voltage vector are utilized instead of real zero voltage vectors (V_0 and V_7), the instantaneous error voltage vector of the proposed AZSPWM algorithm is greater than that of the CSVPWM algorithm [11]. Since the frequency of the error voltage vector is the same as the switching frequency, the amplitude of the current at the switching frequency is increased.

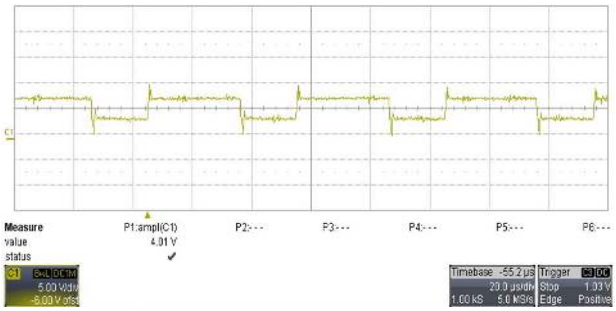
Since the tests were carried out under no-load conditions, the increase in the current amplitude at the switching frequency could be seen clearly. However, under rated-load conditions, because the amplitude of the current at the fundamental frequency is quite large (approximately $140[A_{peak}]$ in the utilized system), the increase in the current amplitude at the switching frequency becomes relatively small. Moreover, it can be seen that there is no significant difference in the amplitude at double the switching

TABLE V
FFT RESULTS OF THE OUTPUT CURRENT

	CSVPWM	PROPOSED AZSPWM
Fundamental frequency(180Hz)	3.42[A_{peak}]	3.23[A_{peak}]
Switching frequency(20kHz)	0.45[A_{peak}]	0.96[A_{peak}]
Double switching frequency(40kHz)	0.12[A_{peak}]	0.13[A_{peak}]



(a) CSVPWM algorithm.



(b) Proposed AZSPWM algorithm.

Fig. 10. Experimental waveform of the CMV (yellow, 5V/div, 20us/div).

frequency. Therefore, the effects of harmonics on the system can be considered to be negligible.

In Fig. 10, experimental waveforms of the CMV are presented when adopting the CSVPWM algorithm and the proposed AZSPWM algorithm, respectively. When the proposed AZSPWM algorithm is used, the peak value of the CMV decreased from 11.93V to 4.01V, corresponding to approximately 1/3 that of the CSVPWM algorithm.

As a result, the amplitude of the current at the switching frequency increases at the expense of a decrease in the common mode voltage. However, because this increase in the current amplitude can be considered to be very small under the rated-load condition, it is expected that the proposed AZSPWM algorithm can be used in systems where the EMC performance is significant.

VII. CONCLUSIONS

In this paper, a new AZSPWM algorithm that can reduce CMV and has the lowest number of switchings in three-phase ac motor inverter systems is proposed. From the theory, it was deduced that the proposed AZSPWM algorithm can reduce the CMV by using only active vectors, which is similar to AZSPWM1-3 algorithms. The CSVPWM algorithm and the AZSPWM1-3 algorithms were analyzed and compared in terms of the total number of switchings that leads to heat loss. From this analysis, it was observed that the proposed AZSPWM algorithm, like the CSVPWM algorithm, has the lowest number of switchings. The validity of the proposed AZSPWM algorithm was verified using simulation and experimental results. It can be seen that the proposed AZSPWM algorithm is more competitive than the CSVPWM algorithm with respect to EMI noise and it is more competitive than the AZSPWM1-3 algorithms with respect to heat performance.

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