RESEARCH   **Open Access**

A new approach of presenting reversible logic gate in nanoscale

Ali Newaz Bahar[1*], Sajjad Waheed[1] and Nazir Hossain[2]

Abstract

Conventional lithography-based VLSI design technology deployed to optimize low-powered-computing and higher scale integration of semiconductor components. However, this downscaling trend confronts serious challenges of tunneling and leakage current increment to the Complementary Metal–Oxide–Semiconductor (CMOS) technology on nanoscale regimes. To resolve the physical restriction of the CMOS, Quantum-dot Cellular Automata (QCA) technology dedicates for the nanoscale technology that embrace a new information transformation technique. However, QCA is limited to the design of the sequential and combinational circuits only. This paper presents some highly scalable features reversible logic gate for the QCA technology. In addition, proposed layout compared with CMOS technology, offer a better reduction in size up to 233 times.

Keywords: Quantum-dot Cellular Automata (QCA); Complementary Metal Oxide Semiconductor (CMOS); Nanoscale reversible gate

Introduction

Over the years, the reversible logic has attained a great attention due to their ability of power minimization which is the main requirement in the low power VLSI design. This technology is a promising computing paradigm that has immense applications in emerging technologies such as quantum dot cellular automata, quantum computing, optical computing, DNA computing, optical information processing, etc. (Al-Rabadi 2004; Ma et al. 2008; Thapliyal and Ranganathan 2008; Thapliyal and Ranganathan 2009a; Thapliyal and Ranganathan 2010). In reversible circuits the input and output mapping is one-to-one that means every unique output vector is generated from each input vector, and vice versa. It has shown by (Landauer 1961) that the loss of every bit of information dissipates energy of $kTln2$ joules, where k is Boltzmann's constant and T is the absolute temperature. In room temperature T_R, the amount of heat generated due to one bit of information loss (Landauer 1961) is small, which is calculated as 2.9×10^{-21} joule, but is not negligible. Later on, (Bennett 1973) showed that the energy losses could be avertable; if the computation is carried out by reversible circuits.
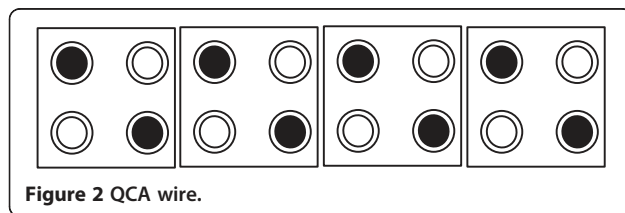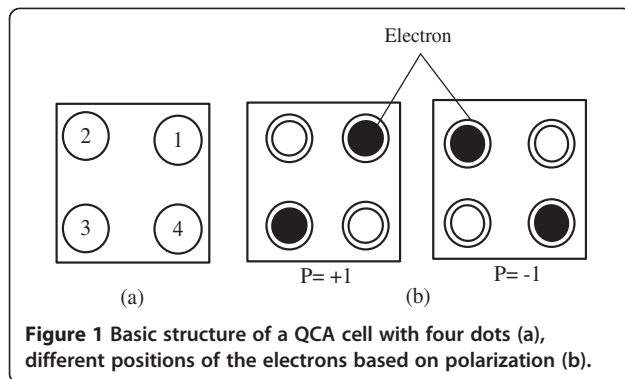
Now-a-days, CMOS technology is imminent to its physical boundary in downscaling and confronting critical challenges of designing ultra low power consuming computational devices. This projected the expectation to go looking new technologies that offer emerging solutions. One of the alternatives is known as Quantum-dot Cellular Automata (QCA) (Lent et al. 1993a; Lent et al. 1993b) which has recently been recognized as one of the top emerging technologies with potential applications in future computing (Orlov et al. 1997; Wilson et al. 2002) for its express speed, nanoscale integration and ultra low power consumption in various computational applications (Lent et al. 1993a).

Molecular QCA can operate at room temperature shown in (Lent et al. 2003; Wang and Lieberman 2004). Since the emancipation of QCA, a number of QCA-based logic circuits have been proposed based on majority voter gate, inverter and QCA wires. A lot of QCA based combinational (Azghadi et al. 2007; Cho and Swartzlander 2007; Cho and Swartzlander 2009; Gin et al. 1999; Hänninen and Takala 2010; Ke-ming and Yin-shui 2007; Kim et al. 2007; Mardiris and Karafyllidis 2010; Navi et al. 2010; Sara et al. 2012; Sayedsalehi et al.

* Correspondence: bahar_mitdu@yahoo.com
[1]Department of Information and Communication Technology, Mawlana Bhashani Science and Technology University, Tangail 1902, Bangladesh
Full list of author information is available at the end of the article

Figure 1 Basic structure of a QCA cell with four dots (a), different positions of the electrons based on polarization (b).

Figure 2 QCA wire.

2011; Srivastava and Bhanja 2007; Tougaw and Lent 1994; Vetteth et al. 2002; Wang et al. 2003; Zhang et al. 2005), sequential (Askari et al. 2008; Dehkordi et al. 2011; Ghosh et al. 2013; Huang et al. 2007; Sen et al. 2013; Vankamamidi et al. 2008; Venkataramani et al. 2008; Wu et al. 2014; Xiao et al. 2012; Yang et al. 2010) circuits have been proposed in recent years. However, reversible logic circuit designs (Bahar et al. 2013; Shah et al. 2012) in QCA are still unexplored research area. In this paper, four novel QCA circuit layouts of reversible logic gate have been presented and their functionality has been verified using the QCADesigner (Walus et al. 2004).

Material and methods

A Quantum Cellular Automata, one of the emerging nanotechnologies was first introduced by (Lent et al. 1993a) which encodes information based on position of

electrons. The basic element of a QCA based device is the squared cell with two mobile electrons and two quantum dots (Amlani et al. 1999; Ling-gang et al. 2005) shown in Figure 1. Based on the occupied electron's position, a QCA cell has two different types of polarization, $P = +1$ or binary 1 and $P = -1$ or binary 0 (Lent and Tougaw 1997). A cell polarization p is +1 if the electrons are occupied the position 1 and 3, similarly a cell polarization p is -1 in the case of electrons are occupied the position 2 and 4. The equation for the cell polarization (Lent and Tougaw 1997) is given below:

$$P = \frac{(\rho_2 + \rho_4) - (\rho_1 + \rho_3)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \tag{1}$$

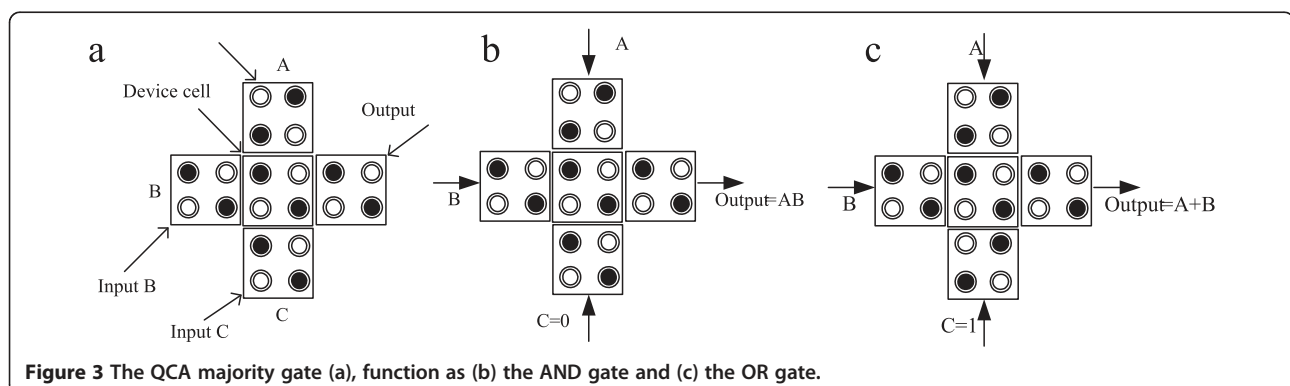Where, ρ_i denotes the electronic charge at dot i.

The QCA based design consists of a wire, a 3-input majority voter gate, and an inverter. An array of cells arranged one after another makes up the QCA wire, as shown in Figure 2. In the QCA wire, the polarization of each cell is affected by the electrostatic forces generated through neighboring cells. Thus, information propagates from one cell to another by through the QCA wires.
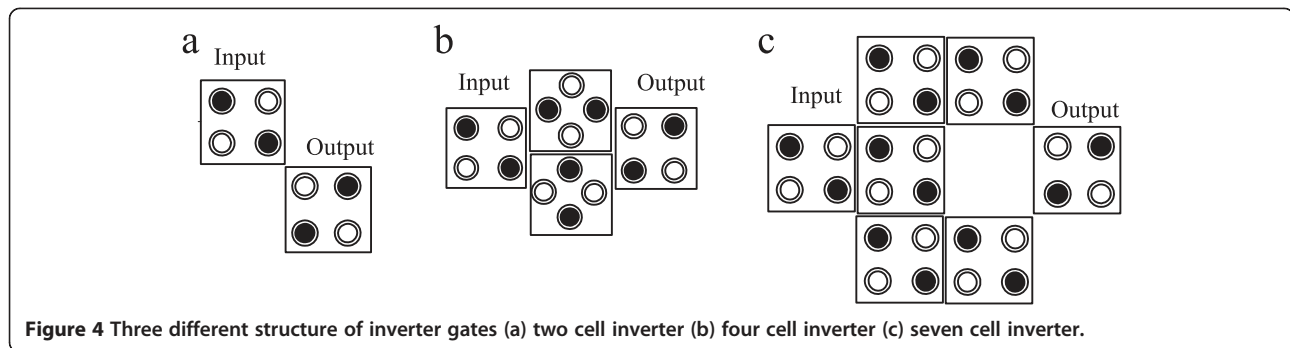
The 3-input majority gate has five cells: three inputs, a middle cell, and one output shown in the Figure 3 (a). The middle cell of the 3 input majority gates switches major polarization and maintains a consistent output. If the polarization of one of the 3-input cells is constant to $P = -1$ or $P = +1$ then this gate can be programmed to function as a 2-input AND or a 2-input OR gates, respectively shown in the Figure 3 (b) and (c).

In the Figure 4 shows the variety module of the inverting gate in the QCA. Seven cells inverter in the Figure 4 (c) operate appropriately in all various circuits.

Proposed circuits and presentation

A reversible logic gate is one that has *n* input *n* output; with one-to-one mapping that means it determines the outputs from the inputs. It also helps the inputs to be uniquely recovered or reconstructed from the outputs.

Figure 3 The QCA majority gate (a), function as (b) the AND gate and (c) the OR gate.

Figure 4 Three different structure of inverter gates (a) two cell inverter (b) four cell inverter (c) seven cell inverter.

NFT gate

The New Fault Tolerant (NFT) gate is one of the basic 3 × 3 parity preserving (Haghparast and Navi 2008) reversible logic gates having the inputs and output mapping as $P = A \oplus B$, $Q = \bar{B}C \oplus A\bar{C}$ and $R = BC \oplus A\bar{C}$, where the input vector is I (A, B, C) and the output vector is
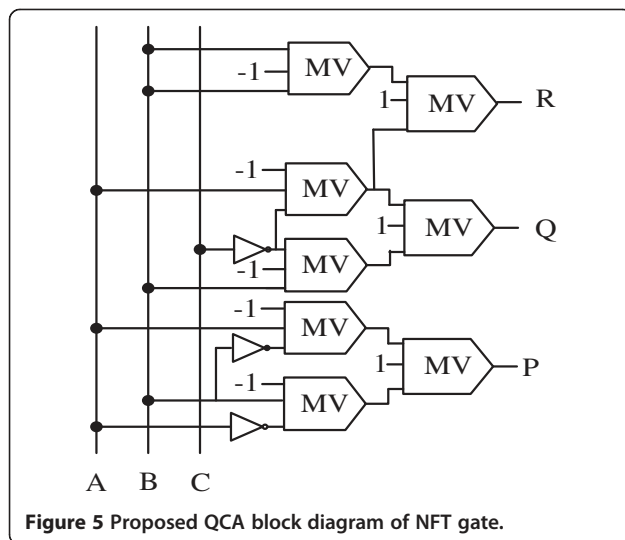
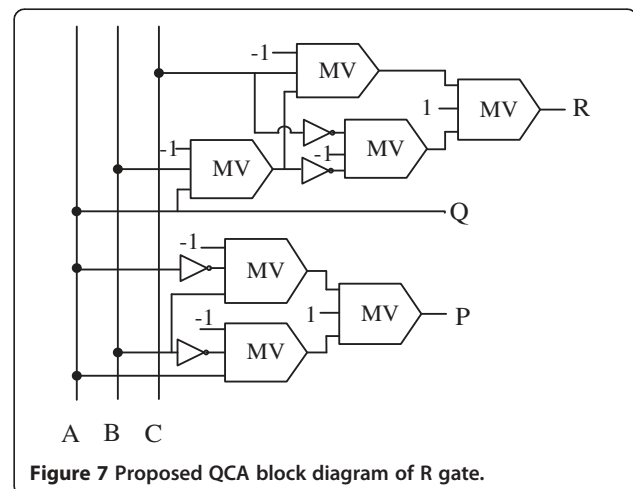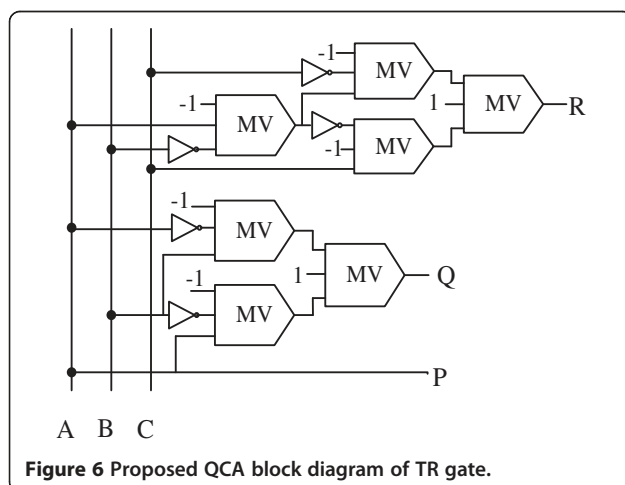O (P, Q, R). The Figure 5 shows the QCA representation of this gate.

TR gate

The TR gate is a 3-input, 3-output, reversible gate (Thapliyal and Ranganathan 2009b) having inputs to output mapping as $P = A$, $Q = A \oplus B$ and $R = (A\bar{B}) \oplus C$, where A, B, C are the inputs and P, Q, R are the outputs, respectively, as shown in Figure 6.
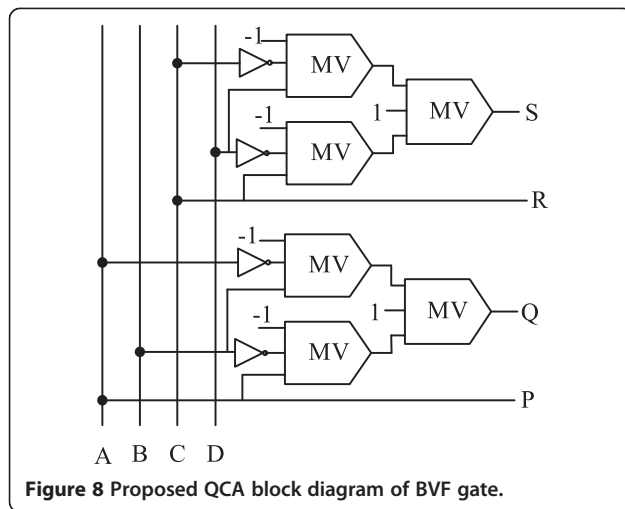
R gate

The R gate is a 3-input, 3-output, reversible gate (Vasudevan et al. 2006). Figure 7 shows the block diagram of this gate in QCA. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined as $P = A \oplus B$, $Q = A$ and $R = AB \oplus \bar{C}$.

BVF gate

BVF gates also known as 4 × 4 double XOR reversible logic gates (Bhagyalakshmi and Venkatesha 2010). This can be used for duplication of the required inputs to meet the fan-out requirements. The input vector is I (A, B, C, D), the output vector is O (P, Q, R and S) and the

Figure 5 Proposed QCA block diagram of NFT gate.

Figure 6 Proposed QCA block diagram of TR gate.

Figure 7 Proposed QCA block diagram of R gate.

Figure 8 Proposed QCA block diagram of BVF gate.

output is defined as $P = A$, $Q = A \oplus B$, $R = C$ and $S = C \oplus D$ shown in Figure 8.

Simulations and result analysis

Our proposed circuits have been simulated using the QCADesigner (Walus et al. 2004) a common and powerful simulation tool for QCA circuits. Bistable Approximation has been applied for simulating the proposed circuit with below parameters: cell size = 18 nm, number of

samples = 50000, convergence tolerance = 0.0000100, radius of effect = 65.000000 nm, relative permittivity = 12.900000, clock high = $9.800000e^{-022}$ J, clock low = $3.800000e^{-023}$J, clock shift = 0, clock amplitude factor = 2.000000, layer separation = 11.500000 and maximum iterations per sample = 100. Most of the above mentioned parameters are default for Bistable Approximation. The circuit layout of NFT, TR, R and BVF gates are shown in Figure 9. Here, the input cells are denoted by A, B, C and D, output cells are P, Q, R and S; and the two polarizations, $P = +1$ is denoted by 1 and $P = -1$ denoted by -1. Figure 10 shows the input and output waveforms of our proposed gate in QCADesigner.

Table 1 shows the different parameters of the proposed gates. From the above table it is clear that QCA technology provides highly integrated designing paradigm over CMOS technology. Covered areas in both CMOS and QCA technologies with improvements are shown in Figure 11. Here, Microwind and Dsch3 has been employed to design and calculate covered area for CMOS design. Moreover, the number of cells and majority voter gates are the total number of cells and majority voter gates required to design a gate.

Conclusion

Quantum-dot cellular automata, one of the promising nanotechnologies that are appropriate for the design of
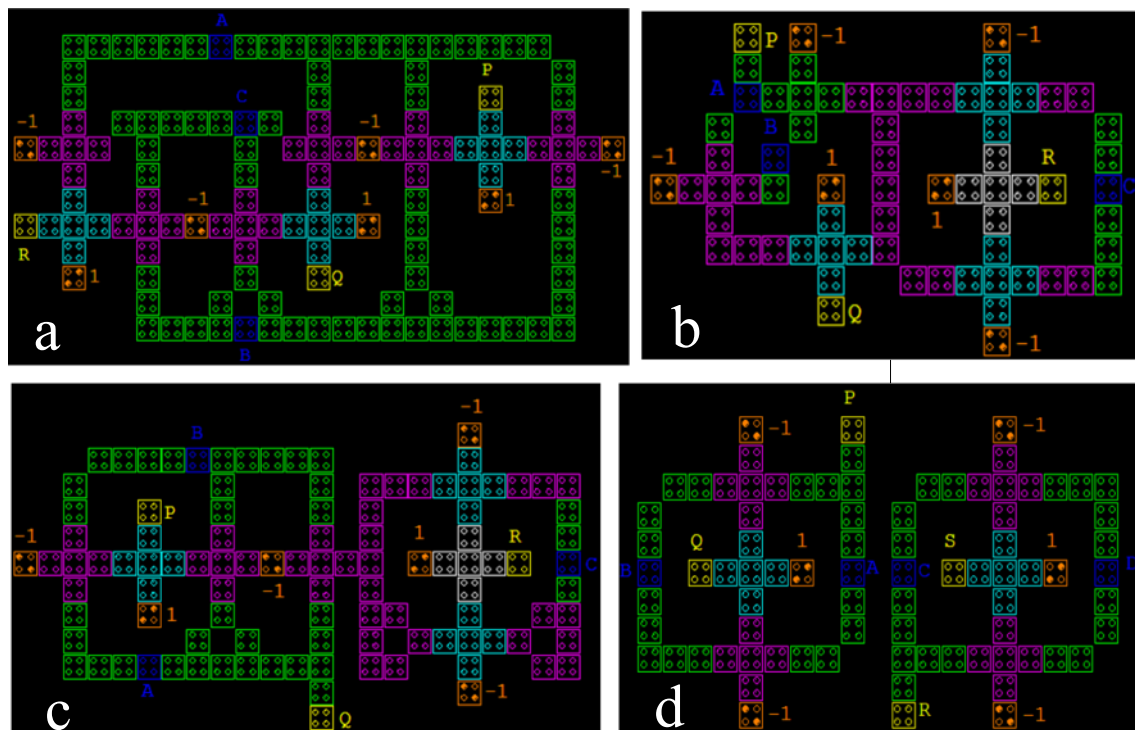

Figure 9 QCA simulated circuit layout of (a) NFT gate, (b) TR gate, (c) R gate, and (d) BVF gate.
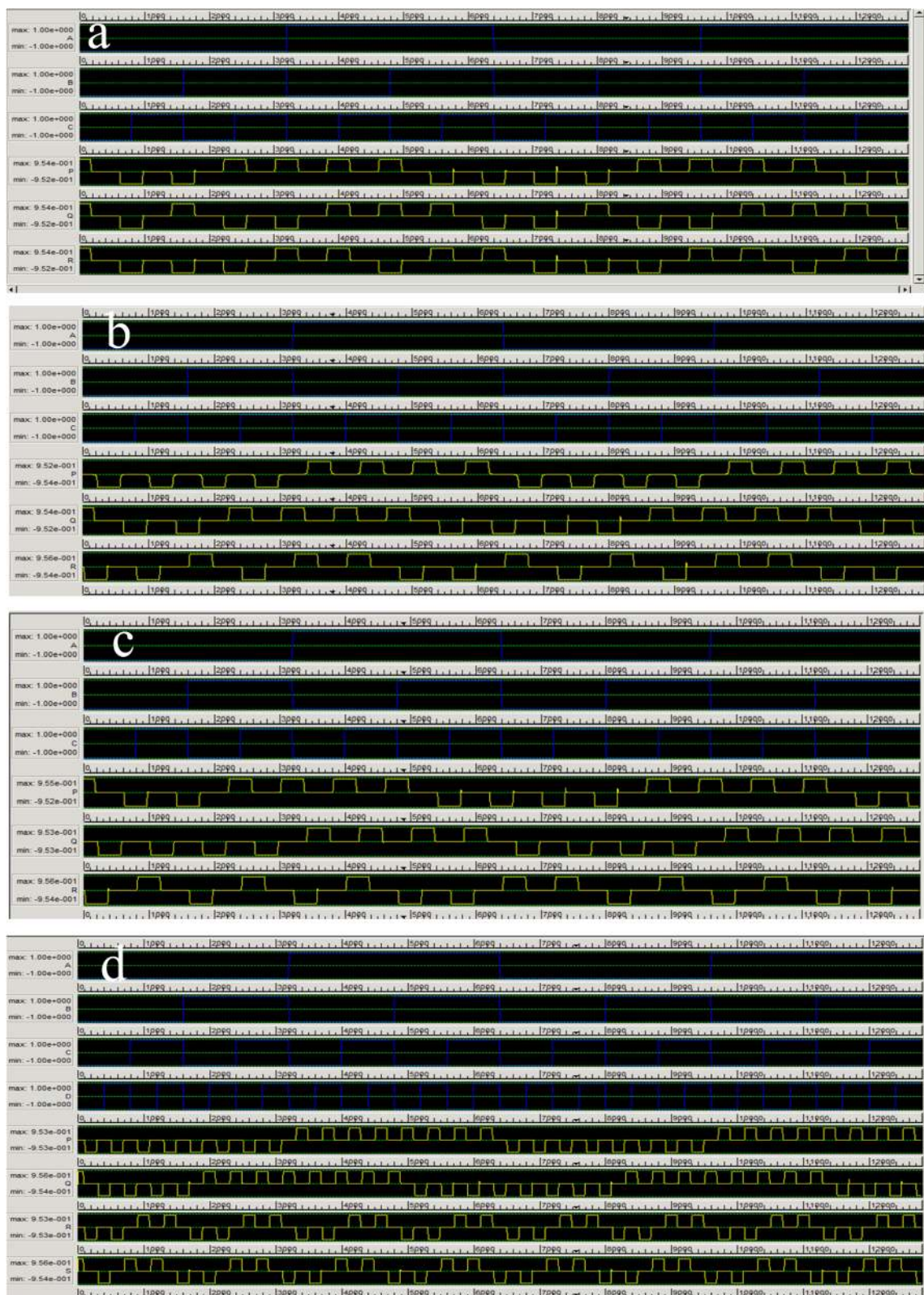
Figure 10 Input output waveforms of (a) NFT gate, (b) TR gate, (c) R gate, and (d) BVF gate.

Table 1 Performance analysis of proposed gates

Parameters	NFT gate	TR gate	R gate	BVF gate
Number of cells	128	68	105	82
Number of majority voter gate	9	6	6	6
Time delay (clock cycle)	0.5	0.75	0.75	0.5
Covered area (size) in QCA (μm^2)	0.142	0.079	0.126	0.10
Covered area (size) in CMOS (μm^2)	33.02	12.3	12.3	8.3
Improvement (in times)	233	156	98	83

	NFT Gate	TR Gate	R Gate	BVF Gate
■ Improvement (in times)	233	156	98	83
■ Covered area in QCA (µm2)	0.142	0.079	0.126	0.1
■ Covered area in CMOS (µm2)	33.2	12.3	12.3	8.3
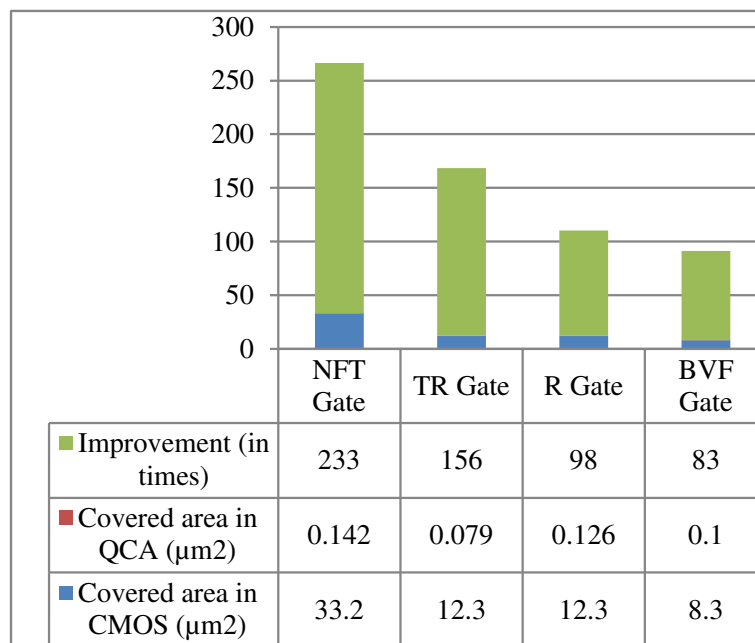
Figure 11 Comparative figures for covered area (size) of QCA and CMOS with improvement.

highly scalable logic circuits. A number of QCA-based reversible logic gates, which are significantly smaller size than CMOS have been presented here. In addition, QCA design accomplished by the basic gate and logic circuit in which less area is required to make a device. Thus the new device will consume less power and increase device performance. Since nanotechnology has high demand in the market, this QCA technology can be best suited substitute of CMOS based technology.

Competing interests
The authors declare that they have no competing interests.

Authors' contributions
ANB designed the logic of proposed circuits and simulated them using QCAdesigner, Microwind and Dsch3. SW and NH helped in literature study and drafting the manuscript. All authors read and approved the manuscript.

Acknowledgements
We express our thanks to AH, Ahsan Habib, for his valuable guideline in preparing manuscript.

Author details
[1]Department of Information and Communication Technology, Mawlana Bhashani Science and Technology University, Tangail 1902, Bangladesh. [2]Department of Physics, University of South Dakota, Vermillion, SD 57069, USA.

References
Al-Rabadi AN (2004) Reversible logic synthesis: from fundamentals to quantum computing. Springer, Heidelberg
Amlani I, Orlov AO, Toth G, Bernstein GH, Lent CS, Snider GL (1999) Digital logic gate using quantum-dot cellular automata. Science 284(5412):289–291
Askari M, Taghizadeh M, Fardad K (2008) Design and analysis of a sequential ring counter for qca implementation. In: International Conference on Computer and Communication Engineering. IEEE, Kuala Lumpur, 13-15 May 2008
Azghadi MR, Kavehei O, Navi K (2007) A novel design for quantum-dot cellular automata cells and full adders. J Appl Sci 7(22):3460–3468
Bahar AN, Habib M, Biswas NK (2013) A novel presentation of toffoli gate in quantum-dot cellular automata (QCA). Int J Comput Appl 82(10):1–4, doi:10.5120/14149-2243
Bennett CH (1973) Logical reversibility of computation. IBM J Res Dev 17(6):525–532
Bhagyalakshmi H, Venkatesha M (2010) An improved design of a multiplier using reversible logic gates. Int J Eng Sci Technol 2(8):3838–3845

Cho H, Swartzlander EE (2007) Adder designs and analyses for quantum-dot cellular automata. Nanotechnol IEEE Trans 6(3):374–383

Cho H, Swartzlander EE (2009) Adder and multiplier design in quantum-dot cellular automata. IEEE Trans Comput 58(6):721–727

Dehkordi MA, Shamsabadi AS, Ghahfarokhi BS, Vafaei A (2011) Novel ram cell designs based on inherent capabilities of quantum-dot cellular automata. Microelectron J 42(5):701–708

Ghosh B, Gupta S, Kumari S, Salimath A (2013) Novel design of combinational and sequential logical structures in quantum dot cellular automata. J Nanostructure Chem 3(1):1–9

Gin A, Williams S, Meng H, Tougaw PD (1999) Hierarchical design of quantum-dot cellular automata devices. J Appl Phys 85(7):3713–3720

Haghparast M, Navi K (2008) A novel fault tolerant reversible gate for nanotechnology based systems. Am J Appl Sci 5(5):519

Hänninen I, Takala J (2010) Binary adders on quantum-dot cellular automata. Sci J Circ Syst Signal Process 58(1):87–103

Huang J, Momenzadeh M, Lombardi F (2007) Design of sequential circuits by quantum-dot cellular automata. Microelectron J 38(4):525–537

Ke-ming Q, Yin-shui X (2007) Quantum-dots cellular automata comparator. In: 7th International Conference on ASIC. IEEE, Guilin, 22-25 Oct. 2007

Kim K, Wu K, Karri R (2007) The robust qca adder designs using composable qca building blocks. IEEE Trans Comput Aided Des Integrated Circ Syst 26(1):176–183

Landauer R (1961) Irreversibility and heat generation in the computing process. IBM J Res Dev 5(3):183–191

Lent CS, Tougaw PD (1997) A device architecture for computing with quantum dots. Proc IEEE 85(4):541–557

Lent CS, Tougaw PD, Porod W (1993a) Bistable saturation in coupled quantum dots for quantum cellular automata. Appl Phys Lett 62(7):714–716

Lent CS, Tougaw PD, Porod W, Bernstein GH (1993b) Quantum cellular automata. Nanotechnology 4(1):49

Lent CS, Isaksen B, Lieberman M (2003) Molecular quantum-dot cellular automata. J Am Chem Soc 125(4):1056–1063

Ling-gang Z, Qing-kang W, Yong-bing D (2005) A new phenomenon of quantum-dot cellular automata. J Zhejiang University Sci A 6(10):1090–1094, doi:10.1007/BF02842231

Ma X, Huang J, Metra C, Lombardi F (2008) Reversible gates and testability of one dimensional arrays of molecular qca. J Electron Test 24(1–3):297–311

Mardiris VA, Karafyllidis IG (2010) Design and simulation of modular 2^n to 1 quantum-dot cellular automata (QCA) multiplexers. Int J Circ Theor Appl 38:771–785, doi:10.1002/cta.595

Navi K, Farazkish R, Sayedsalehi S, Azghadi MR (2010) A new quantum-dot cellular automata full-adder. Microelectron J 41(12):820–826

Orlov A, Amlani I, Bernstein G, Lent C, Snider G (1997) Realization of a functional cell for quantum-dot cellular automata. Science 277(5328):928–930

Sara H, Mohammad T, Keivan N (2012) An efficient quantum-dot cellular automata full-adder. Sci Res Essays 7(2):177–189, doi:10.5897/SRE11.1182

Sayedsalehi S, Moaiyeri MH, Navi K (2011) Novel efficient adder circuits for quantum-dot cellular automata. J Comput Theor Nanosci 8(9):1769–1775

Sen B, Goswami M, Some S, Sikdar BK (2013) Design of sequential circuits in multilayer qca structure. In: International Symposium on Electronic System Design (ISED). IEEE, Singapore, 10-12 December 2013

Shah N, Khanday F, Iqbal J (2012) Quantum-dot cellular automata (qca) design of multi-function reversible logic gate. Communications in Information Science and Management Engineering

Srivastava S, Bhanja S (2007) Hierarchical probabilistic macromodeling for qca circuits. IEEE Trans Comput 56(2):174–190

Thapliyal H, Ranganathan N (2008) Testable reversible latches for molecular qca. In: 8th IEEE Conference on Nanotechnology, NANO'08. IEEE, Arlington, TX, 18-21 August 2008

Thapliyal H, Ranganathan N (2009a) Conservative qca gate (cqca) for designing concurrently testable molecular qca circuits. In: 2009 22nd International Conference on VLSI Design. IEEE, New Delhi, 5-9 January 2009

Thapliyal H, Ranganathan N (2009b) Design of efficient reversible binary subtractors based on a new reversible gate. In: IEEE Computer Society Annual Symposium on VLSI, ISVLSI'09. IEEE, Tampa, FL, 13-15 May 2009

Thapliyal H, Ranganathan N (2010) Reversible logic-based concurrently testable latches for molecular qca. IEEE Trans Nanotechnol 9(1):62–69

Tougaw PD, Lent CS (1994) Logical devices implemented using quantum cellular automata. J Appl Phys 75(3):1818–1825

Vankamamidi V, Ottavi M, Lombardi F (2008) A serial memory by quantum-dot cellular automata (qca). IEEE Trans Comput 57(5):606–618

Vasudevan DP, Lala PK, Di J, Parkerson JP (2006) Reversible-logic design with online testability. Instrum Meas IEEE Trans 55(2):406–414

Venkataramani P, Srivastava S, and Bhanja S (2008) Sequential circuit design in quantum-dot cellular automata. Nanotechnology, 2008. NANO'08. 8th IEEE Conference on, IEEE, pp. 534-537

Vetteth A, Walus K, Dimitrov VS, Jullien GA (2002) Quantum-dot cellular automata carry-look-ahead adder and barrel shifter. IEEE Emerging Telecommunications Technologies Conference, pp. 2-4

Walus K, Dysart TJ, Jullien GA, Budiman RA (2004) Qcadesigner: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans Nanotechnol 3(1):26–31

Wang Y, Lieberman M (2004) Thermodynamic behavior of molecular-scale quantum-dot cellular automata (qca) wires and logic devices. IEEE Trans Nanotechnol 3(3):368–376

Wang W, Walus K, Jullien GA (2003) Quantum-dot cellular automata adders. In: 2003 Third IEEE Conference on Nanotechnology, NANO 2003, IEEE, vol. 1, pp. 461-464

Wilson M, Kannangara K, Smith G, Simmons M, Raguse B (2002) Nanotechnology: basic science and emerging technologies. CRC Press, Boca Raton, Florida

Wu CB, Xie GJ, Xiang YL, Lv HJ (2014) Design and simulation of dual-edge triggered sequential circuits in quantum-dot cellular automata. J Comput Theor Nanosci 11(7):1620–1626

Xiao LR, Chen XX, Ying SY (2012) Design of dual-edge triggered flip-flops based on quantum-dot cellular automata. J Zhejiang University Sci C 13(5):385–392

Yang X, Cai L, Zhao X, Zhang N (2010) Design and simulation of sequential circuits in quantum-dot cellular automata: falling edge-triggered flip-flop and counter study. Microelectron J 41(1):56–63

Zhang R, Walus K, Wang W, Jullien GA (2005) Performance comparison of quantum-dot cellular automata adders. In: IEEE International Symposium on Circuits and Systems, ISCAS 2005, IEEE, vol. 03, pp. 2522-2526