A NEW ARCHITECTURE FOR LOW-VOLTAGE LOW-PHASE-NOISE HIGH-FREQUENCY CMOS LC VOLTAGE-CONTROLLED OSCILLATOR

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A NEW ARCHITECTURE FOR LOW-VOLTAGE LOW-PHASE-NOISE HIGH- FREQUENCY CMOS LC VOLTAGE-CONTROLLED OSCILLATOR

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SUMMARY

Presented in this work is a novel design technique for a low-phase-noise high-frequency CMOS voltage-controlled oscillator. Phase noise is generated from electrical noise near DC, the oscillation frequency, and its harmonics. In CMOS technology, low-frequency flicker noise dominates the close-in phase noise of the VCO. The proposed technique minimizes the VCO phase noise by seeking to eliminate the effect of flicker noise on the phase noise. This is accomplished by canceling out the DC component of the impulse sensitivity function (ISF) corresponding to each flicker-noise source, thus preventing the up-conversion of low-frequency noise into phase noise. The proposed circuit topology is a modified version of the complementary cross-coupled transconductance VCO, where additional feedback paths are introduced such that a designer can choose the feedback ratios, transistor sizes, and bias voltages to achieve the previously mentioned design objectives. A step-by-step design algorithm is presented along with a MATLAB script to aid in the computation of the ISFs and the phase noise of the VCO. Using this algorithm, a 5-GHz VCO was designed and fabricated in a 0.18μm CMOS process, and then tested for comparison with simulated results.

CHAPTER 1
INTRODUCTION

1.1 Motivation

The growing demand for high-speed wireless connectivity has accelerated the development of data-centric third-generation (3G) services, particularly the wireless local area network (WLAN) communications protocols such as the Institute of Electrical and Electronics Engineers (IEEE) standard 802.11a and the European Telecommunications Standardization Institute (ETSI) standard HiperLAN2. To support the increasingly faster data rates and to combat the less favorable propagation conditions at higher carrier frequencies, these standards employ the more complex modulation scheme of orthogonal frequency division multiplexing (OFDM). With OFDM, the carrier is subdivided into several individually modulated orthogonal subcarriers, all of which are simultaneously transmitted [1]-[4]. However, a higher data rate is often accompanied by more sensitivity to phase errors for a particular modulation scheme. This increased sensitivity is inevitably translated into more stringent phase noise requirements for the voltage-controlled oscillator (VCO). The VCO is an integral and critical part of a phase-locked loop (PLL) or a frequency synthesizer often found in the transceivers of modern communications systems.

At the same time, continuing advances in the complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technologies have allowed low-cost practical realization of the transceiver designs in the multi-gigahertz frequency range.

Unfortunately, the supply voltages for these advanced CMOS technologies are also proportionately reduced so as not to damage the thin gate-oxide layer of the active devices. For VCO circuits, the lower supply voltage translates to lower output voltage swing, which further exacerbates the difficulty of achieving low phase-noise performance. Adding to the problem is the cost sensitive consumer market, which has driven the desirability of a fully-integrated design for the VCO.

In CMOS technologies, a fully-integrated VCO can be implemented as a ring oscillator, an active inductor-capacitor (LC) oscillator, or a passive LC oscillator. A VCO using a transmission-line resonator can also be realized for better phase-noise performance, but it is generally not considered because of the large-area requirement. The ring oscillators are typically implemented with an odd number of inverter stages connected in series, forming a positive feedback configuration. They are attractive because of their ease of implementation and large tuning range. However, they suffer from poor phase-noise performance and are generally not suitable for communications applications. The active LC oscillators employ LC resonators as the frequency-determining elements, where the inductors are implemented with capacitance and active devices in a gyrator-C circuit topology. The active inductors are capable of very large quality factors (Q). But the noise contribution from the active devices, causes the phase noise of the oscillator to be relatively high, compared to its passive counterpart, and is therefore not suitable for low-noise design applications [5], [6]. Similarly, the passive LC oscillators employ passive LC resonators as their frequency-determining elements. Of this type of circuit, the complementary cross-coupled transconductor LC VCO of Figure 1.1(a) is arguably the most ubiquitous circuit topology because it can be implemented entirely on-chip and it

provides reasonably good phase-noise performance. It is also attractive for low-power design resulting from sharing the bias current between the NMOS and PMOS transconductors. Its drawback is the relatively low output voltage swing because of the voltage drop across the bias current transistor M5. To alleviate this problem, it is possible to eliminate either the NMOS or the PMOS transconductor, as shown in Figure 1.1(b) [7], [8]. The output signal swing is increased, and the noise contribution from the active devices is lower (the number of transistors is halved). However, for the same bias current and operation in the current-limited regime, the output swing of the NMOS-only (PMOS-only) topology is theoretically only half that of the complementary circuit [9]-[11]. As a result, the phase-noise performance of the latter is generally more superior.

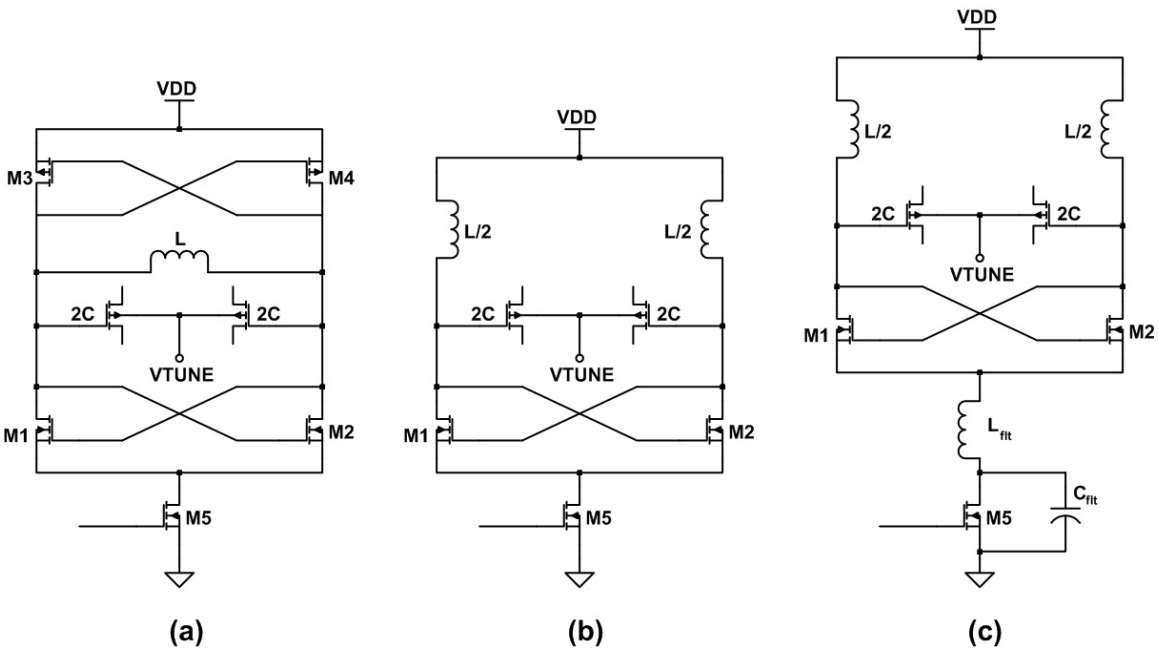

Figure 1.1 Schematic of the (a) complementary cross-coupled-transconductors CMOS LC VCO, (b) NMOS-transconductor-only CMOS LC VCO, and (c) VCO with tail current noise filter.

Phase noise can be improved by increasing the quality factor of the LC resonator, i.e., increasing the Q of the inductor (the Q of the varactor is generally much higher). This may be accomplished with the use of bond-wire inductance whose quality factor can be as great as 50 at 2 GHz [12]-[15]. However, this approach is not widely accepted in the industry because of the concern about the reproducibility and reliability of the bond-wire inductors. In addition, small values of inductance (less than 5 nH) are difficult to produce, making the design of high-frequency VCO (greater than 5 GHz) impractical. Another approach to increase the quality factor of the inductor is to fabricate the device in a thick insulating layer embedded in a separate silicon substrate [16]. The resulting isolation increases the Q of the embedded inductor by more than 300% relative to that of the equivalent on-chip device. The obvious drawback is the additional processing steps, and therefore higher cost. Albeit with less dramatic improvement, a transformer-based LC resonator, which is fully compatible with the CMOS process, can be used to achieve better quality factor [17]. The gain in Q is relatively small, approximately (1+k) where k is the coupling coefficient of the transformer [18], while the area penalty (60%) is fairly significant [19].

Alternatively, VCO phase-noise performance can also be improved with the use of various design techniques to minimize the effect of circuit noise. For the CMOS VCO shown in Figure 1.1(a) and (b), flicker noise of the bias transistor is the most dominant noise source because its 1/f characteristics generate very high close-in phase noise. In [20]-[22], inductive degeneration and capacitive filtering, as shown in Figure 1.1(c) are used to attenuate the noise around twice the resonant frequency ($2\omega_0$) at the drain of the bias transistor. Additionally, a large external inductor or capacitor, not shown in the

figure, is needed to filter out the low-frequency noise. A more elegant approach to reduce the flicker noise of the bias transistor is proposed in [23], where two identical bias transistors are switched on and off in a complementary fashion (Figure 1.2a). The switching action results in the transistor flicker noise being reduced by about 8 dB at 1 KHz, but the reduction is progressively less at higher frequencies (~2 dB at 100 KHz) [24]-[26]. Yet another approach to improve the VCO phase noise is to replace the bias transistor with poly-silicon resistors, as shown in Figure 1.2(b), thereby removing the dominant flicker noise source [27]. However, the flicker noise of the switching transistors remains and becomes major noise sources at low frequency. Additionally, the bias current needs to be regulated with digital control bits from a replica servo loop, and a large capacitor (75 pF) is necessary to suppress the resistor thermal noise. Table 1.1 summarizes the gain in phase-noise performance using the fore-mentioned flicker-noise reduction techniques.

Table 1.1 Summary of phase-noise performance gain by reducing flicker noise.

Reference	Power (mW)	f_0(Hz)	Δf(KHz)	Phase noise(dBc/Hz) @ Δf	
				Ref. VCO	Proposed VCO
[22]	12	1.8G	100	-95.5	-105.5
[23]	3.5	1.88G	10	-81	-87
			600	-126	-127.6
[27]	16.2	1.5G	10	-70	-88
			100	-100	-110
			600	-124	-126

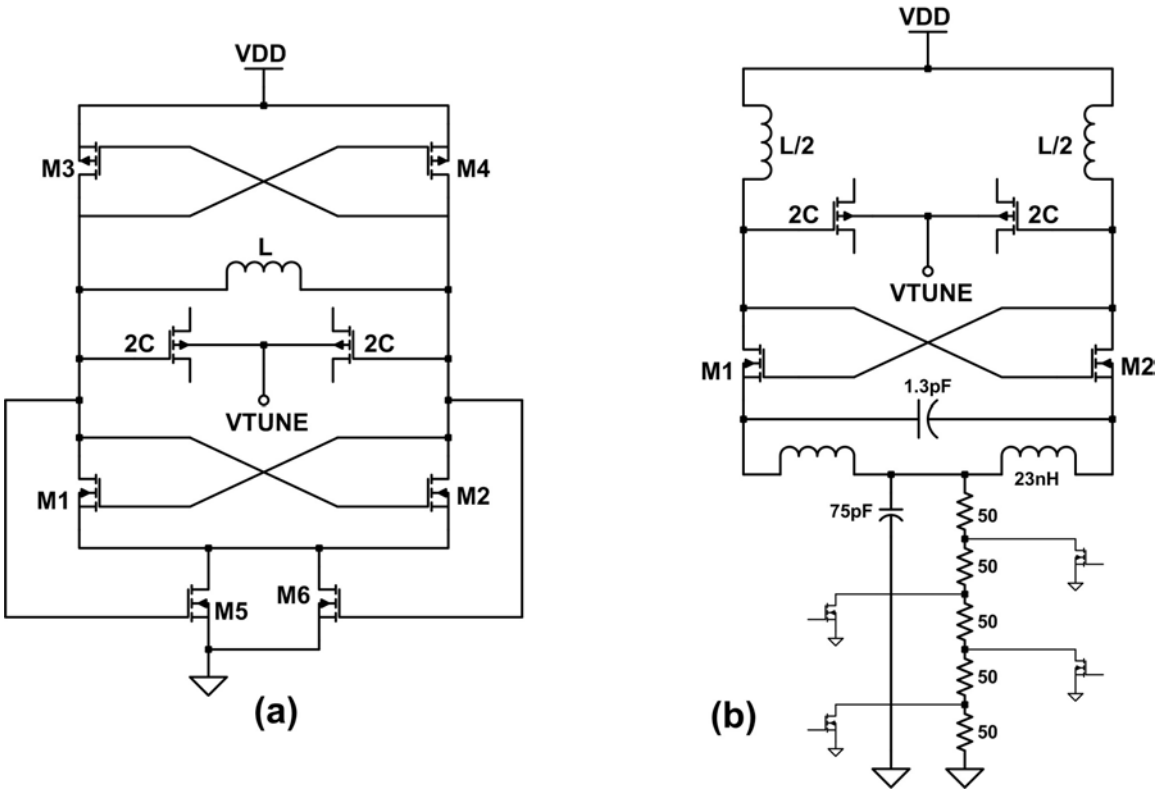

Figure 1.2 Schematic of proposed VCO in (a) [23] (b) [27].

1.2 Scope of Research

As demonstrated in the previous section, the phase noise of a CMOS LC VCO (Figure 1.1(a)) can be greatly improved by reducing the flicker noise of its bias transistor. Therefore, it is reasonable to expect that further improvement can be achieved by canceling out all flicker noise sources present in the VCO circuit, which will be the objective of this thesis. This noise cancellation technique is based on the linear time-variant phase noise model presented by Hajimiri and Lee in [28]-[30]. For each noise source in the circuit, there is a corresponding periodic impulse sensitivity function (ISF) describing the conversion mechanism of this circuit noise into phase noise. The VCO output excess phase caused by this source can be calculated by convolving its noise function with the

ISF. The VCO close-in phase noise is then proportional to the product of the DC component of the ISF and the integral of the low-frequency portion of the noise function. Therefore, if the circuit can be designed such that the ISF corresponding to each transistor noise source has no DC component, the flicker noise will not have any effect on the phase noise of the VCO. In order to achieve good noise cancellation result, an iterative design approach, requiring accurate phase-noise simulation methodology, is necessary. The simulation method involves a transient analysis to obtain the ISF of a noise source, several additional miscellaneous analyses to characterize this noise source and its cyclostationary properties if necessary, and a post-processing algorithm combining all simulated results to calculate the VCO phase noise exacted by this noise source. Finally yet importantly, the resulting circuit topology provides an additional benefit for quadrature VCO design. It allows capacitive coupling of the individual VCOs, thereby avoids any phase-noise degradation that exists in the typical parallel- or series-quadrature VCO topologies [31].

1.3 Thesis Organization

This thesis is divided into seven chapters. Chapter 1 discusses the motivation and challenges in low-phase-noise CMOS VCO design, and provides a summary of several high-performance circuit topologies found in recently published literature. Chapter 2 presents the theory of three different phase noise models, from which an optimal one is selected to aid in the design and simulation of the proposed VCO. Chapter 3 gives an overview of the various structures used in the implementation of high-quality-factor on-chip LC resonator. Chapter 4 provides a detailed circuit and phase noise analysis of the reference VCO, which is the ubiquitous cross-coupled transconductor VCO. Phase

noise reduction techniques, previously mentioned in chapter 1, are discussed in more details. Similarly, chapter 5 provides a detailed circuit and phase noise analysis of the proposed VCO. A systematic design procedure is included, and is used to design a low-phase-noise 5.5-GHz oscillator. Chapter 6 presents the simulated and experimental results of the reference VCO and the proposed oscillator. A comparison with recently published works is also provided. Finally, chapter 7 gives the conclusions, summary of contributions, and future work plan.

CHAPTER 2
OSCILLATOR PHASE NOISE

Phase noise is arguably the most critical parameter in the design of a high-performance VCO. In the frequency domain, it is defined as the noise power, near the fundamental component of oscillation, thus smearing the ideal shape of the Dirac-delta function at this frequency (Figure 2.1). If not properly controlled, phase noise can cause frequency instability, resulting in serious performance degradation such as intermodulation distortion and timing error in a communication system.

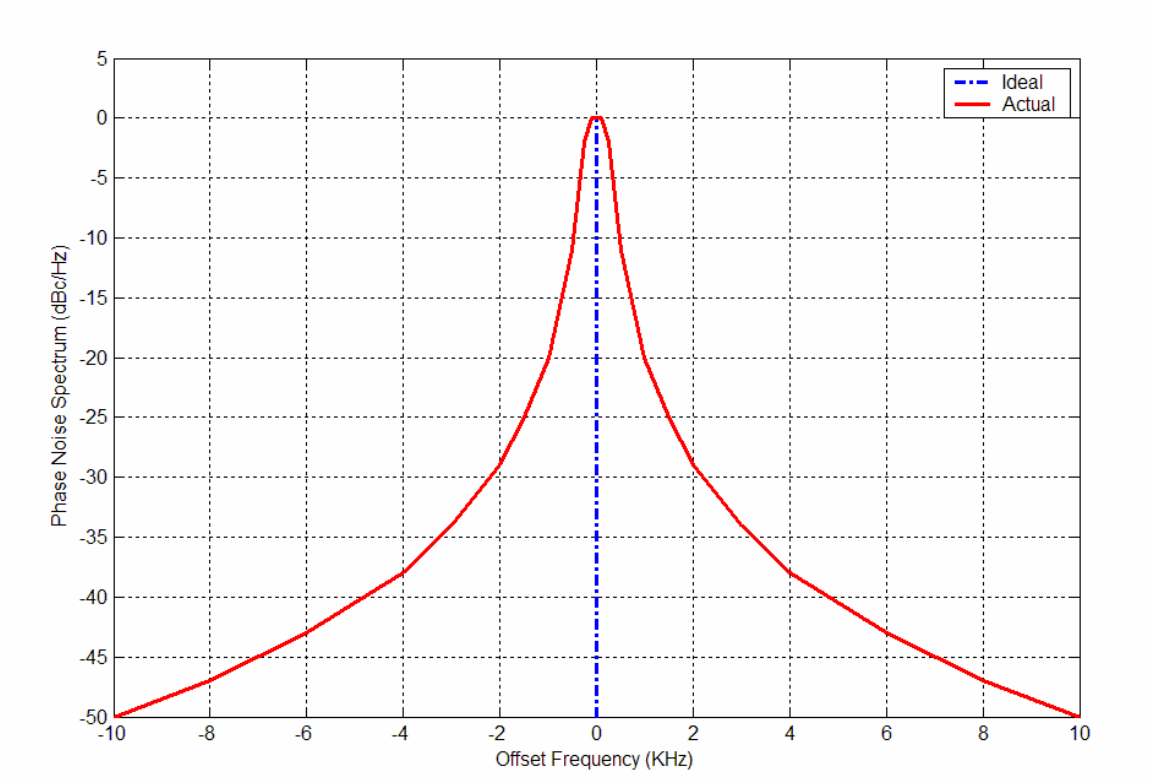

Figure 2.1 Phase noise spectrum of a typical 5-GHz CMOS oscillator.

Mathematically, it is defined as a zero-mean stochastic process $\phi(t)$ in the general expression for the output voltage of an oscillator (Equation 2.1). Its voltage power spectral density $S_{V\phi}(f)$ is typically measured with a spectrum analyzer, and the single-sideband phase noise spectral density is defined as this noise power relative to the fundamental power at oscillation frequency (Equation 2.2).

$$v_{osc}(t) = (V_m + \varepsilon(t)) \cdot \cos(\omega_0 t + \phi(t)) \tag{2.1}$$

$$\left(\frac{N_0}{P_0}\right)_{fm} = \frac{S_{V\phi}(f_0 \pm f_m)}{P_0} \tag{2.2}$$

Possibly the first published paper on VCO phase noise model is that by Leeson in [32]. It was a linear time-invariant (LTI) model, derived heuristically in the frequency domain for a positive feedback oscillator, and later expanded more rigorously by the work of others [5], [33]-[37]. The simplicity of this model, at the expense of accuracy, allows circuit designers to have direct insight into the fundamental of design tradeoffs. On the other end of the spectrum, nonlinear time-variant models, based on solid theoretical background, have been proposed with much better accuracy [38]-[40]. However, the intensive mathematical requirements will often cause the readers to lose sight of the important links between phase noise and circuit design parameters. Between these two extremes are the linear time-variant (LTV) models proposed in [28], [41], [42], which can produce better phase noise prediction than the LTI models but retain some of the nonphysical artifacts such as infinite noise power at the fundamental frequency. In particular, Hajimiri and Lee's model is capable of very good phase-noise prediction without most of the mathematical complexities [28]. The improved accuracy is achieved by taking into account the cyclostationary property of the noise sources that inherently

exists because of the switching action of the VCO. The drawback is the breakdown of its accuracy for circuit topologies involving non-stationary noise sources such as injection-locking VCOs [43].

2.1 Linear Time-Invariant Phase-Noise Model

In [32], Leeson derived heuristically an expression (Equation 2.3) for the phase noise spectral density of a feedback oscillator, where F is the circuit noise factor, k is the Boltzmann's constant, T is the temperature, P_0 is the oscillator output power, Q_L is the loaded quality factor of the resonator, ω_0 is the oscillator fundamental frequency, $\Delta\omega$ is the offset frequency, and ω_c is the flicker noise corner frequency.

$$S_\phi(\Delta\omega) = \frac{FkT}{P_0} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\omega_c}{\Delta\omega}\right) \tag{2.3}$$

Equation 2.3 can be derived more rigorously with the help of the Barkhausen criterion, a necessary condition for stable oscillation. Given the feedback circuit of Figure 2.2(a), its transfer function can be easily shown to be that of Equation 2.4. For this circuit to be autonomous during normal operation, the denominator of Equation 2.4 has to be equal to zero or equivalently $F(s) \cdot B(s) = 1$.

$$H(s) = \frac{Y(s)}{X(s)} = \frac{F(s)}{1 - F(s) \cdot B(s)} \tag{2.4}$$

For this circuit to operate as an oscillator it can be redrawn as Figure 2.2(b) without loss of generality, where the forward gain block $F(s)$ is implicitly set equal to unity, and the feedback block $B(s)$ is replaced by a transconductor $G_m(s)$ and a frequency-selective component, i.e. a parallel RLC tank. The resistance R_P represents the total loss of the

resonator while L and C represent an ideal inductor and capacitor respectively. At resonant frequency ω_0, the reactive components vanish, leaving only R_P as the impedance of the tank. Applying the Barkhausen criterion, the equality $G_m R_P = 1$ must be satisfied for sustained oscillation (assuming the transconductance $G_m(s)$ is constant near ω_0). On the other hand, the impedance of the tank at an offset frequency $\Delta\omega << \omega_0$ can be shown to be (Appendix A):

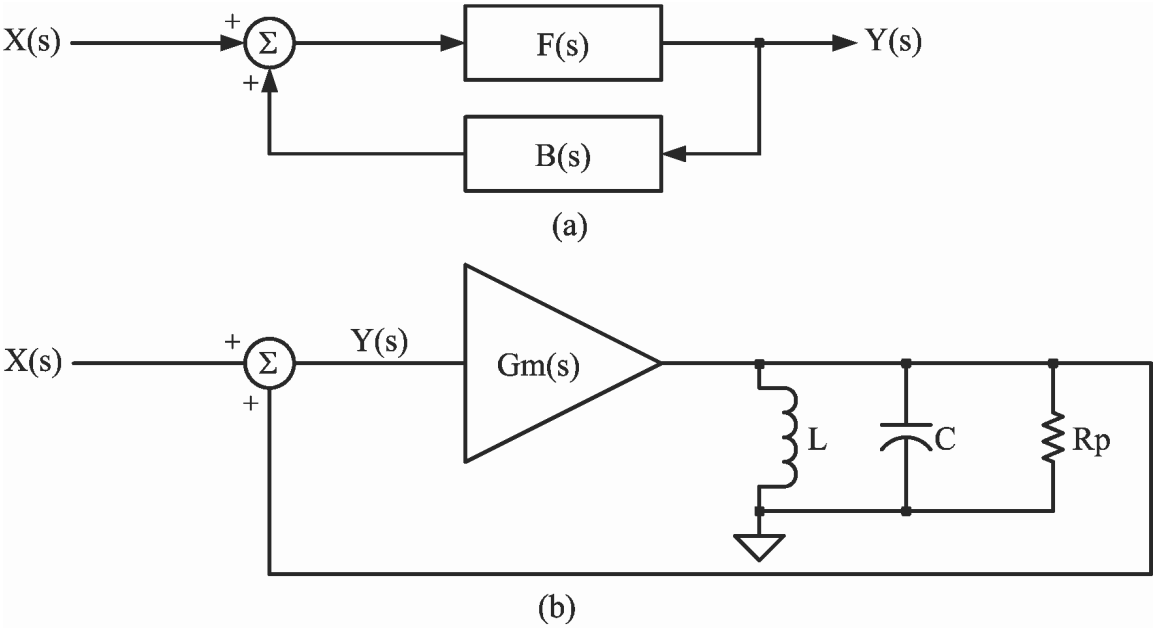

Figure 2.2 Block diagrams of (a) a positive feedback circuit (b) a positive feedback LC oscillator.

$$Z(\omega_0 + \Delta\omega) = \frac{R_P}{1 + j2Q_L \dfrac{\Delta\omega}{\omega_0}} \tag{2.5}$$

Substituting Equation 2.5 into Equation 2.4 to obtain:

$$H(j\omega) = \frac{1}{1 - \dfrac{G_m R_P}{1 + j2Q_L\,\Delta\omega/\omega_0}}$$

Using the equality $G_m R_P = 1$, and simplifying the equation:

$$H(j\omega) = \frac{1}{1 - \dfrac{1}{1 + j2Q_L\,\Delta\omega/\omega_0}} = 1 + \frac{1}{j2Q_L\,\Delta\omega/\omega_0} \tag{2.6}$$

Thus, the output phase noise can be calculated as shown below:

$$S_Y(\Delta\omega) = S_X(\Delta\omega)\cdot H(j\omega)\cdot H^*(j\omega)$$

The input-referred noise spectral density is empirically determined in the Leeson model, where the circuit noise factor F and the flicker-noise corner frequency ω_c are just fitting parameters.

$$S_X(\Delta\omega) = FkT\cdot\left(1 + \frac{\omega_c}{\Delta\omega}\right)$$

$$\Rightarrow \qquad S_Y(\Delta\omega) = FkT\cdot\left(1 + \frac{\omega_c}{\Delta\omega}\right)\cdot\left(1 + \frac{1}{j2Q_L\,\Delta\omega/\omega_0}\right)\cdot\left(1 - \frac{1}{j2Q_L\,\Delta\omega/\omega_0}\right)$$

$$S_Y(\Delta\omega) = FkT\cdot\left(1 + \frac{\omega_c}{\Delta\omega}\right)\cdot\left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \tag{2.7}$$

In summary, the advantages of the Leeson phase-noise model are its simplicity, showing an explicit relationship between the output phase noise and circuit parameters. However, it relies heavily on fitting parameters derived from measured data because it cannot account for the noise generated from nonlinear mixing processes. Thus, its usefulness in phase noise prediction is limited.

2.2 Nonlinear Time-Varying Phase-Noise Model

Perhaps the first comprehensive nonlinear phase-noise model presented is that by Demir *et al* in [39]. It is described by a system of differential equations (Equation 2.8), where $x \in R^n$ is the state variable, $f(.): R^n \to R^n$ is a description of circuit behavior, $b(.): R \to R^p$ is the noise source, and $B(.): R^n \to R^{n \times p}$ represents the noise source dependence on circuit states.

$$\dot{x} = f(x) + B(x)b(t) \tag{2.8}$$

The traditional approach to analyze perturbed nonlinear system is to linearize about the unperturbed solution, assuming that the resultant deviation will be small. Equation 2.8 is then transformed into Equation 2.9, where $w(t)$ is the deviation from the unperturbed solution $x_s(t)$, the Jacobian $A(t) = \delta f(x)/\delta x|_{x_s(t)}$ is T-periodic, and $B(x)$ is approximated by $B(x_s(t))$.

$$\dot{w}(t) \cong A(t)w(t) + B(x_s(t))b(t) \tag{2.9}$$

However, it can be shown that the solution of Equation 2.9 for oscillators may grow unbounded even for small $b(t)$, indicating that the linearized perturbation analysis is inconsistent. To resolve this problem, Demir *et al* presented a novel nonlinear perturbation analysis for oscillators. The original perturbation $B(x)b(t)$ is to be divided into two parts $b_1(x,t)$ and $\tilde{b}(x,t)$ (as defined by Equation 2.10 and 2.11) such that the solution to the equation $\dot{x} = f(x) + b_1(x,t)$ is $x_p(t) = x_s(t + \alpha(t))$, where $\alpha(t)$ is defined in Equation 2.12. The phase deviation $\alpha(t)$ can grow unboundedly large with time even though the perturbation $b_1(x,t)$ remains small. Then, $z(t) = x_s(t + \alpha(t)) + y(t)$ is the

solution to Equation 2.8, and the orbital deviation $y(t)$ can be obtained from the traditional perturbation analysis since it can be shown that $y(t)$ will remain small for all t.

$$b_1(x,t) = c_1(x,t) \cdot u_1(t + \alpha(t)) \tag{2.10}$$

$$\tilde{b}(x,t) = \sum_{i=2}^{n} c_i(x,t) \cdot u_i(t + \alpha(t)) \tag{2.11}$$

$$\frac{d\alpha(t)}{dt} = v_1^T(t + \alpha(t)) \cdot B(x_s(t + \alpha(t))) \cdot b(t) \tag{2.12}$$

where $c_i(x,t) \equiv v_i^T(t + \alpha(t)) \cdot B(x) \cdot b(t)$

and u_i, v_i are the Floquet eigenvectors as described in [39].

Assuming that the perturbation $b(t)$ is a vector of uncorrelated stationary white noise sources, Demir *et al* proved that $\alpha(t)$ becomes, asymptotically with time, a Gaussian random variable with a constant mean m, a variance that is linearly increasing with time $\sigma^2(t) = ct$, and a correlation function $E[\alpha(t)\alpha(t+\tau)] = m^2 + c \cdot \min(t, t+\tau)$.

$$c = \frac{1}{T} \int_0^T v_1^T(t) \cdot B(x_s(t)) \cdot B^T(x_s(t)) \cdot v_1(t) \cdot dt \tag{2.13}$$

Once the stochastic characterization of $\alpha(t)$ is known, the correlation function of $x_s(t + \alpha(t))$ can be calculated:

$$R(t,\tau) = E[x_s(t + \alpha(t)) \cdot x_s(t + \tau + \alpha(t+\tau))]$$

$$R(t,\tau) = \sum_{i=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} X_i X_k^* e^{j(i-k)\omega_0 t} e^{-jk\omega_0 \tau} E\left[e^{j\omega_0 \beta_{ik}(t,\tau)}\right] \tag{2.14}$$

where $\beta_{ik}(t,\tau) = i\alpha(t) - k\alpha(t+\tau)$

and X_i's are the Fourier coefficients of $x_s(t)$

It can also be shown that this autocorrelation function becomes independent of time asymptotically, i.e.

$$\lim_{t\to\infty} R(t,\tau) = \sum X_i X_i^* e^{-ji\omega_0\tau} e^{-0.5\omega_0^2 i^2 c|\tau|} \tag{2.15}$$

The power spectral density (PSD) and the single-sided spectral density of $x_s(t+\alpha(t))$ can now be computed by taking the Fourier transform of Equation 2.15:

$$S(\omega) = \sum_{i=-\infty}^{\infty} X_i X_i^* \frac{\omega_0^2 i^2 c}{\frac{1}{4}\omega_0^4 i^4 c^2 + (\omega + i\omega_0)^2} \tag{2.16}$$

$$S_{ss}(f) = 2S(2\pi f) = 2\sum_{i=-\infty}^{\infty} X_i X_i^* \frac{f_0^2 i^2 c}{\pi^2 f_0^4 i^4 c^2 + (f + if_0)^2} \tag{2.17}$$

The single-sideband phase-noise spectrum, defined as noise PSD around the first harmonic of the unperturbed solution, can then be calculated and simplified, assuming that c is small and $\Delta f << f_0$. Note that the spectrum has the Lorentzian shape at the carrier frequency (and its harmonics) which is consistent with the physical limitation that noise power must be finite.

$$L(\Delta f) = 10\log_{10}\left(\frac{S_{ss}(f_0+\Delta f)}{2\left|X_1^2\right|}\right) \cong 10\log_{10}\left(\frac{f_0^2 c}{\pi^2 f_0^4 c^2 + \Delta f^2}\right) \tag{2.18}$$

In summary, Demir *et al* has established a mathematically rigorous model for phase noise of any type of oscillators. An exact nonlinear equation for phase error was derived and solved for random noise sources. The result showed that a single scalar constant c is sufficient to characterize the noise spectral density, and experimental data were consistent with prediction by this model, even at very small offset frequencies where other models broke down. However, the model does not provide any insight into the relationship

between phase noise and circuit parameters, such that a circuit designer can utilize for phase noise optimization.

2.3 Linear Time-Varying Phase-Noise Model

The phase-noise model proposed by Hajimiri and Lee in [28] is based on the impulse sensitivity function (ISF), which is a measure of the sensitivity of the oscillator to an impulsive input. It is a dimensionless periodic (in 2π) function that is independent of the output frequency and amplitude, describing phase shift result from applying a unit impulse at any point in time. Figure 2.3 illustrates this sensitivity for an LC resonator with the impulse applied at the zero crossing and the peak of its output waveform. Note that there is also an amplitude response due to the injected current, but it decays while the phase response persists indefinitely. Moreover, in a typical oscillator, some form of mechanism to restore amplitude exists. Therefore, the amplitude perturbation can be neglected.

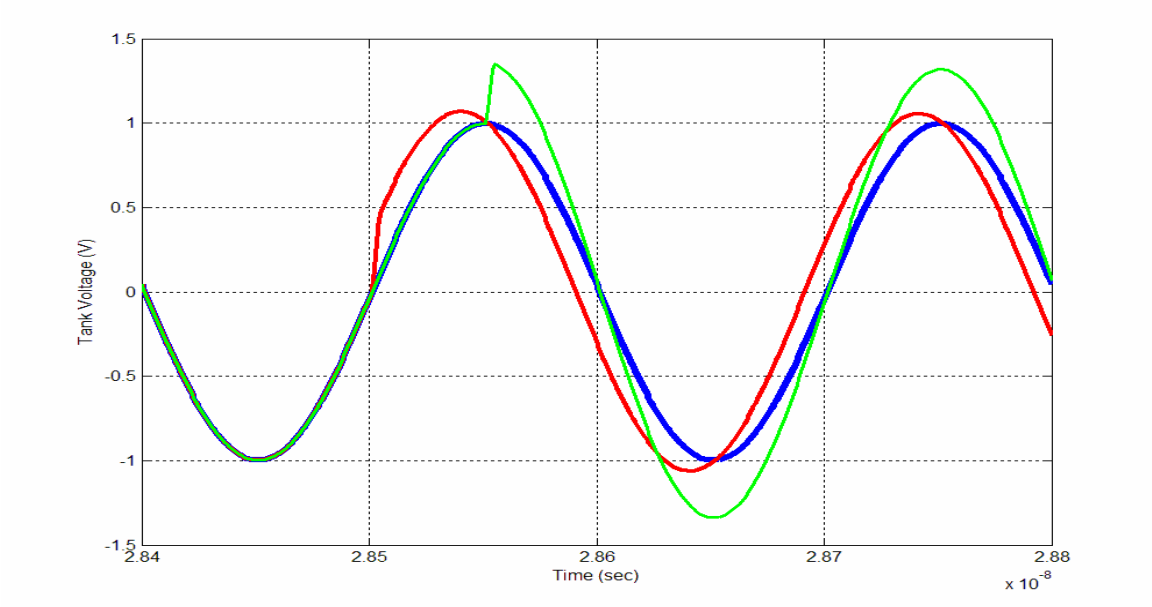

Figure 2.3 Phase shift resulting from applying current impulse to an ideal LC resonator at its peak and its zero-crossing point.

For a small injected charge Δq, the resulting phase shift $\Delta\phi$ is shown in Equation 2.19, where Γ is the ISF and $q_{\max}$ is the maximum charge swing. Since the phase shift persists indefinitely, the unity phase-impulse response can be easily obtained from (2.19) as shown in Equation 2.20. The ISF function is assumed linear for small injected charge, even though the circuit active elements may have strongly nonlinear voltage-current behavior. Therefore, the output excess phase can be calculated using the superposition integral as shown in Equation 2.21, where $i(t)$ represents the injected noise current.

$$\Delta\phi = \Gamma(\omega_0\tau)\cdot\frac{\Delta q}{q_{\max}} \qquad \Delta q << q_{\max} \tag{2.19}$$

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}}\cdot u(t-\tau) \qquad u(t)\text{: a unit step function} \tag{2.20}$$

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)\cdot i(\tau)d\tau = \int_{-\infty}^{t}\frac{\Gamma(\omega_0\tau)}{q_{\max}}\cdot i(\tau)d\tau \tag{2.21}$$

Since Γ is periodic, it can be expanded in a Fourier series as shown in Equation 2.22. Substituting (2.22) back into (2.21) and exchanging the order of summation and integration, Equation 2.23 is obtained. It describes the conversion process of an arbitrary injected noise source into excess phase in terms of the Fourier coefficients of the ISF.

$$\Gamma(\omega_0\tau) = c_0 + \sum_{n=1}^{\infty} c_n\cdot\cos(n\omega_0\tau) \tag{2.22}$$

$$\phi(t) = \frac{1}{q_{\max}}\left[c_0\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n\int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)d\tau\right] \tag{2.23}$$

To understand this process more clearly, let $i(t) = I_0\cos(\Delta\omega\cdot t)$ and compute the resulting excess phase using (2.23). Assuming $\Delta\omega << \omega_0$, all the integrals associated with $c_n, n = 1,\ldots\infty$ are much smaller than the term arising from the first integral. Therefore,

the resulting excess phase can be approximated as in Equation 2.24. Similarly, for $i(t) = I_n \cos((n\omega_0 + \Delta\omega)\cdot t), n = 1,\ldots\infty$, $\phi(t)$ is approximated by Equation 2.25.

$$\phi(t) = \frac{I_0 c_0 \sin(\Delta\omega \cdot t)}{q_{\max} \cdot \Delta\omega} + \sum_{n=1}^{\infty} \frac{I_0 c_n}{2 \cdot q_{\max}} \left[\frac{\sin((n\omega_0 + \Delta\omega)\cdot t)}{n\omega_0 + \Delta\omega} + \frac{\sin((n\omega_0 - \Delta\omega)\cdot t)}{n\omega_0 - \Delta\omega} \right]$$

$$\phi(t) \cong \frac{I_0 c_0 \sin(\Delta\omega \cdot t)}{q_{\max} \cdot \Delta\omega} \tag{2.24}$$

$$\phi(t) \cong \frac{I_n c_n \sin(\Delta\omega \cdot t)}{2 \cdot q_{\max} \cdot \Delta\omega} \tag{2.25}$$

The excess phase is then converted to a pair of equal sidebands at $\omega_0 \pm \Delta\omega$ (Equation 2.26), from which the sideband power relative to the carrier can be calculated (Equation 2.27). Figure 2.4 summarizes this noise conversion and folding process.

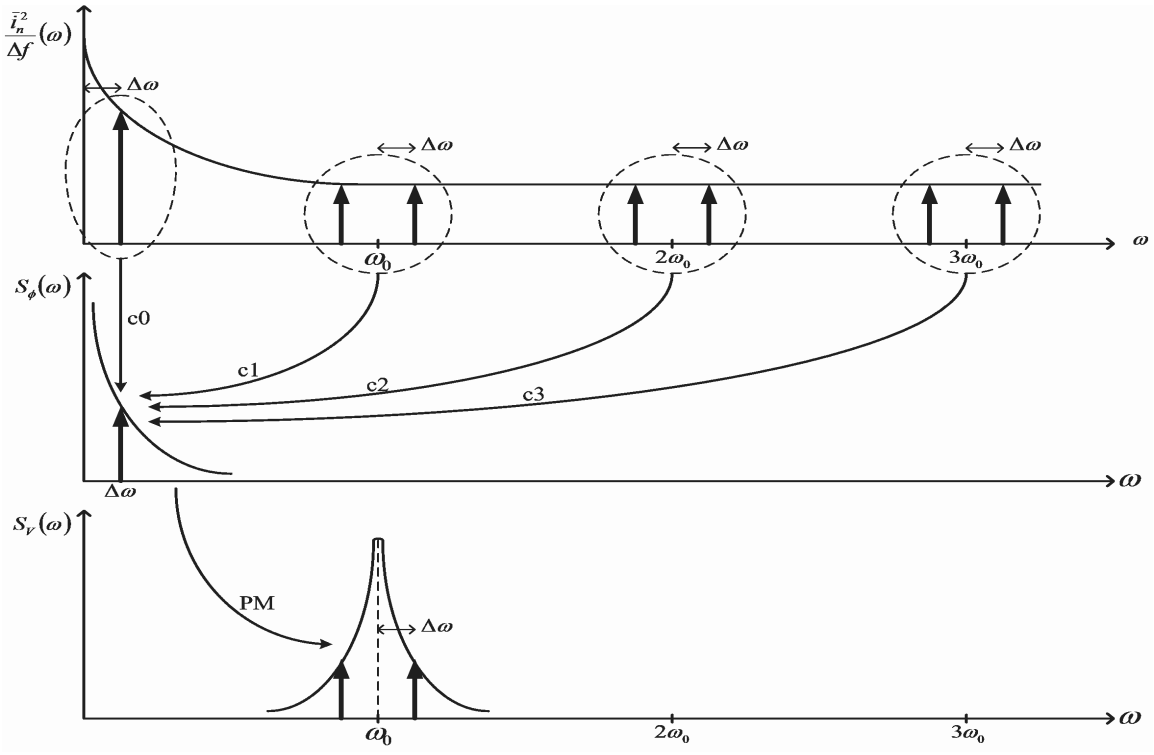

Figure 2.4 Conversion of circuit noise to excess phase (via ISF), and then to phase-noise sideband [30].

$$\cos[\omega_0 t + \phi(t)] = \cos(\omega_0 t)\cos[\phi(t)] - \sin(\omega_0 t)\sin[\phi(t)], \qquad \phi(t) << 2\pi$$

$$\cos[\omega_0 t + \phi(t)] \cong \cos(\omega_0 t) - \phi(t)\cdot\sin(\omega_0 t)$$

$$\cos[\omega_0 t + \phi(t)] \cong \cos(\omega_0 t) + \frac{I_n c_n}{4 q_{\max}\Delta\omega}\left[\cos((\omega_0 + \Delta\omega)t) - \cos((\omega_0 - \Delta\omega)t)\right] \qquad (2.26)$$

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2I_0^2 c_0^2 + \sum_{n=1}^{\infty} I_n^2 c_n^2}{8 q_{\max}^2 \Delta\omega^2}\right] \qquad (2.27)$$

Hajimiri and Lee went on in [30] to derive a closed-form expression for the single sideband phase noise in the case of multiple stochastic noise processes. However, it cannot easily be evaluated, and Equation 2.27 remains to be the most useful expression for determining the phase noise of an oscillator.

The definition of the ISF can be expanded to take into account the presence of cyclostationary noise sources such as the channel noise of a MOS transistor. Its statistical properties vary with time in a periodic manner because the noise power is modulated by the gate-source overdrive voltage. A white cyclostationary noise current $i_n(t)$ can always be decomposed as in (2.28), where $i_{no}(t)$ is a white stationary process and $\alpha(\omega_0 t)$ (called the noise modulating function) is a deterministic periodic function describing the noise amplitude modulation. The noise modulating function (NMF) is normalized to a maximal value of one and can be easily derived from the device noise characteristics and the noiseless steady-state waveform. Substituting (2.28) into (2.21) yields an expression (Equation 2.29) for the excess phase resulting from a cyclostationary noise source. It is identical to that which is caused by a stationary noise applied to a system with a new ISF

given by Equation 2.30. Hence, this new definition of the ISF should be used in the calculation of the Fourier coefficients c_n's specified in (2.27).

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t) \tag{2.28}$$

$$\phi(t) = \int_{-\infty}^{t} i_{n0}(\tau) \frac{\alpha(\omega_0 \tau) \cdot \Gamma(\omega_0 \tau)}{q_{\max}} d\tau \tag{2.29}$$

$$\Gamma_{NMF}(x) = \Gamma(x) \cdot \alpha(x) \tag{2.30}$$

In summary, the linear time-variant phase-noise model proposed by Hajimiri and Lee can accurately predict phase noise of most practical oscillators by taking into account the cyclostationary properties of the random noise sources. At the same time, it remains compatible with standard simulation tools (SPICE) and does not require rigorous mathematical computation. The introduced ISF accurately describes the contribution to phase perturbation by each individual noise source, allowing efficient optimization of phase noise performance. It also accounts for the effect of circuit topologies, thus offering a quick and objective way of comparison among different VCO circuits.

CHAPTER 3
INTEGRATED LC RESONATOR

The resonator is an integral part of a low-phase-noise oscillator or VCO circuit. It is a frequency-selective element capable of operating in resonance with an applied electrical stimulus. There is a variety of different types of resonators in addition to the well-known LC tanks. Some of the commonly used ones along with their performance characteristics are summarized in Table 3.1. For integrated circuit applications at the RF and microwave frequencies, only LC and possibly transmission line resonators are suitable. However, transmission lines generally take up much more space than planar inductors, and therefore, they are not usually implemented. Additionally, as indicated by Leeson's model (Equation 2.3), the quality factor (Q) of the resonator has a direct impact on the phase-noise performance of an oscillator. Therefore, this chapter focuses on the optimal implementation of integrated LC resonators in CMOS technologies.

Table 3.1 Types of resonators and their performance characteristics.

Resonator Type	**Frequency Range**	**Quality Factor**	**Tuning Range**	**Cost**
LC (integrated)	500 MHz – 10 GHz	3 – 10	Wide	Very low
LC (discrete)	100 MHz – 1 GHz	50 – 100	Wide	Low
Quartz crystal	1 MHz – 500 MHz	10000 – 100000	Very narrow	High
Ceramic	3 KHz – 20 MHz	500 – 5000	Very narrow	Low
Transmission line	> 100 MHz	1000 – 5000	Wide	Moderate
Surface Acoustic Wave (SAW)	100 MHz – 2 GHz	30 – 400	Narrow	High
Dielectric (DRO)	2 GHz – 30 GHz	About 12000	Narrow	Moderate

Figure 3.1 depicts a simplified equivalent schematic of an LC resonator, where L represents an ideal inductor, C represent an ideal capacitor, r_L and r_C represent the parasitic resistance of the inductor and the capacitor respectively, and R_P represents the external load applied to the resonator. In steady state, the active devices of an oscillator compensate for the losses incurred by the load and parasitic resistances, allowing the resonator to oscillate at the resonant frequency $\omega_0 = 1/\sqrt{LC}$. The inductance L can be implemented with a spiral metal trace above the silicon substrate, bond wires, or active devices. Bond-wire and active inductors can have much higher Q than spiral inductors, but bond-wire inductors have issues in yield and reliability, while active inductors generate significantly more noise than their passive counterparts do [5], [6]. Therefore, spiral inductors remain the only viable option for fully integrated low-phase-noise VCO design despite their inherently low Q. On the other hand, the capacitance C, called a varactor, typically serves as a frequency-tuning element. A varactor generally can be implemented with a p-n junction diode, an inversion-mode MOS capacitor, or an accumulation-mode MOS capacitor.

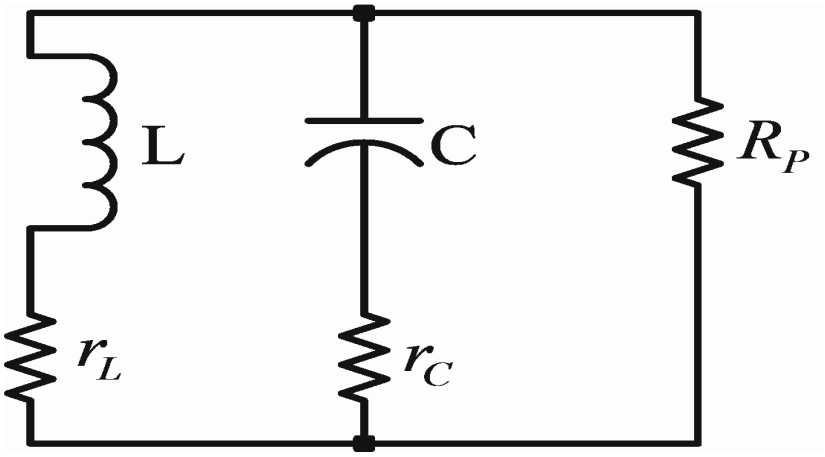

Figure 3.1 Simplified schematic of an LC resonator.

3.1 On-chip Spiral Inductors

On-chip spiral inductors are fabricated as simple geometric patterns of metal traces above the silicon substrate. Their performance characteristics are determined by their shape and dimension, and as such, they have very small variations resulting from the tight tolerance of modern photolithographic processes. The simplest and most studied pattern is the square spiral structure shown in Figure 3.2(a). However, the most efficient structure is that of a circular spiral because it allows the largest amount of conductors in the smallest possible area, thereby minimizing the series resistance of the inductor. Unfortunately, most fabrication processes do not support the circular patterns. A very good compromise is the octagonal spiral shown in Figure 3.2(b), which can have a quality factor that is only slightly smaller than that of the circular structure [44], [45].

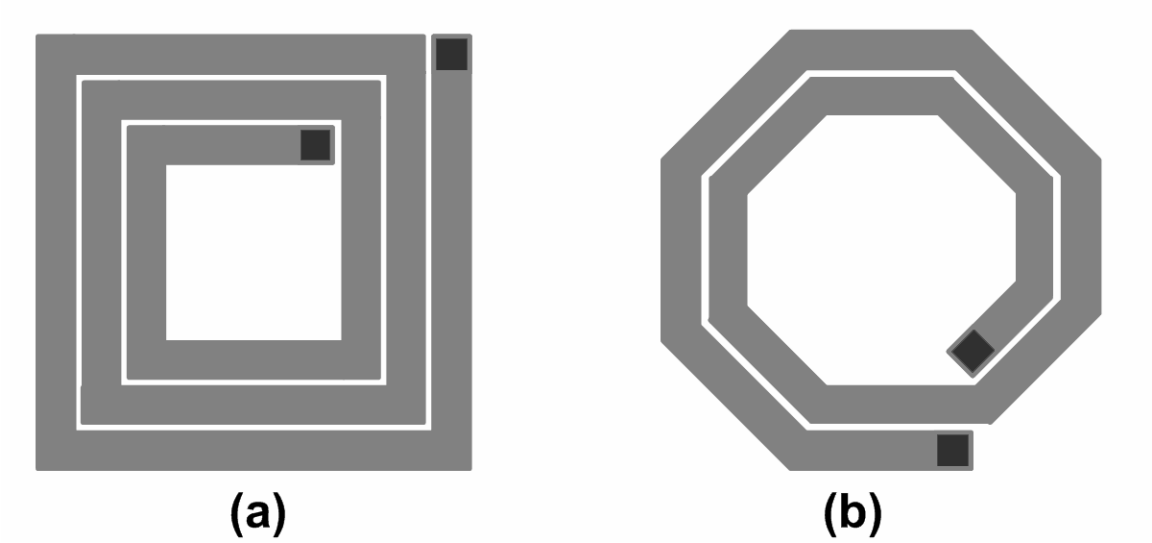

Figure 3.2 Spiral inductor structure (a) square (b) octagonal

A common drawback of these planar spirals is their relatively large size. The area, however, can be significantly reduced with a stacked spiral structure realized on multiple metal layers at the expense of resonant frequency [46], [47]. This is due to the increased metal-metal and metal-substrate capacitance. A similar multiple-metal-layer structure, called miniature 3-D inductor, was investigated, and found to have reduced area with increased resonance frequency [48]. This results from the metal-metal capacitances between turns being in series, as opposed to being in parallel for the stacked inductor.

3.1.1 Losses in Spiral Inductors

Monolithic spiral inductors, realized on CMOS processes, have notoriously low quality factor because of a multitude of energy dissipation mechanisms. The most obvious is the loss from the inductor current flowing through the series winding resistance of the inductor itself. This resistance is further increased at high frequency by the skin effect and eddy current phenomena. For frequency below 2 GHz, the skin effect (current flowing only near the surface of a conductor) is relatively small since the metal thickness is typically less than the skin depth. Above 2 GHz, the resistance grows proportionally to the square root of frequency, as a first-order approximation. Much more severe is the effect of eddy current, which results in increased resistance at a higher than linear rate. This phenomenon is well known and is illustrated in Figure 3.3. The B field of adjacent turns of the inductor penetrates a metal trace and induces eddy current loops as shown, resulting in higher net current on the inside edge (nearest to the center of the spiral) and lower net current on the outside edge. This non-uniform distribution of current constricts current flow, resulting in higher resistance [49]-[52]. The introduction of copper and thick top-level interconnects, along with the practice of shunting multiple levels of metal,

has helped improving the inductor quality factor [53]. Additionally, small inner turns of the spiral should be avoided since eddy current significantly increases their resistance while they contribute little to the total inductance value [7].

However, other energy-dissipation mechanisms, i.e. CMOS substrate losses, remain dominant and are the limiting factor of monolithic inductor performance. In a CMOS process, there exists parasitic capacitance between the spiral metal trace and the substrate. The substrate is typically made of heavily doped p-type material and is tied to ground potential for proper circuit operation. Thus, it allows RF current leakage resulting in lower inductance and self-resonance frequency. In addition, the magnetic field extends into the substrate, and according to Faraday's law, induces an image current that flows in the substrate and in the opposite direction of the inductor current. These image currents can account for 50% or more of the losses in a CMOS spiral inductor [7]. For this reason, the coil area cannot be arbitrarily large, which places an upper limit on the inductance obtainable with a planar spiral.

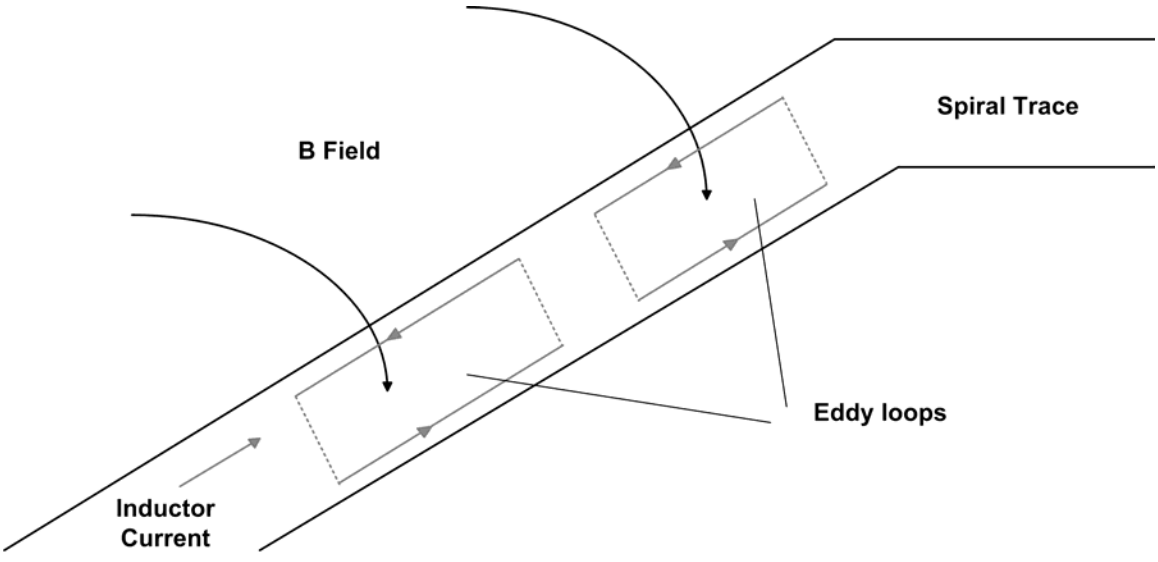

Figure 3.3 Illustration of eddy-current effect [50].

The use of a pattern ground shield (PGS) can alleviate the substrate coupling loss [54]. The shield provides a shorted path to ground to prevent the inductor electric field from reaching the substrate, thereby eliminating energy dissipation. A solid conductive ground shield between the spiral and the substrate is quite effective for this purpose. However, image current in the shield, induced by the magnetic field of the inductor, flows in a loop with opposite direction to the main current, creating a negative mutual coupling effect to reduce the net magnetic field and thus the overall inductance. Narrow slots orthogonal to the spiral, patterned into the shield as illustrated in Figure 3.4, act to disrupt the path of the induced loop current and prevent this negative mutual coupling. An important negative side effect of the PGS is the additional parasitic capacitance between the inductor and the shield, which acts to increase the capacitor loss factor severely [55]. For metal-1 PGS and polysilicon PGS, this additional energy dissipation more than offsets for the reduction of substrate loss, resulting in quality factor degradation. The n^+-diffusion PGS, on the other hand, benefits from a larger separation distance and provides a quality factor improvement of up to 21% for a 5-nH spiral inductor at a frequency of about 2 GHz [55].

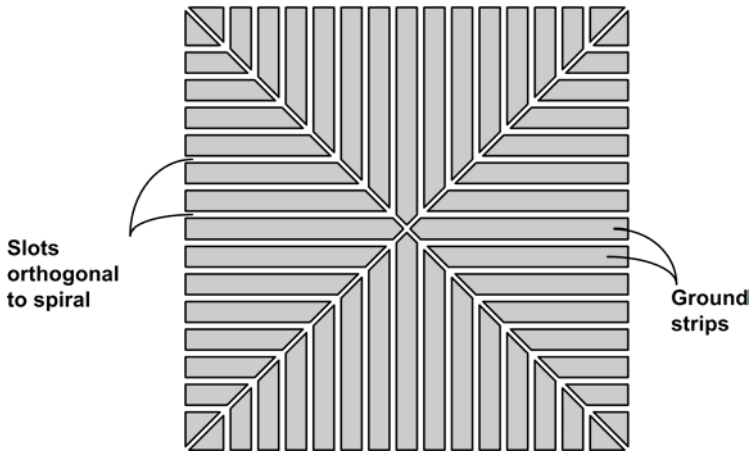

Figure 3.4 Pattern ground shield for spiral inductor.

3.1.2 Circuit Model of Spiral Inductors

Accurate modeling of an integrated spiral inductor is a difficult and challenging task because of the complexity of high-frequency phenomena such as eddy-current effect in the metal trace and substrate loss in silicon. This is evident by the many different methods reported in recent years [56]-[64]. Many are based on numerical techniques, curve fitting, or empirical formulae and therefore are relatively inaccurate and not scalable over a wide range of layout dimensions and process parameters. Thus, a physics-based analytical model is usually preferred for ease of inductor design and optimization. A general circuit, shown in Figure 3.5, can accurately model the monolithic inductor on a silicon substrate since it includes circuit elements to describe all the fore-mentioned loss mechanisms.

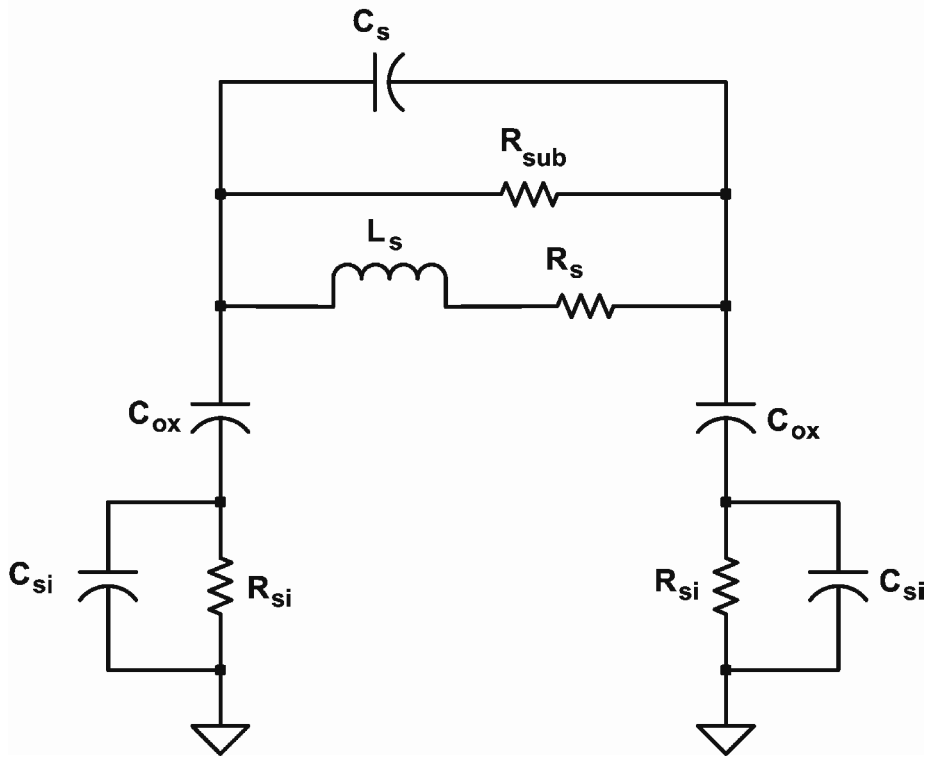

Figure 3.5 Lumped physical model of a spiral inductor.

The series inductance L_S of rectangular planar spirals can be accurately computed, using the Greenhouse method [62], [65], by summing the self-inductance of each wire segment and the positive and negative mutual inductance between all possible wire segment pairs. Thus, for an N-turn square spiral, the total inductance includes 4N self-inductance terms, 2N(N-1) positive mutual inductance terms and $2N^2$ negative mutual inductance terms. However, as the number of turns increases, the number of summation terms becomes large, making the Greenhouse method cumbersome. As an alternative, closed-form expressions for the inductance of rectangular and octagonal spirals were developed in [66] and shown to be typically within 2.3% of the measured inductance values.

The series resistance R_S models the metal wire resistance, the skin effect and eddy current effect at high frequency. It can be expressed as [62]:

$$R_S = \frac{\rho \cdot l}{w \cdot \delta \cdot \left(1 - e^{-t/\delta}\right)} \tag{3.1}$$

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \equiv \text{skin depth}$$

$\rho \equiv$ wire resistivity in Ω-m l, w, t ≡ length, width, thickness of spiral

$\mu \equiv$ permeability in H/m f ≡ frequency in Hz

The series capacitance C_S models the parasitic capacitive coupling between the input and output ports of the inductor. It includes both the crosstalk between the adjacent turns and the overlap capacitance of the crossover wire segment. However, the crosstalk capacitance is negligible since the adjacent turns are almost at the same potential.

Therefore, for most practical inductors, the series capacitance can be estimated as the sum of all overlap capacitances [62]:

$$C_S = n \cdot w^2 \cdot \frac{\varepsilon_{OX}}{t_{OX(M1-M2)}} \tag{3.2}$$

n ≡ number of overlaps w ≡ spiral line width

ε_{OX} ≡ oxide permittivity

$t_{OX(M1-M2)}$ ≡ oxide thickness between the spiral and the crossover underpass

The substrate parasitics C_{OX} represents the oxide capacitance, while C_{SI} and R_{SI} represent the silicon substrate capacitance and resistance respectively. The lateral dimensions of spiral inductors are typically much larger than the oxide thickness and are comparable to the silicon thickness. Thus, the substrate capacitance and resistance can be estimated as being proportional to the area of the inductor [62]:

$$C_{OX} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{OX}}{t_{OX}} \tag{3.3}$$

$$C_{SI} = \frac{1}{2} \cdot l \cdot w \cdot C_{substrate} \tag{3.4}$$

$$R_{SI} = \frac{2}{l \cdot w \cdot G_{substrate}} \tag{3.5}$$

$C_{substrate}$ and $R_{substrate}$ are capacitance and conductance per unit area of the silicon substrate. They are functions of the substrate doping and can be extracted from measured data.

Finally, the parallel resistance R_{SUB} models the loss resulting from the magnetic coupling with the substrate. Most modeling approaches account for this loss mechanism through a frequency-dependent value of the series resistance R_S, which makes it

impossible to distinguish between metal loss and substrate loss, a feature that can be useful in the optimization of a low-loss inductor. Currently, R_{SUB} can be determined only through parameter extraction as described in [61].

3.2 On-chip Varactors

Varactors are usually implemented with p-n junction diodes, MOS capacitors, or accumulation-mode MOS capacitors. In addition, three-terminal MOS structures are also available for applications where extra-wide tuning range is required.

3.2.1 PN-Junction Varactors

Until recently, the most widely used varactor has been the reverse biased p^+-n junction, whose capacitance is controlled by the applied reverse bias voltage. In a standard CMOS process, this is typically implemented using p^+ source/drain implants in the n-well, as shown in Figure 3.6(a). The junction capacitance is related to the controlling voltage via the simple expression:

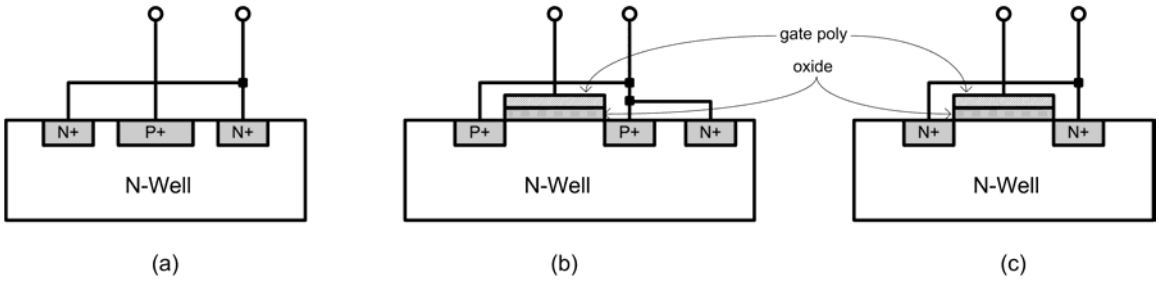

Figure 3.6 Diagram of (a) pn-junction varactor (b) PMOS varactor (c) accumulation-mode varactor

$$C_J(V_D) = \frac{C_{j0}}{\left(1 - \frac{V_D}{\Phi}\right)^{\frac{1}{\gamma}}} \tag{3.6}$$

$C_{j0} \equiv$ junction capacitance at zero bias voltage

$\Phi \equiv$ junction built-in potential

$\gamma \equiv$ doping profile constant = 2 for abrupt junction, or 3 for graded junction.

Unfortunately, the p-n junction varactor possesses many limitations. It has poor capacitance/area ratio and a low quality factor because of the relatively high parasitic series resistance [67]. It also has small tuning range (about ±10% capacitance variation) because the junction should always remain reverse biased to avoid Q degradation, which typically limits the control voltage to less than half the supply voltage. In addition, it does not scale with technology since the maximum supply voltage and the maximum diode reverse voltage are reduced, further restricting the tuning range [68].

3.2.2 MOS Varactors

The MOS varactor is normally realized as a PMOS transistor structure in an n-well with the source, drain, and bulk terminals connected together (Figure 3.6(b)). The device capacitance is then equivalent to the gate-oxide capacitance in series with the capacitance of the depletion layer created under the gate. When the gate-source voltage V_{GS} is positive, the transistor operates in the accumulation region, and its capacitance is at a maximum and is equal to the gate-oxide capacitance. As V_{GS} decreases and becomes negative, a depletion layer develops under the gate and generates a depletion capacitance. Therefore, the overall capacitance decreases until V_{GS} becomes less than the threshold

voltage V_{TP}. Then, an inversion channel builds up with mobile holes, and the device capacitance increases back up to its maximum value. Typical tuning characteristics of the MOS varactor are depicted in Figure 3.7 [69].

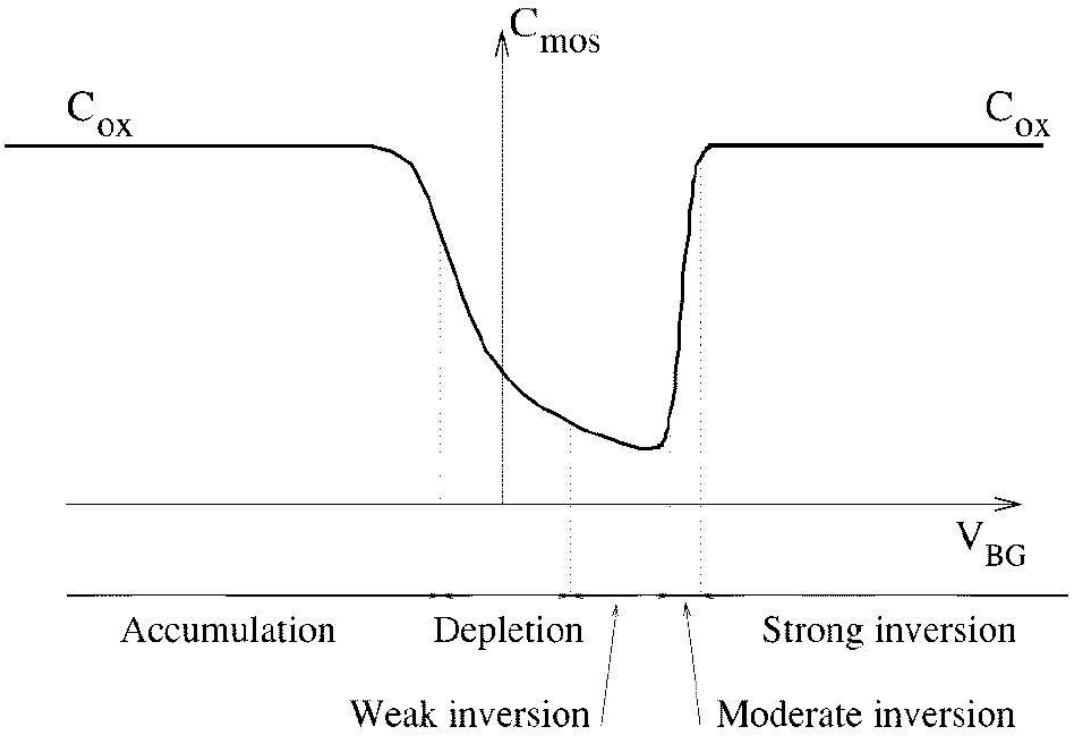

Figure 3.7 Characteristics of the PMOS varactors with B-D-S connected [69]

The non-monotonicity of the aforementioned characteristics impairs the tuning capability of the VCO circuit, thus suggesting a better alternative of using the PMOS device operating in the accumulation and depletion modes only. Replacing the p^+ source/drain implants with their n^+ counterparts, as illustrated in Figure 3.6(c), suppresses the injection of holes into the channel and prevents the transistor from entering the inversion region [68]-[70]. This type of structure, called an accumulation-mode MOS varactor (A-MOS), allows monotonic and wider-range tuning characteristics (Figure 3.8).

The maximum capacitance remains the same as the oxide capacitance C_{OX} corresponding to heavily accumulated condition, while the approximate minimum capacitance C_{DMIN} is reached when V_{GS} equals the device threshold voltage. The ratio of C_{OX} and C_{DMIN} defines the tuning range, which scales inversely with technology dimensions. In addition, the parasitic resistance, between the n^+ contacts and the edge of the depletion region, can be estimated as being inversely proportional to the transistor W/L ratio, thus also improving as technology scales down [70].

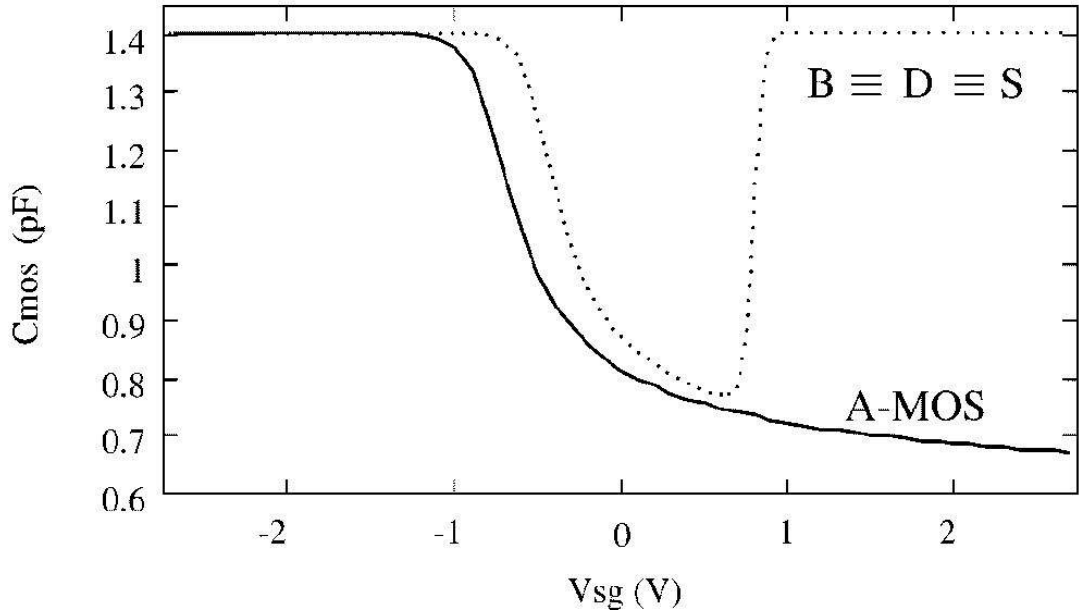

Figure 3.8 Tuning characteristics of accumulation-mode MOS varactor [69].

3.2.3 Three-Terminal MOS Varactors

The maximum thickness of the depletion layer in an A-MOS varactor is constrained by the formation of an inversion layer on the silicon surface because of the thermal generation of electron-hole pairs, thus limiting the minimum capacitance of the

device. An additional p^+ implant, acting as a third terminal, can alleviate this restriction by removing the generated minority carriers when a negative potential with respect to the source/drain/bulk terminal is applied [71]. The p^+ region is created at the head of the A-MOS structure, within the same n-well. The n^+ and p^+ diffusions are also separated by a small section of the n-well region to prevent early Zener breakdown, as illustrated in Figure 3.9. An improvement of the tuning range from 2.2:1 for the A-MOS varactor to 3.1:1 for this three-terminal device has been reported for a standard 0.35-μm CMOS process [71].

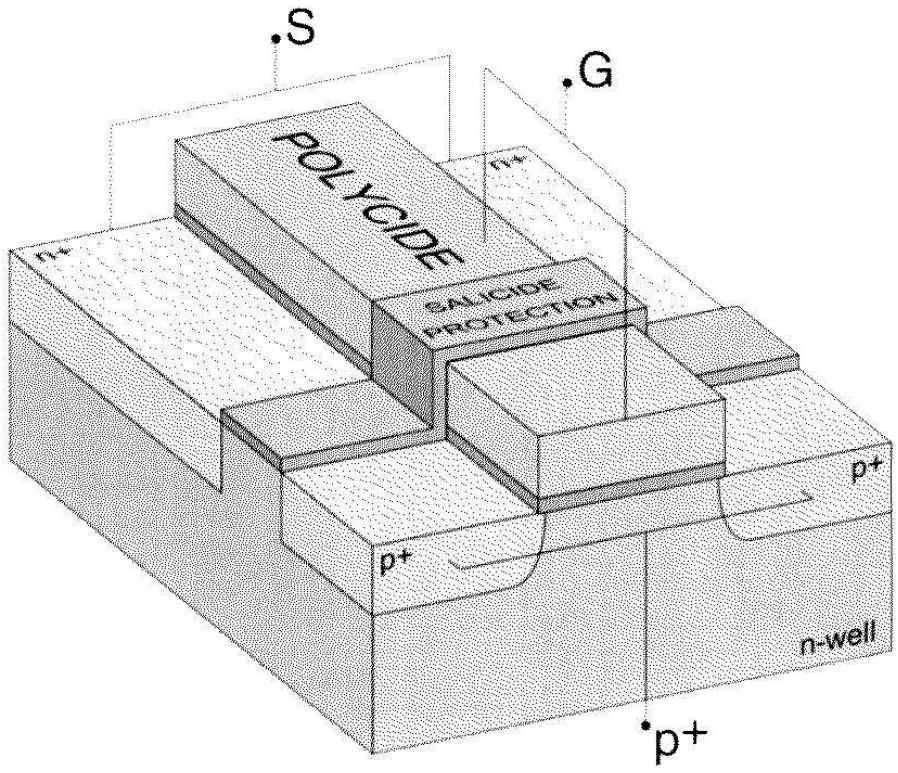

Figure 3.9 Physical structure of the three-terminal MOS varactor [71].

A similar but different three-terminal structure is shown in Figure 3.10. The capacitance looking into the drain of the device is dependent on the voltage at its gate and source. The maximum capacitance can be estimated by the sum of the oxide capacitance,

the p-n junction capacitance, and the parasitic capacitance. As the potential difference between the drain and the gate (as well as between the drain and the source) increases, the depletion region under the gate extends downward and the depletion region across the p-n junction widens, resulting in the reduction of the device capacitance. This process continues until the depletion regions merge, at which point, because of the subsurface depletion phenomena, the oxide and junction capacitances have little effect and a minimum capacitance is reached. This device reportedly has a wider tuning range (3.3:1) than the previous structure, but its quality factor is inferior because of the introduction of a large p-n junction diode [72].

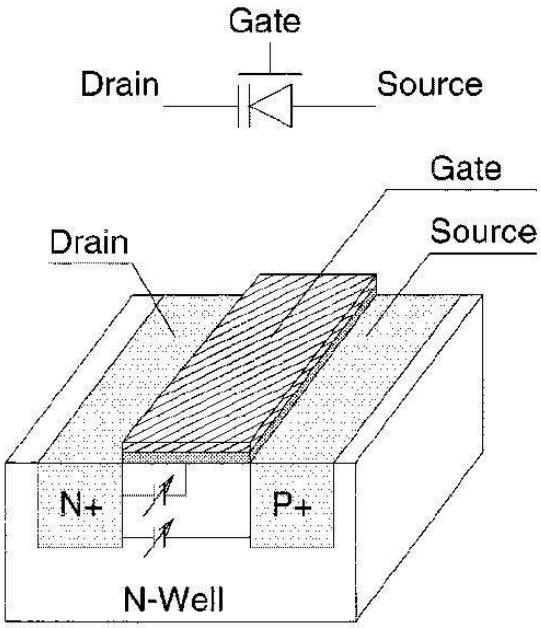

Figure 3.10 Physical structure of the gated varactor [72].

CHAPTER 4
CROSS-COUPLED TRANSCONDUCTOR CMOS VCO

Another factor that can have significant impact on VCO phase-noise performance is circuit topologies. Generally, the oscillators can be categorized as amplifiers with positive feedback satisfying the well-known Barkhausen criterion [73], or as negative-resistance circuits. An example of the positive feedback oscillators is the Pierce circuit (Figure 4.1), which is widely used in the crystal oscillator industry [74]. On the other hand, the Colpitts, Hartley, and Clapp circuits (Figure 4.2) are of the negative-resistance type. The Colpitts oscillator can potentially achieve good phase-noise performance, but requires high gain for reliable startup and is sensitive to parameter variations and common-mode noise sources resulting from single-ended operation [75]. The Hartley oscillator is analogous to the Colpitts oscillator, but is not suitable for practical implementation because of the use of two separate inductors, thereby requiring more die area. The Clapp oscillator is a variation of the Colpitts oscillator with better phase noise performance at the expense of higher power consumption. However, more recently the cross-coupled transconductor circuit of Figure 4.3(a) (and its variations) has become increasingly popular, particularly for low-power applications. This can be attributed to its inherent differential operation, ease of design, and efficient use of bias current.

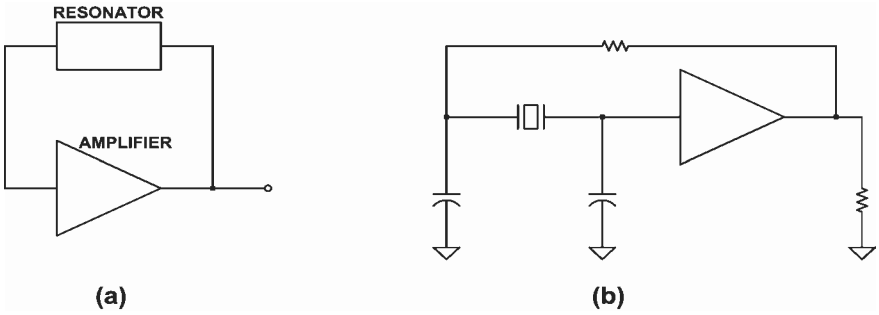

Figure 4.1 The positive feedback oscillator (a) Block diagram (b) Pierce crystal oscillator

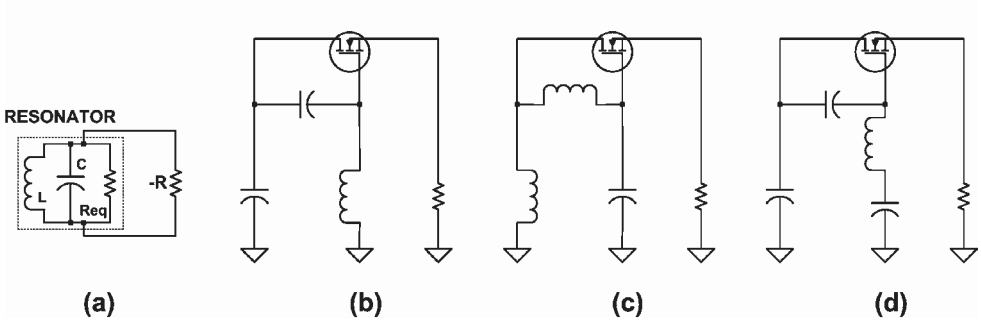

Figure 4.2 Negative resistance oscillator (a) Block diagram (b) Colpitts (c) Hartley (d) Clapp

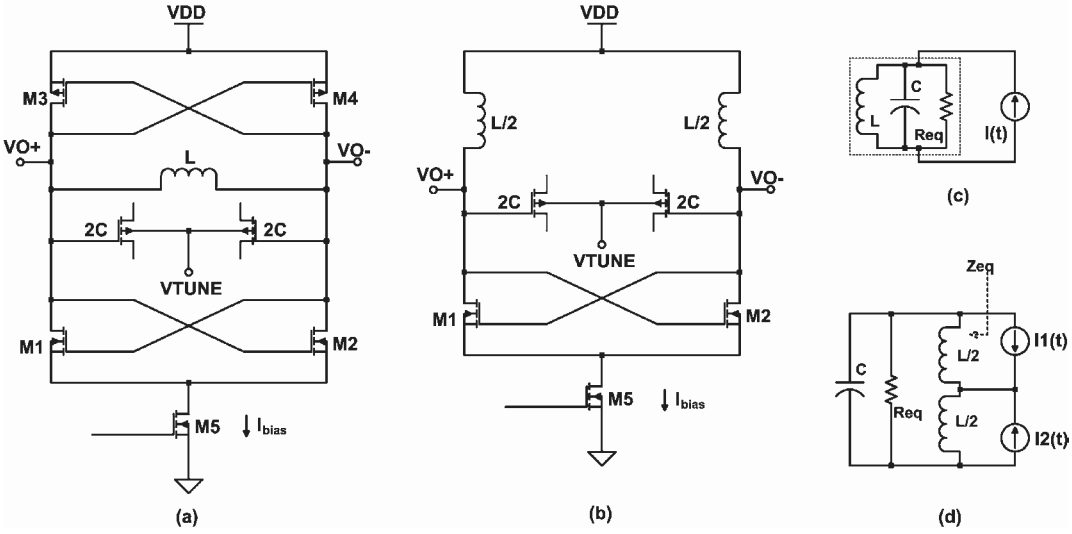

Figure 4.3 Cross-Coupled-Transconductor VCO (a) Complimentary, (b) NMOS-only (c) Equivalent circuit of (a), (d) Equivalent circuit of (b).

4.1 Circuit Analysis

For the complementary cross-coupled transconductor LC VCO of Figure 4.3(a), the impedance of the inductor and capacitor cancel each other out at the resonant frequency, leaving the bias current to flow through the parallel parasitic resistance R_{eq} of the resonator, as is easily seen in the equivalent circuit of Figure 4.3(c). If the transconductors are approximated as ideal switches, the output signal swing is then

$$V_{m(complimentary)} \approx \frac{4}{\pi} I_{bias} R_{eq} \tag{4.1}$$

For the NMOS-only (or PMOS-only) cross-coupled-transconductor VCO of Figure 4.3(b), the switching action of the transistors can be approximated as a linear superposition of two current sources, as shown in Figure 4.3(d). The output signal swing is derived as follows [10]:

$$V_{m(NMOS-only)} = 2 \cdot I1(t) \cdot Z_{eq} \cdot \frac{R_{eq} // (1/j\omega C)}{[R_{eq} // (1/j\omega C)] + j\omega L/2} \tag{4.2}$$

$$Z_{eq} = \frac{j\omega L}{2} // \left(\frac{j\omega L}{2} + \left(R_{eq} // \frac{1}{j\omega C} \right) \right)$$

Simplifying (4.2), and using the identity $\omega^2 = 1/LC$ to get

$$V_{m(NMOS-only)} = I1(t) \cdot R_{eq} \approx \frac{2}{\pi} \cdot I_{bias} \cdot R_{eq} \tag{4.3}$$

Examination of Equations 4.1 and 4.3 shows that for the same bias current, the output voltage of the complementary VCO is approximately twice that of the NMOS-only circuit. Therefore, despite of having fewer active devices the latter generally has poorer phase noise performance than its complementary counterpart. Additionally, the quality factor of the monolithic inductor excited differentially has been shown to be 50% higher

than that of the same device driven single-ended [76], further enhancing the phase noise advantage of the complementary topology.

For a given supply voltage V_{DD}, the approximate optimal output voltage swing is $V_{DD} - V_{DSsat}$ where V_{DSsat} is the saturation voltage of the bias transistor. The required bias current is then determined as follows (the $4/\pi$ scale factor is ignored for high frequencies because the current waveform is more sinusoidal than rectangular resulting from finite switching time and limited gain):

$$V_{m(complimentary)} \approx I_{bias} R_{eq} \approx V_{DD} - V_{DSsat}$$

$$I_{bias} \approx \frac{V_{DD} - V_{DSsat}}{R_{eq}} \tag{4.5}$$

The selected bias current must not be too large to cause the oscillator to enter the voltage-limited regime. In this mode of operation, excess bias current results in power being wasted without the benefit of increased output voltage swing. Additionally, the noise of active devices is increased from higher channel conduction current. To sustain oscillation in steady state, the total negative resistance generated by the transconductors M1-M2 and M3-M4 must be equal to the parasitic parallel resistance of the LC resonator R_{eq}. However, for reliable startup, it is typically chosen to be about three times R_{eq} for the required DC bias current I_{bias} (Equation 4.5). The size of the NMOS and PMOS transistors are then selected to achieve symmetrical output waveform (equal rise and fall time), or equivalently, the negative resistance of the NMOS transconductor (Appendix B) is equal to that of the of the PMOS counterpart (Equation 4.6).

$$\left(\frac{2}{g_{mNMOS}} + \frac{2}{g_{mPMOS}} \right) = 3 \cdot R_{eq} \tag{4.5}$$

$$g_{mNMOS} = g_{mPMOS} = \frac{4}{3R_{eq}} = \sqrt{\frac{K'_{NMOS} W_{NMOS} I_{bias}}{L_{NMOS}}} = \sqrt{\frac{K'_{PMOS} W_{PMOS} I_{bias}}{L_{PMOS}}} \tag{4.6}$$

4.2 Phase Noise Analysis

Figure 4.4 depicts all the noise sources in the complementary cross-coupled transconductor VCO. The noise of the effective series resistance of the inductor may be neglected for high-Q resonator. However, for lower-Q system and low-noise circuit topologies, it must be taken into account. Its noise density is $\overline{i_{nrs}^2}/\Delta f = 4kT/r_s$, or it can be expressed as a noise current in parallel with the resonator by finding the Norton equivalent as follows:

$$\frac{\overline{i_{nRp}^2}}{\Delta f} = \frac{4kT}{r_s} \cdot \left| \frac{r_s}{r_s + j\omega L} \right|^2 = \frac{4kT}{r_s} \cdot \frac{r_s^2}{r_s^2 + \omega^2 L^2} \tag{4.7}$$

Assuming that proper symmetrical layout of the inductor and trace wiring is taken; the DC and harmonic components of the ISF corresponding to this noise source should be relatively small with respect to the fundamental. Therefore, phase perturbation is caused only by the thermal noise near the resonant frequency where $r_s << \omega L$, and (4.7) can be approximated as follows:

$$\frac{\overline{i_{nRp}^2}}{\Delta f} \approx \frac{4kT}{r_s} \cdot \frac{r_s^2}{\omega^2 L^2} \approx \frac{4kT}{R_P} \tag{4.8}$$

where $R_P = \dfrac{\omega_0^2 L^2}{r_s}$

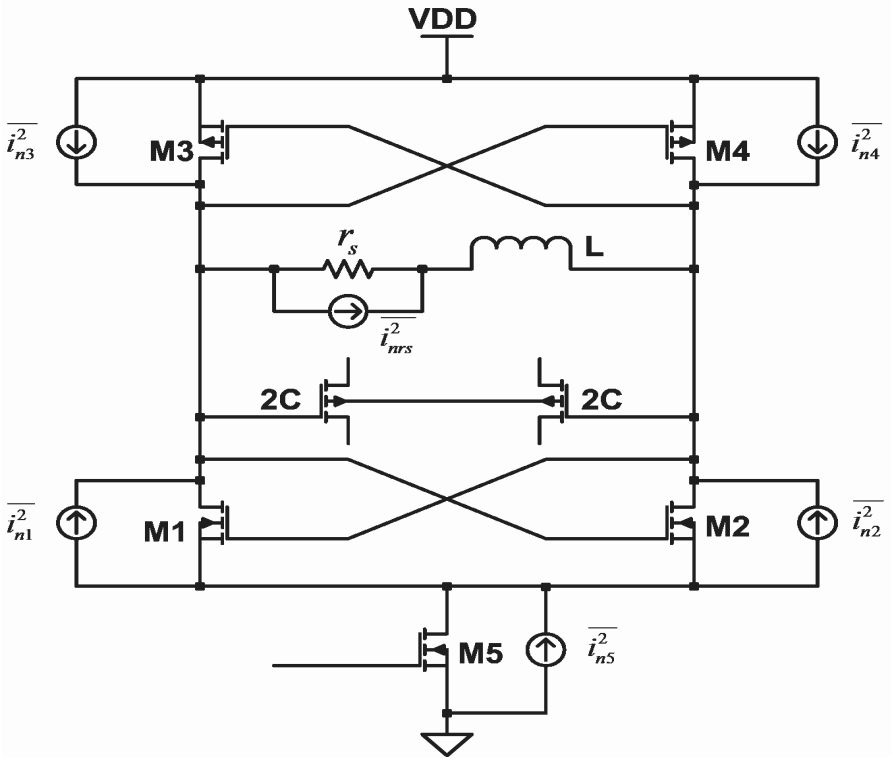

Figure 4.4 Noise sources in the complementary cross-coupled-transconductor VCO

Figure 4.5 shows the simulated ISF of the remaining noise sources. As shown for the NMOS and PMOS switching transistors, the DC component of the ISF (corresponding to the upconversion of flicker noise into close-in phase noise) can be minimized by properly sizing these devices to achieve single-ended symmetry (i.e. equal rise and fall times). Additionally, the flicker noise density of these transistors is reduced by the switching action of the oscillator [24]. Therefore, it is expected that only the thermal noise of these sources contribute to the phase noise of the VCO. The thermal noise density is described in Equation 4.9, where μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor respectively, V_{GS} is the DC gate-source voltage, V_T is the threshold voltage, and γ is a

scale factor that is about 2/3 for long-channel devices and between 2 and 3 for short-channel transistors.

$$\overline{i_n^2}/\Delta f = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS}-V_T) \tag{4.9}$$

However, as illustrated in Figure 4.6 and 4.7 for the PMOS switching transistor, the periodic drain current modulates the noise density of the device. It effectively behaves as an unmodulated noise source with a new ISF that is a cascade of the original ISF and the normalized periodic drain current. The energy of the original waveform, which is concentrated at the fundamental frequency, is spread out to higher harmonics and the DC component of the new ISF. Because of this cyclostationary property, the flicker noise of the (NMOS/PMOS) switching transistors may have a strong impact on the phase noise of the oscillator. Nevertheless, this effect can be lessened by operating the VCO well within the voltage-limited regime but with the undesirable reduction of output voltage swing.

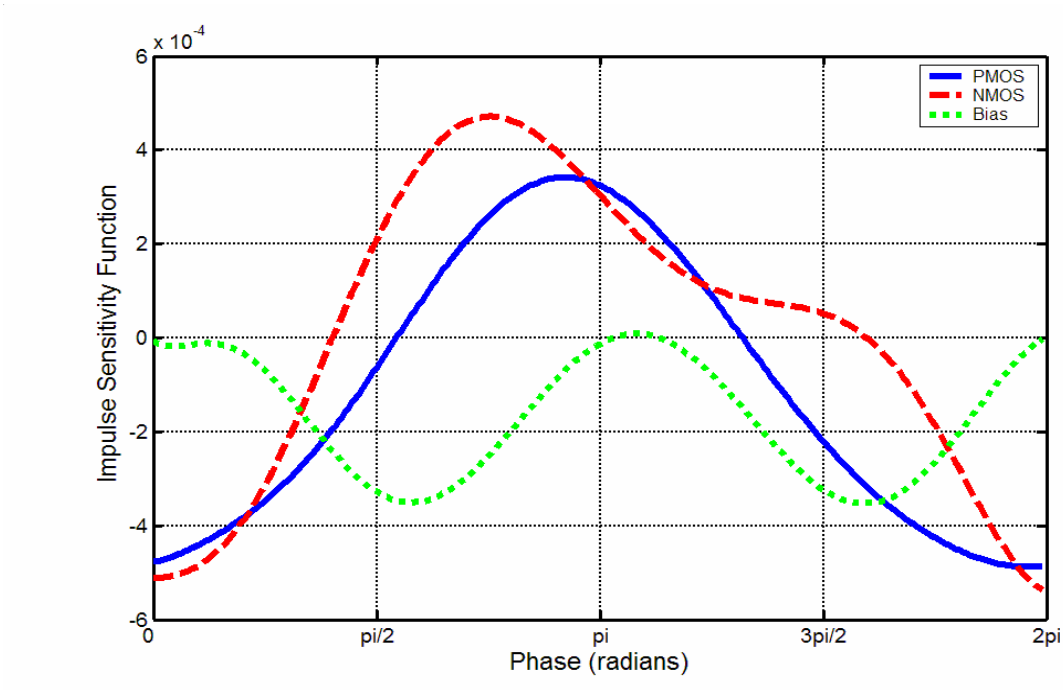

Figure 4.5 The impulse sensitivity functions of various noise sources.

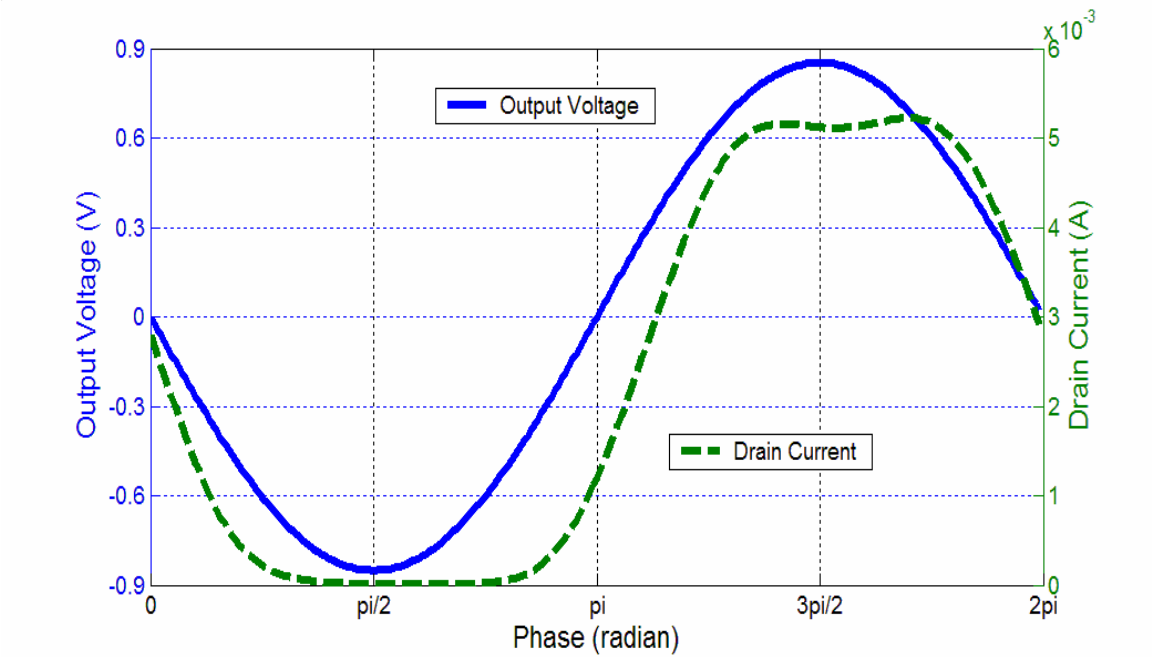

Figure 4.6 Drain current of switching PMOS transistor for a period of output signal

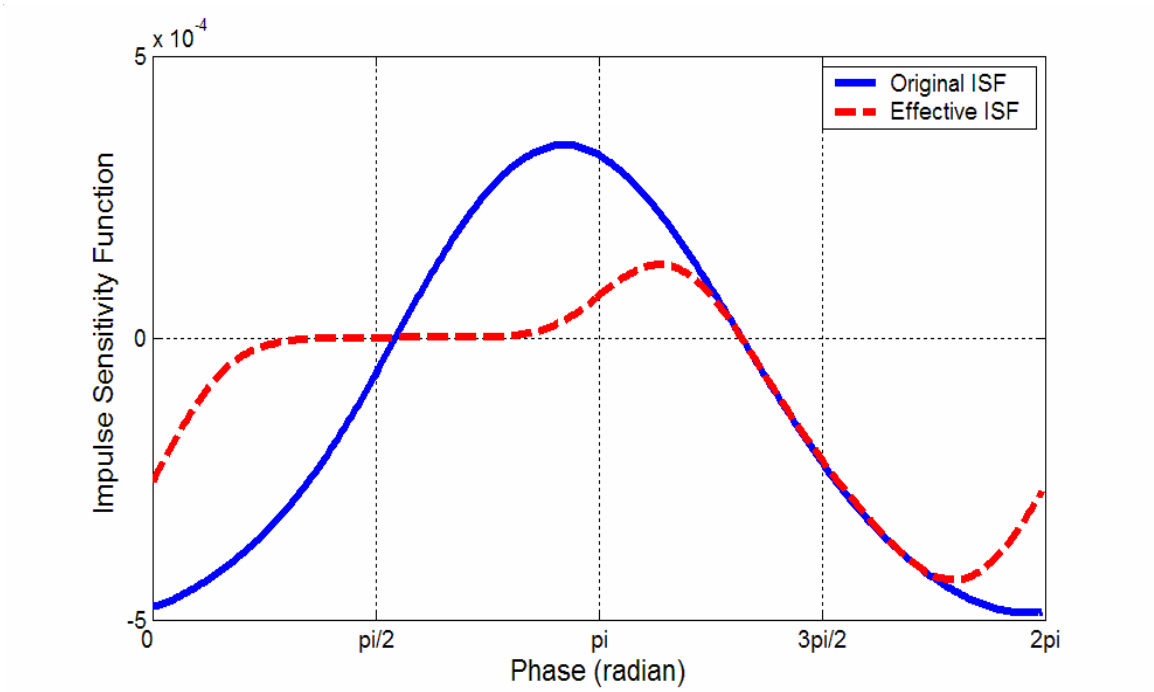

Figure 4.7 Comparison between the original ISF and the effective ISF for the PMOS switching transistor noise source.

Finally, as can be seen from Figure 4.5, the ISF corresponding to the bias transistor has a large component at twice the resonant frequency and at DC. The DC component results from the inherent asymmetry created by the presence of the bias transistor itself, and the $2\omega_0$ component is caused by the switching action of each of the two differential NMOS devices. Therefore, its flicker noise and thermal noise near $2\omega_0$ have significant effect on the phase noise. The spectral density for this noise source must include not only that of the bias transistor but also the noise contributed by the circuitry driving it. Typically, the driver is part of a current mirror, and in this case, if there is a current gain (to minimize power consumption), the noise of the driving transistor is amplified and severely degrades the phase noise of the VCO. For these reasons, the bias transistor and its driving circuitry generally are the dominant noise sources, and receive considerable attention in the literature for ways to minimize their effect on the phase noise.

4.3 Phase Noise Reduction Techniques

Increasing the quality factor (Q) of the LC resonator is the most obvious and logical approach for phase noise reduction because of its quadratic effect on the phase noise performance (Leeson's formula). However, for a fully-integrated conventional CMOS process, the possible enhancement of this parameter (Q) is limited by strong parasitic effects. The second approach for phase noise reduction is to attenuate the strength of the noise sources. Figure 4.8 shows a brute-force method of filtering the noise of the bias transistor (the dominant noise source) [22]. To attenuate the low-frequency noise, a large external inductor L_{lf} (10-100 μH) or capacitor C_{lf} (10-100 nF) can be used. The inductor

works by degenerating M_{src}, thus reducing the noise current by a factor of $\left|1 + jg_m \omega L_{lf}\right|^2$ where g_m is the transconductance of M_{src}. The frequency band of attenuation is limited on the low end by the inductance value and on the high side by the parasitic parallel capacitance of the inductor. On the other hand, the capacitor suppresses noise by shunting it to ground. The choice of filtering by capacitor is motivated by the fact that it is less bulky, more ideal, and cheaper than the inductor. However, it is less robust than inductive degeneration because it creates a low-impedance path from the common-source node to ground, which allows excessive current and noise in the switching transistors. To alleviate this problem, an on-chip inductor L_{flt} and capacitor C_{flt} are added to resonate (with other capacitance at this node) at about $2\omega_0$ so that high-impedance level is restored at this important harmonic frequency. Table 4.1 reports the measured improvement of phase noise performance for a 1.8-GHz VCO with noise filtering fabricated in a 0.35-μm standard CMOS process. As can be seen, the phase noise reduction is substantial, especially for inductive degeneration. However, the drawbacks of this method are also significant. The use of external components is highly undesirable, and the attenuation of very-low-frequency noise (<10 KHz) is difficult to achieve because very large inductance or capacitance would be required.

Table 4.1 Measured phase noise data (in dBc/Hz) [22].

Offset Frequency	$L_{lf} = 0, C_{lf} = 0$	$L_{lf} = 0, C_{lf} = 30nF$	$L_{lf} = 100\mu H, C_{lf} = 0$
100 KHz	-95.5	-98	-105.5
600 KHz	-116	-120	-123.5
3 MHz	-131.5	-136.5	-138.5

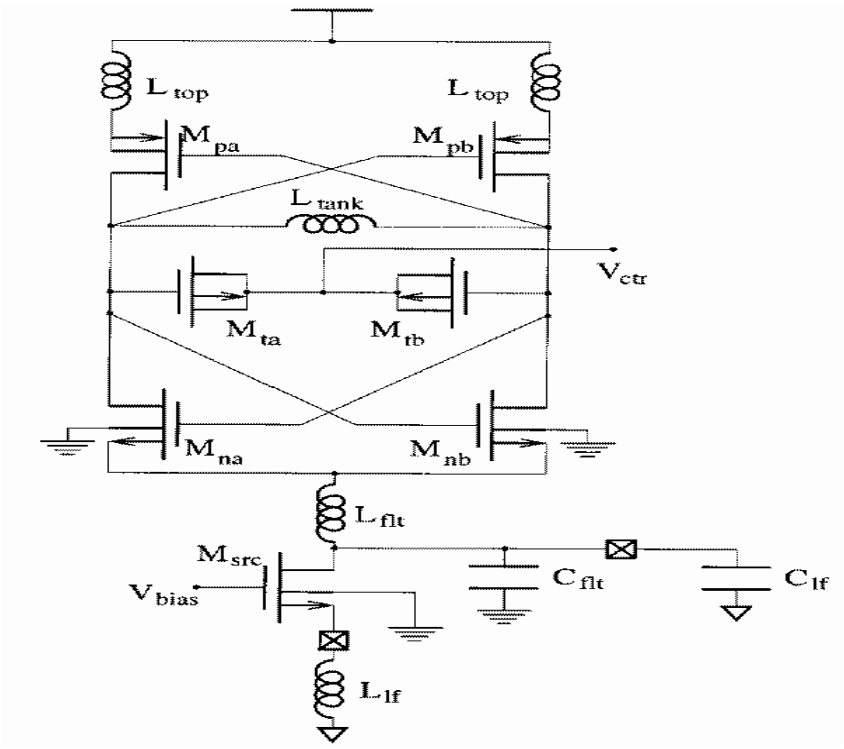

Figure 4.8 VCO schematic with noise filtering of bias transistor [22].

A more elegant method of flicker-noise attenuation is proposed in [23], where a novel switched-biasing scheme depicted in Figure 4.9 is introduced. Initially, when the circuit is balanced, both the output voltage and current flowing in the two sides are determined by the size of the tail transistors. As the circuit oscillates, each of the tail transistors alternately acts as the bias transistor while the other is turned off. Since all the active devices in this topology are switched on and off periodically, it is expected that the flicker noise will be reduced [24]. Flicker noise is widely accepted as the result of charge trapping-detrapping process from the semiconductor surface to traps located within the oxide layer. Each trap exhibits a random stochastic process with a Lorentzian spectrum and a long time self-correlation. The superposition of a cluster of such traps adds up to 1/f noise. The 1/f characteristic is associated with the long occupation time constants of the

traps. By switching the MOSFET between two states characterized by a significant difference in the Fermi levels at the interface, the occupancy of each trap becomes partially correlated with the switching action, thus disrupting the long time memory of the trapped charge. Experimental data have shown that flicker noise spectral density is reduced by about 6 to 10 dB when the transistor is switched (switching frequency is not critical) [24]-[26]. In [23], a 1.88-GHz VCO circuit, as depicted in Figure 4.9, is implemented in the 0.25-μm IBM SiGe 6 HP process. Disappointingly, when compared to a conventional VCO design in the same technology, the phase noise of this circuit is reduced by only about 1.6 dB at an offset frequency of 600 KHz. This lackluster performance gain, despite large reduction of flicker noise, can be attributed to the bias current not being constant during the oscillation cycle, thus allowing a stronger upconversion mechanism of circuit noise into phase noise.

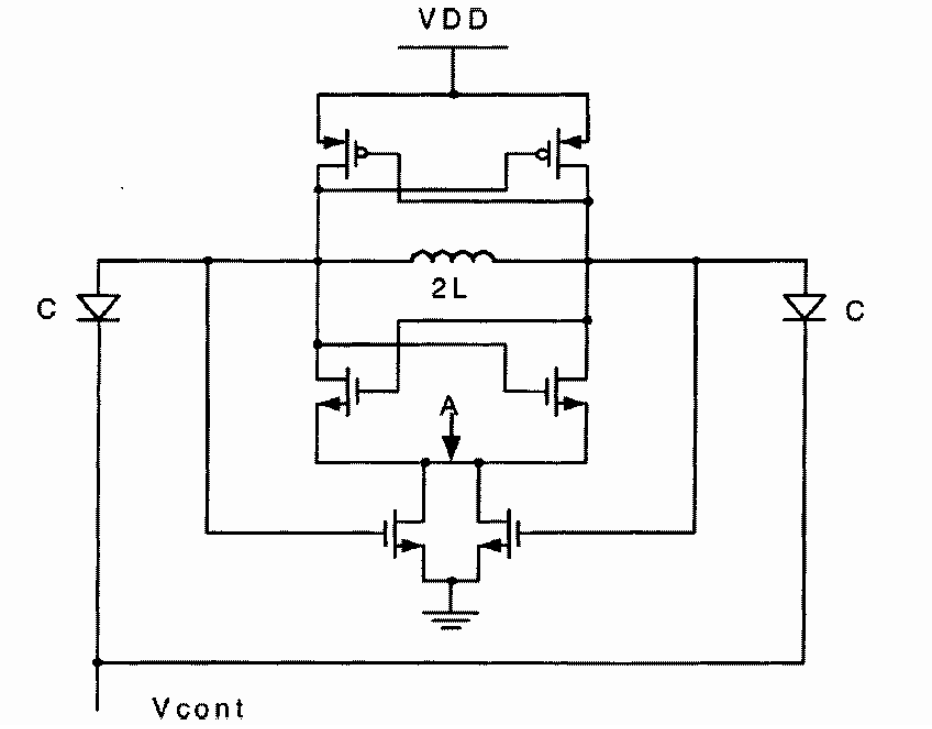

Figure 4.9 Memory-reduced tail transistor VCO [23].

A third way to reduce the flicker noise in a VCO circuit is to use the lateral bipolar junction transistor (BJT) in place of the MOS bias transistor [77]. Lateral BJT is readily available in standard CMOS process, with high current gain and low 1/f noise characteristics [78]. The cross-sectional view of a p-channel device in an n-well process is shown in Figure 4.10, where two parasitic BJT's can be seen. One is the vertical pnp between the drain/source diffusions and the substrate. The substrate must be connected to a fixed potential (typically ground), thereby restricting the use of this BJT to common-collector configurations. The other is the lateral pnp in parallel with the PMOSFET in the n-well. Since all the terminals of this BJT are accessible, it can be used in a wide variety of design applications. When the gate is biased at a high potential (greater than or equal to the supply voltage), the PMOSFET is turned off, and the parasitic BJT's become active when appropriate bias voltages are applied. For the lateral device, the emitter current is split into the base current and the lateral and vertical collector currents. Therefore, the common base current gain is not close to one. However, due to the very small rate of recombination in the lightly doped base region and the high emitter efficiency, the common-collector current gain can be large. The high potential at the gate pushes the carriers to a region below the surface so that the collect-emitter current takes place only in a buried channel separated from the oxide layer. Therefore, the charge trapping-detrapping mechanism in the oxide layer is inhibited, and the flicker noise is significantly reduced. The performance of the lateral BJT depends strongly on its layout. The emitter area and the base width should be minimized, and the collector should surround the emitter (Figure 4.11). In this way, the lateral current in all directions is diverted to the emitter, and all the contact resistances are minimized. Table 4.2 summarizes the performance of a BJT-biased VCO.

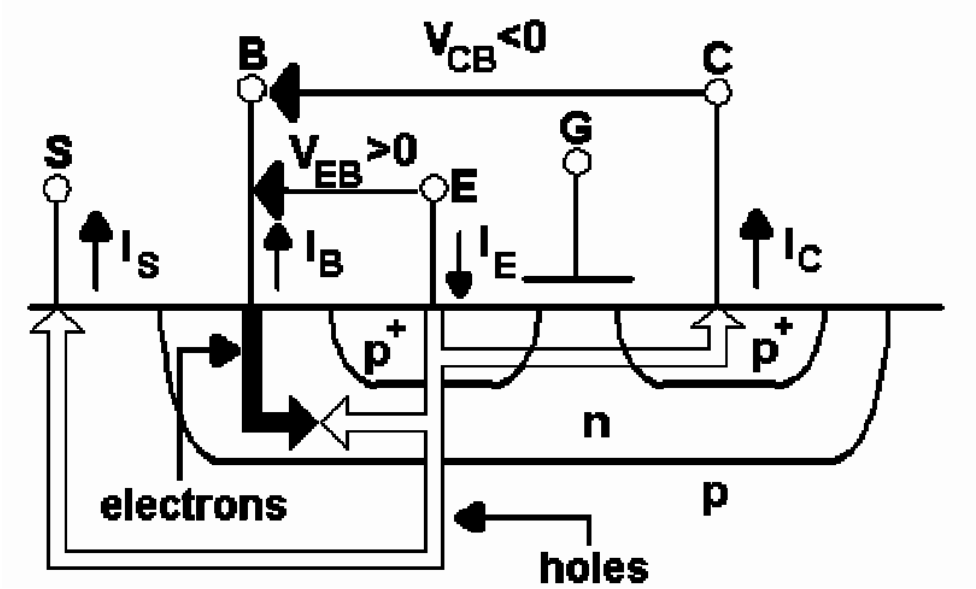

Figure 4.10 Cross-sectional view of a lateral BJT in an n-well CMOS process [77].

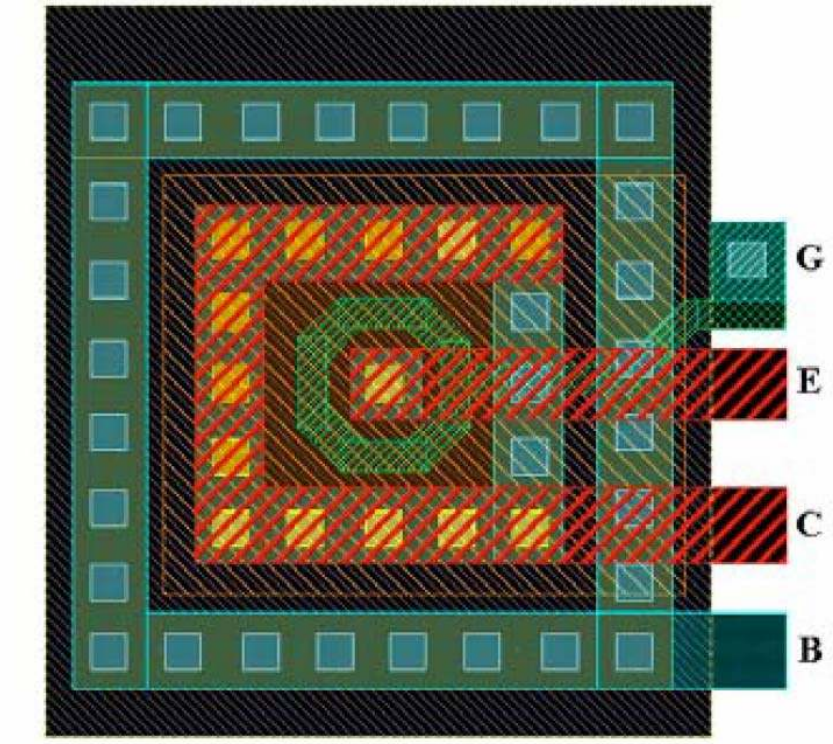

Figure 4.11 Layout of lateral PNP bipolar junction transistor [77].

Table 4.2 BJT-biased VCO Performance Summary [77].

VCO Parameters	Simulated	Measured
f_0	5.5 GHz	3.95 GHz
Tuning range	1 GHz (18%)	130 MHz (4%)
PN@100 KHz offset (PMOS)	-86 dBc/Hz	-106 dBc/Hz
PN@100 KHz offset (BJT)	-93 dBc/Hz	-
Output swing	1.4 V	0.85 V
VDD	2.5 V	3.2 V
Power dissipation	10 mW	13 mW

A similar approach is taken in [27], where the MOSFET bias transistor is replaced by a resistor network as shown in Figure 4.12, thereby eliminating a significant source of flicker noise. The bias current is then regulated by selectively shorting elements of the network with digital control bits derived from a replica servo loop. Two large inductors (23 nH) are added to increase the impedance from the source of the switching transistors to ground to minimize the degradation of the Q of the resonator. A large capacitor (75pF) is used to shunt the resistor thermal noise. In addition, a decoupling capacitor (1.3 pF) is used to track the flicker noise of the switching transistors, counteracting the fluctuating offset voltage that unbalances the differential pair. The value of this capacitor must be carefully chosen. If it is too large, the second harmonic dominates the fundamental and the circuit behaves as the differential pair. If it is too small, the oscillator does not start up. Measured data show that the phase noise of this VCO is lower than that of a conventional design by 15 dB at 50 KHz offset frequency.

In summary, the complementary cross-coupled transconductance LC VCO has proven to be ubiquitous for oscillator design, especially in CMOS technology. Despite low quality factor of on-chip passive components, its phase noise performance can be significantly improved by circuit enhancement techniques.

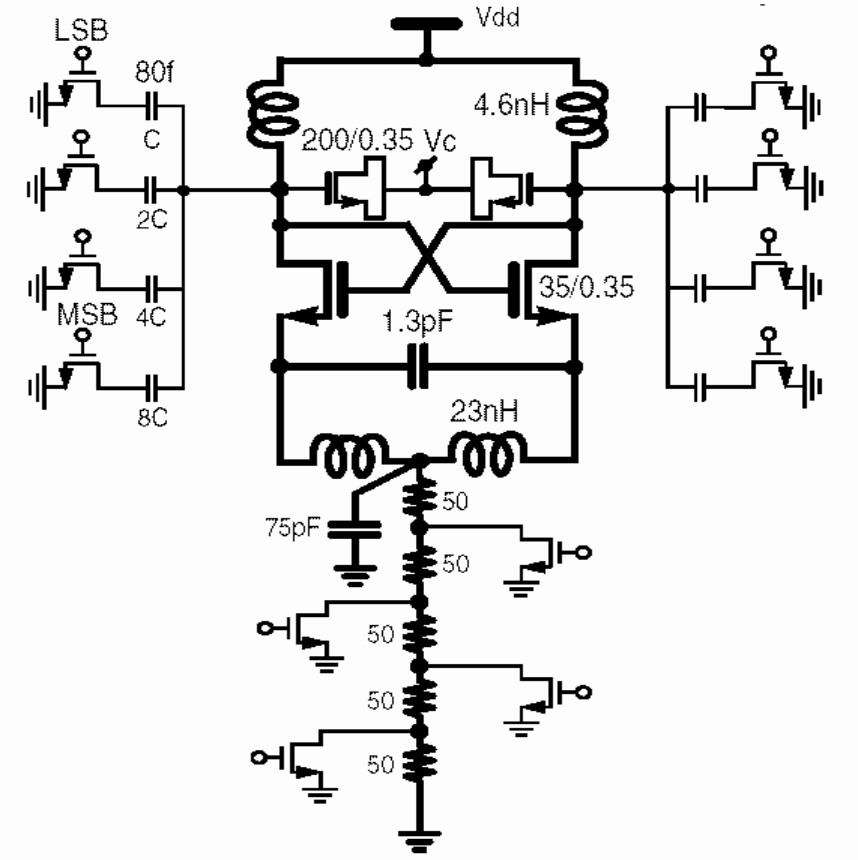

Figure 4.12 Circuit schematic of VCO with resistive bias circuit [27].

CHAPTER 5
A NEW LOW-PHASE-NOISE CMOS LC VCO

As demonstrated in the previous chapter, circuit topology can greatly affect the phase noise performance of an oscillator. In this chapter, a new low-phase-noise CMOS LC VCO is presented. Unlike some of the other approaches that attempt to reduce phase noise by attenuating the flicker noise sources, this new topology seeks to cancel the effect of low-frequency noise altogether by tuning the appropriate circuit parameters such that the ISF corresponding to a particular noise source does not contain any DC component. Therefore, the upconversion of flicker noise into phase noise is inhibited. The new circuit also reduces the strength of the noise sources by operating the switching transistors in the active/subthreshold region, where the noise spectral density is less than that of the devices operating in the saturation region. Additionally, the effect of thermal noise on the phase noise is minimized, i.e. the magnitude of the ISF waveform is minimized by concentrating the energy of the noise source near the peak of the output signal where its phase is least sensitive to noise perturbation. Lastly, the new circuit topology allows quadrature implementation of the VCO via capacitive coupling. Therefore, little or no phase noise degradation occurs since there are no additional active devices.

5.1 Circuit Analysis

Figure 5.1 shows a simplified schematic of the new VCO circuit. As can be seen, this is a variation of the cross-coupled transconductance VCO, where the bias transistor has been eliminated. MOS capacitors are inserted in the cross-coupled connecting paths, so that they form capacitive divider networks with the equivalent input capacitance of the switching transistors (gate-source capacitance plus Miller capacitance). The divider networks attenuate the driving signals of the switching transistors, thereby allowing their aspect ratios to be increased substantially without forcing the oscillator into the voltage-limited regime, the undesirable mode of operation where power is wasted because of output voltage clipping. The large W/L ratio keeps the transistors operating in the triode region even when conducting significant amount of current. This is quite beneficial because in this region, the transistor generates much less flicker noise than it does in the saturation region. This point is illustrated in Figure 5.2, which depicts the simulated noise spectral density for two NMOS transistors in the National Semiconductor Corp. (NSC) CMOS9 process with minimum length (180 nm) and width of 48 μm and 450 μm respectively, each carrying a drain current of 2 mA. Flicker noise in CMOS transistors is generated by the trapping and detrapping of carriers in the oxide layer. When a transistor operates in the triode/subthreshold region, a weak inversion channel is established under the oxide layer where the carrier concentration is substantially less than that in the strong inversion channel formed when the transistor is saturated. Additionally, the vertical electric field over the gate is smaller for the triode/subthreshold region than for the saturation region because of the smaller V_{GS}. These two factors combine to reduce the probability of carrier trapping events, thus reducing the flicker noise of the device.

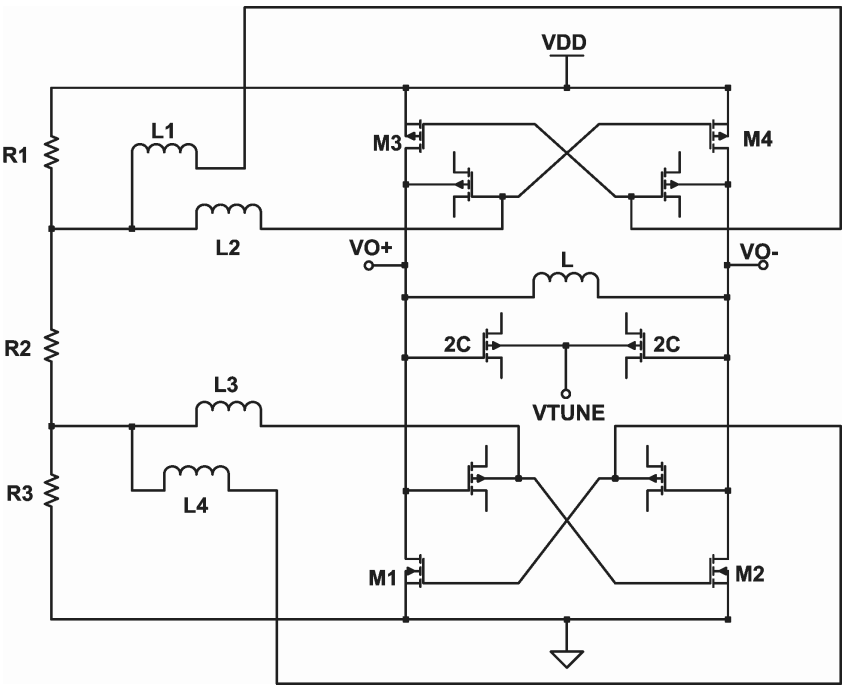

Figure 5.1 Simplified schematic of the new low-phase-noise VCO.

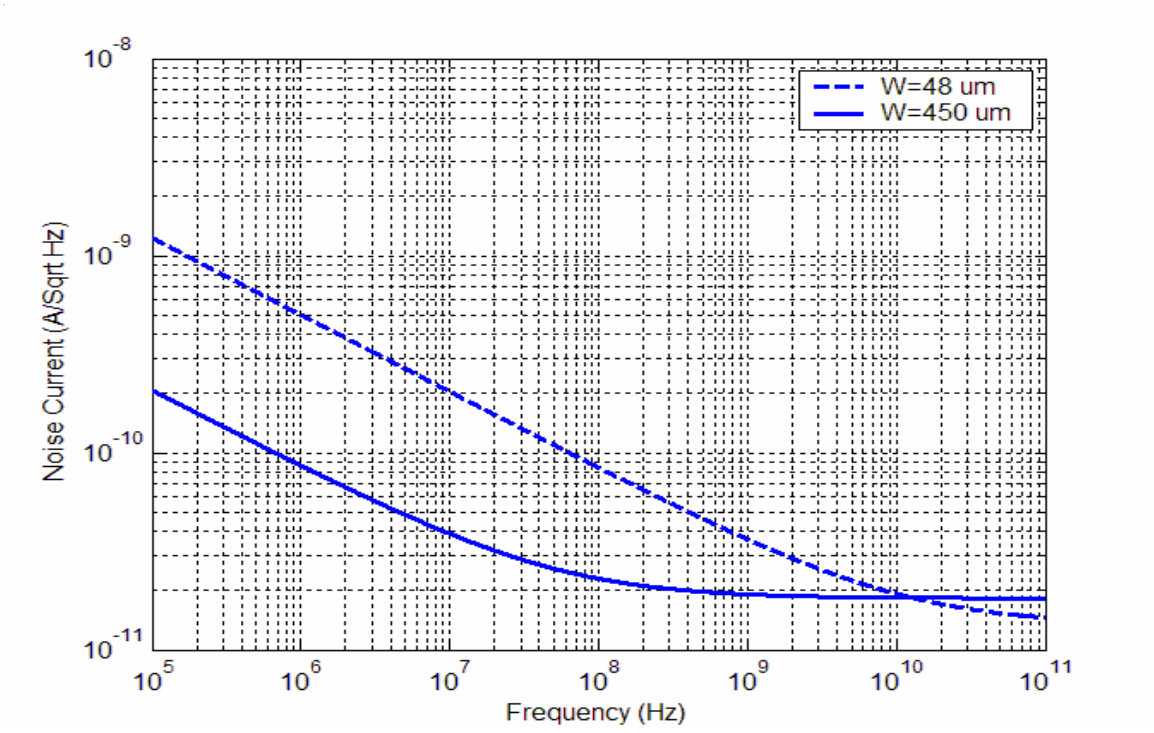

Figure 5.2 Noise spectral density of two NMOS transistor with the same drain current (2 mA), one in the saturation region, the other in the triode region.

These inserted MOS capacitors (feedback capacitors) eliminate the DC feedback paths from the output nodes of the VCO to the gates of the transconductors. Therefore, the resistor network R1-R3 is needed to bias the transconductors. To minimize the effect of circuit noise on the phase noise, the transconductors can be biased below the threshold voltages of the transistors so that the conducting drain current is relatively small near the zero-crossing points of the output waveform, where it is most sensitive to noise perturbation. However, in practice, the propagation delay (from v_{gs} to i_d) of the transistor shifts the current waveform (Figure 5.3) such that the drain current at one of the zero-crossing point is significantly increased (at phase angle=π), thereby diminishing this benefit. Nevertheless, this biasing scheme still provides on average lower drain current near the zero-crossing points than that of the cross-coupled transconductance VCO with fixed bias transistor. Additionally, because of the larger W/L ratio, the corresponding noise spectral density is lower for the same drain current, further reducing the phase noise.

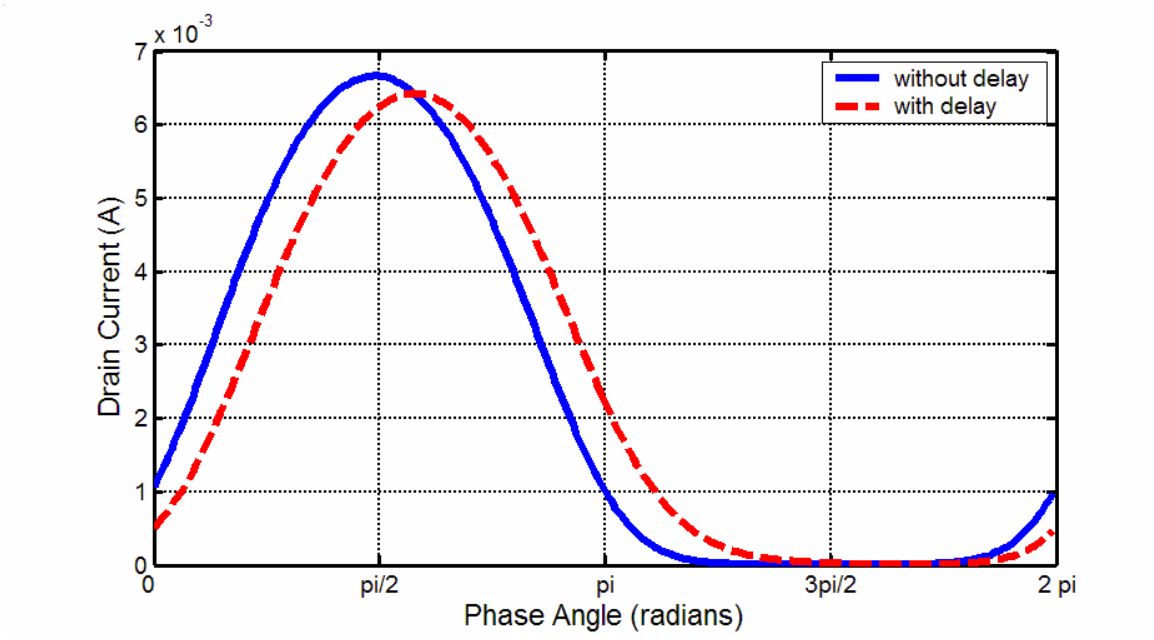

Figure 5.3 PMOSFET drain current during one cycle of oscillation.

Four identical inductors L1-L4 provide AC isolation (at the resonant frequency) between the gates of the NMOS and PMOS transistors. The quality factor of these inductors is not critical but their inductance value should be as large as possible for optimal isolation. Because the signals at the gates of either the NMOS or PMOS transistors are differential, the common terminals of inductors L1-L2 and L3-L4 are essentially AC ground. Therefore, to the extent that the isolation inductors are ideal and do not dissipate any power, there will be little or no leakage of the resonator energy to ground via the biasing circuit. It is noteworthy that to conserve chip area, isolation resistors may be used in place of inductors with some additional power dissipation and degradation of phase noise performance.

Because of the bias voltages being set below the threshold voltages of the transistors, this VCO circuit cannot start up by itself from a quiescent state. Therefore, a startup circuit, as shown in Figure 5.4, is necessary for reliable operation. It consists of four small CMOS switches (transmission gates), connected in parallel with the MOS feedback capacitors. Upon power-up, a control signal is used to turn these switches on for a short period. During this time, the MOS feedback capacitors are shorted out and the VCO essentially reverts to the familiar cross-coupled transconductor topology (without the bias transistor). In this condition, because of the large aspect ratios of the NMOS and PMOS devices and the lack of current limiting by the bias transistor, the effective negative resistance generated by the transconductors is more than sufficient to compensate for the loss of the resonator, which therefore will guarantee oscillation. Once the circuit oscillates and builds up sufficient output amplitude, the startup circuit can be disabled by turning off the CMOS switches with the control signal.

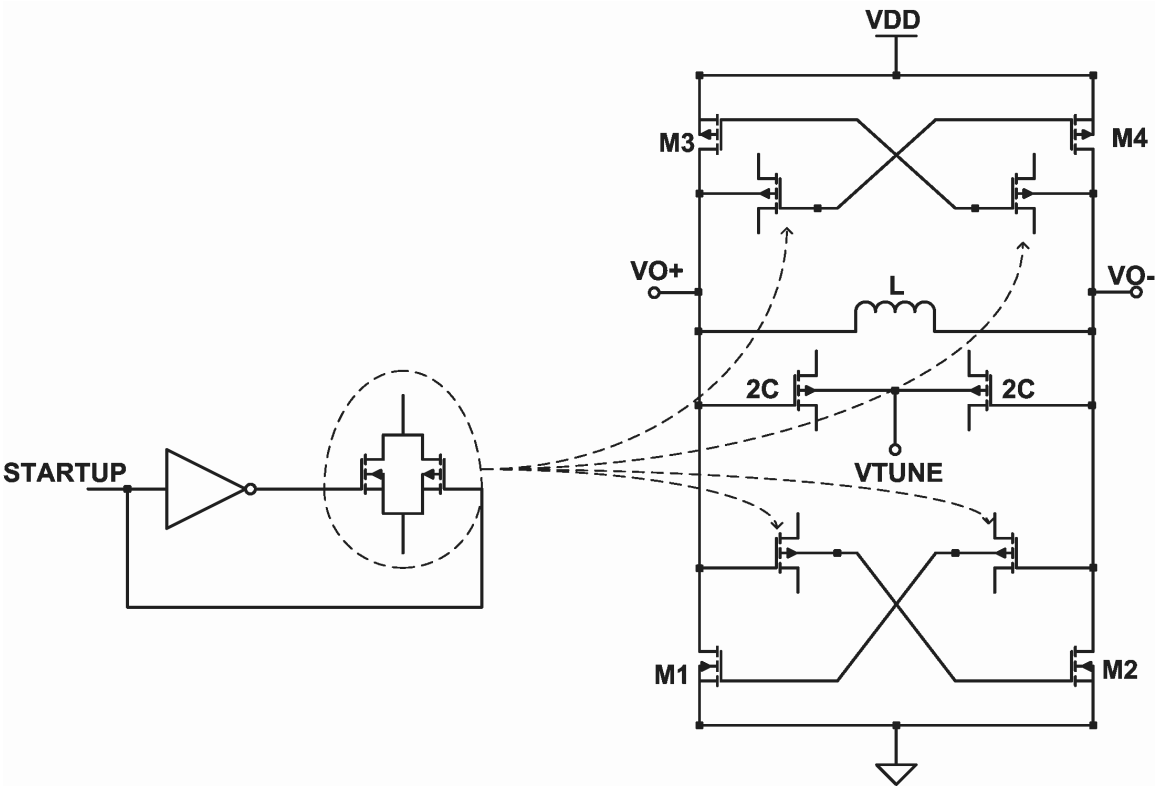

Figure 5.4 Simplified schematic of startup circuit for the new VCO.

When properly tuned, the ISF of each of the transistor noise sources does not have any DC component, resulting in no low-frequency noise being up-converted into phase noise. However, this optimal operating condition is quite sensitive to circuit components' variations such as resistance and capacitance tolerance. Although matching techniques can be used in the layout of the bias resistor network to reduce sensitivity, the same cannot be done for the capacitive dividers of the cross-coupled feedback paths since there is no correlation between the MOS capacitance and the parasitic gate-source capacitance (as well as Miller capacitance) of the transistors. Fortunately, the deviation from the optimal operating condition manifests itself in a shift of the nominal single-ended output DC voltage. Therefore, an automatic tuning circuit, as shown in Figure 5.5, can be used to

keep the VCO operating in the optimal condition. It consists of a differential-to-single-ended source follower (M1, M2) that drives a lowpass RC filter to derive the common-mode voltage of the VCO output. This DC signal is then compared with a reference DC voltage, which is also passed through an identical mirror follower circuit (M3, M4) for tracking components' variations. The output of the high-precision comparator drives a control logic block to generate the necessary control signals to adjust the bias voltages of the switching transistors such that the output common-mode voltage is maintained at its nominal value. The result is that the cancellation of the flicker-noise effect is also maintained.

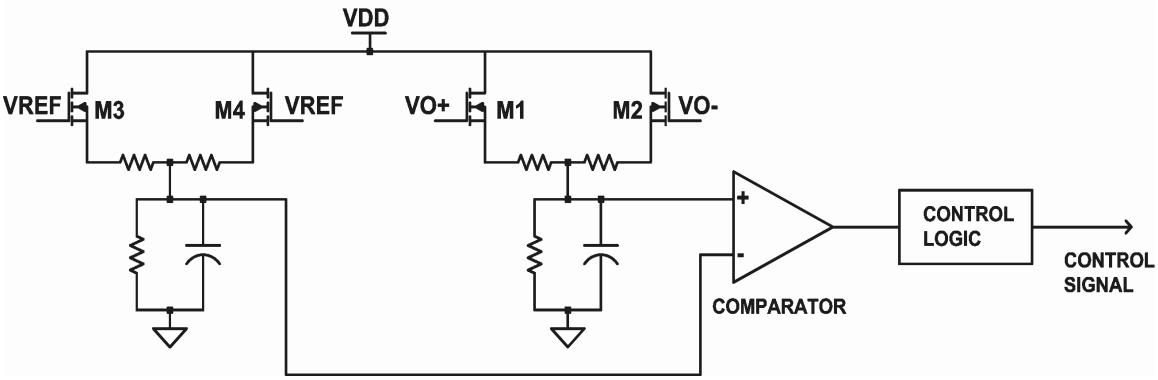

Figure 5.5 Simplified schematic of automatic tuning circuit for the VCO.

The tuning process can be performed discretely or continuously. The discrete tuning method switches on and off elements of a resistor network to vary its resistance, which in turn affects the corresponding bias voltage. The advantage of this approach is its simplicity and that virtually no additional noise is generated by the tuning circuit. However, it requires more chip area and the tuning resolution can be relatively coarse. On the other hand, continuous tuning is more difficult to design since care must be taken to

avoid excessive noise being injected into the main circuit. One possible implementation of continuous tuning is shown in Figure 5.6. The control signal is derived by integrating the output of the comparator. This voltage is then used to drive the gate of a PMOS transistor to vary its drain-source resistance. PMOSFET is chosen for its lower noise characteristics compared to those of NMOSFET. This transistor is placed in parallel with either bias resistor R1 or R3 of Figure 5.1 as a variable resistance to adjust the bias voltage of the switching transistors. It is noteworthy that any noise source in parallel with bias resistor R1 or R3 is amplified and injected into the resonator by both the NMOS and PMOS switching transistors, but with opposing polarity. Thus, depending on the VCO design, there may be significantly more cancellation of the noise source associated with one resistor than that corresponding to the other. Therefore, it is generally most beneficial to place the variable resistance in parallel with the bias resistor having more noise cancellation.

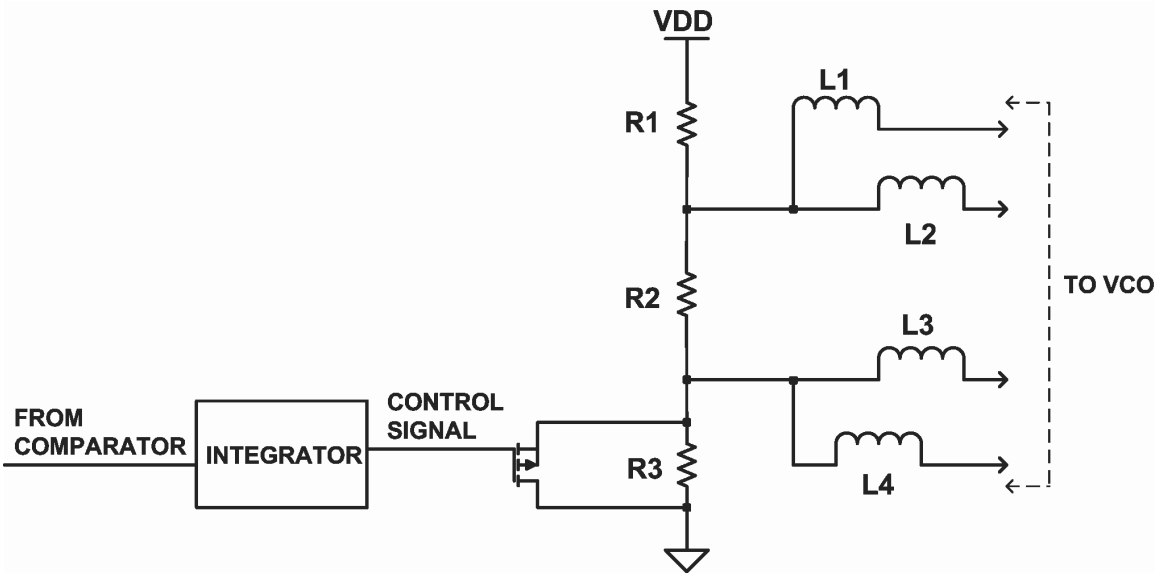

Figure 5.6 Simplified schematic of continuous tuning circuit.

One last attribute of the new VCO topology is in the ease of implementation of the quadrature oscillator. As shown in Figure 5.7, two identical oscillators are interconnected via capacitive coupling in a ring configuration. Each oscillator with its input coupling capacitors can be considered as a differential inverter, which when configured in a ring topology will generate quadrature output signals in steady state. Since there are no added active devices, the phase noise performance is not degraded. Furthermore, the value of the coupling capacitors can be much smaller (in the range of tens of femtofarads) than that of the feedback capacitors and the equivalent input capacitance of the switching transistors. Thus, the injected charge from one oscillator to the other is negligible and does not affect the current-voltage relationship of the resonator. Therefore, each VCO essentially operates in the same manner as in stand-alone mode.

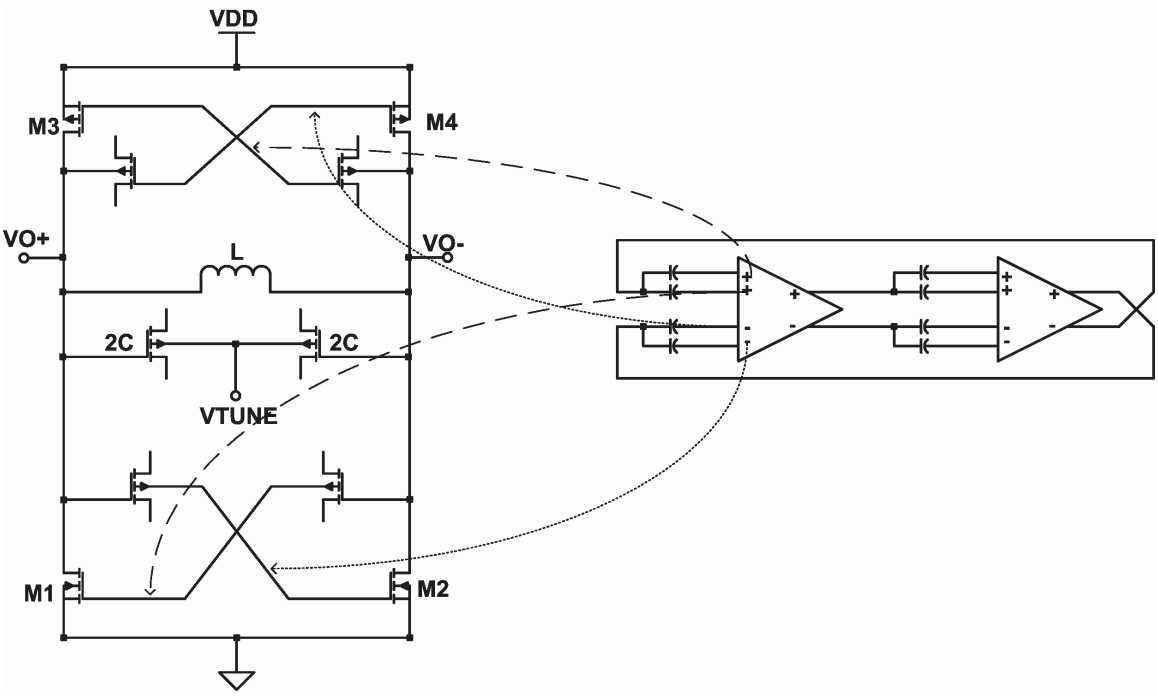

Figure 5.7 Schematic of the new quadrature VCO with capacitive coupling

5.2 Phase Noise Analysis

Figure 5.8 depicts the new VCO circuit with all the noise sources. The noise generated by the isolation inductors (L1-L4) is ignored since it is negligible compared to that generated by the bias resistors. On the other hand, the noise contribution of the parasitic series resistance of the resonator is similar to that described in the previous chapter, i.e., for low-Q system (<10) and low-phase-noise circuit topology, it must be taken into account. In fact, for the new VCO circuit proposed in this work and an inductor with a quality factor of about eight at 5.5 GHz, this noise source may be the most dominant, even at close-in offset frequency. Therefore, it is critical to have an optimal layout for the on-chip inductor and on-chip varactor as well as for the trace wiring between these two components.

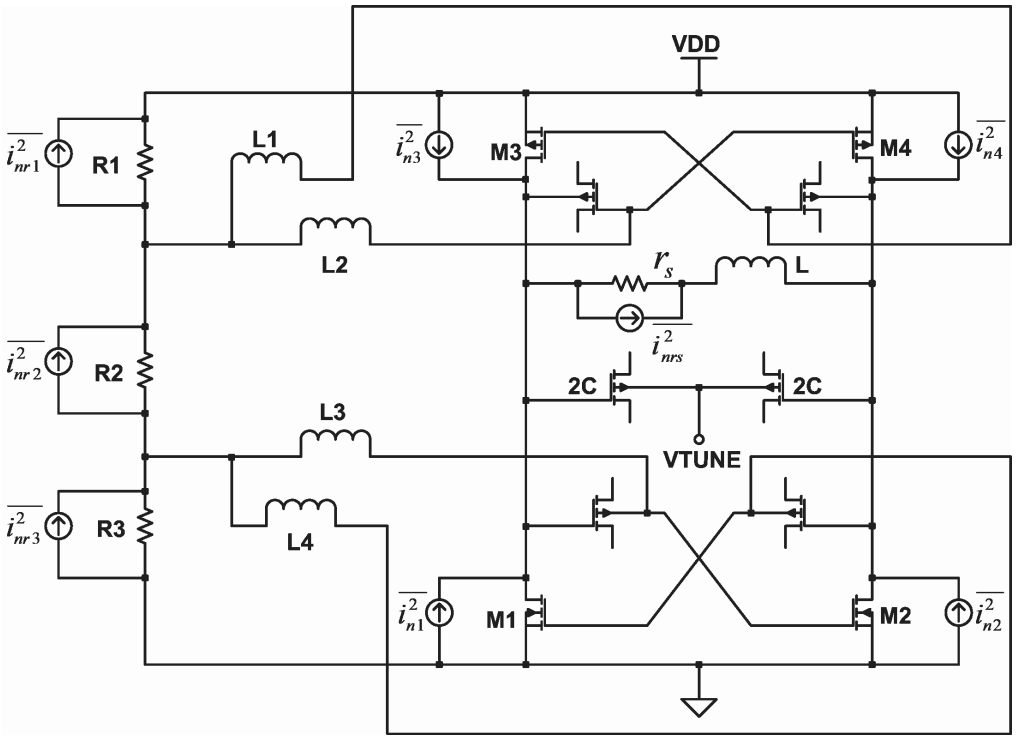

Figure 5.8 Schematic of new VCO with noise sources.

Similarly, the thermal noise sources of the bias resistors (R1-R3) must also be considered carefully. In this case, it is a tradeoff between power dissipation and noise contribution. As mentioned previously, these noise sources are amplified and injected into the resonator by the NMOS and PMOS transistors but with opposite polarity. Thus, there is some partial cancellation of the noise signals at the terminals of the resonator. Therefore, the effect they have on the phase noise is reduced. Because of this, relatively low bias current (less than one milliamp) is possible without any degradation of the phase noise generated by the active devices. Compared to the conventional VCO design, the current mirror adds 3 dB to the phase noise generated by the bias transistor for unity-current gain. To have negligible phase noise degradation, the current gain has to be less than one half. It means that the current in the mirror transistor has to be at least twice that of the bias transistor, a significant penalty in power dissipation.

The phase noise contribution of transistors M1 and M3 is analyzed next. Similar analysis can be applied for transistors M2 and M4 by symmetry. To cancel out the effect of flicker noise, the ISF corresponding to the noise source of M1 and M3 must not have any DC component. This can be accomplished with proper sizing of the NMOS and PMOS transistors as well as the cross-coupled feedback capacitors. However, the cyclostationary property of the noise source, resulting from the oscillation cycle of the transistor drain current, modulates the ISF waveform and regenerates a DC component. Fortunately, the feedback capacitors offer additional parameters that can affect the characteristics of the ISF. By adjusting the feedback ratios and/or the bias voltages of the switching transistors, the phase delay of the ISF can be changed to match the drain current waveform such that the effective ISF (product of the original ISF and the drain current

waveform) does not have a DC component. However, for simultaneous matching of the ISF of both the NMOS and PMOS transistors, their respective propagation delay (v_{gs} to i_d) must be the same. To understand this important requirement more clearly, let us examine the ideal case where the ISF is a perfect cosine waveform and the drain currents are perfect square waves. Note that the ISF corresponding to the NMOS transistor is the same as that of the PMOS device because both the noise sources are connected to the output node and AC ground (VDD and GND). Additionally, the NMOS and PMOS transistors conduct in different half of the oscillation cycle, as shown in Figure 5.9(a). As can easily be seen in Figure 5.9(b), both of the effective ISF's have zero average because of symmetry or perfect matching between the original ISF and the drain current waveform. This can be considered as the case of equal propagation delays, where the flicker noise effect of both the NMOS and PMOS transistors can be cancelled out by proper tuning of the VCO.

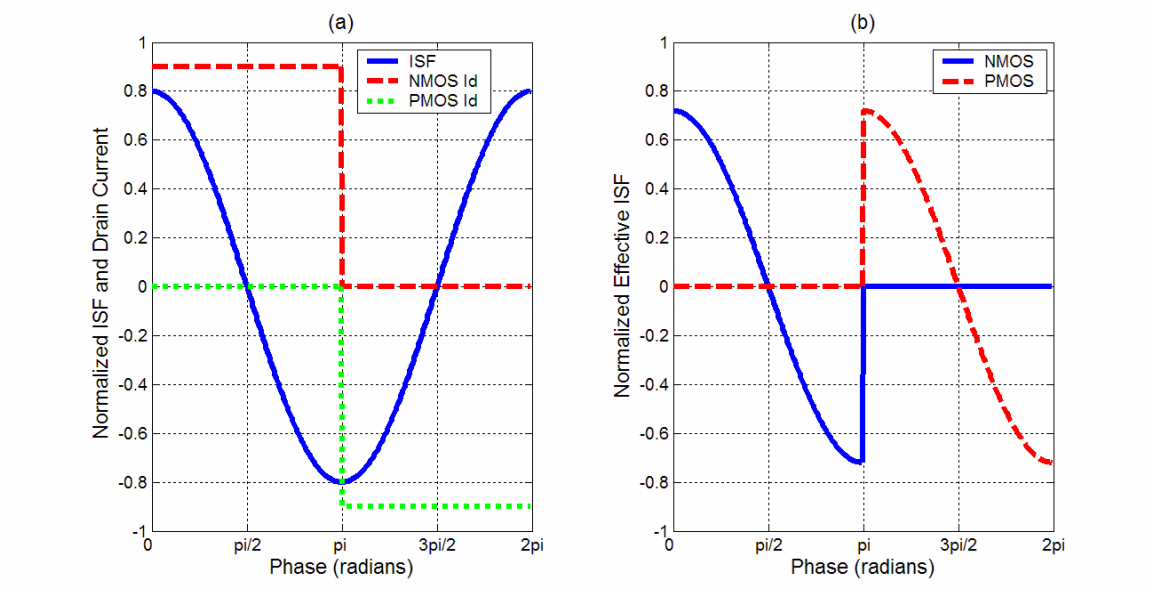

Figure 5.9 (a) Original ISF and drain currents with equal propagation delays
(b) Effective ISF with no DC component because of perfect matching.

If the current of the PMOS transistor is given a small phase shift, simulating the case of different propagation delay, as shown in Figure 5.10(a), the resulting effective ISFs are depicted in Figure 5.10(b), where the DC average of the waveform for the PMOS transistor clearly exists. This is the result of lack of matching between the original ISF and the current waveform. Though the bias voltages and/or feedback capacitors can be modified to change the phase of the ISF to match this PMOS current, any such action would inevitably create mismatch with the NMOS current. Therefore, the propagation delays of the NMOS and PMOS transistors must be the same to cancel the effect of all flicker noise sources on the VCO phase noise.

One final important point is that unlike the conventional cross-coupled design, the generated AM noise is not automatically suppressed in the new VCO topology because the switching transistors essentially still operate linearly at the peak of the output waveform, and it contributes to the overall sideband power of the output signal. The best approach to remove this noise source is to incorporate a gain-limiting mechanism to the output stage.

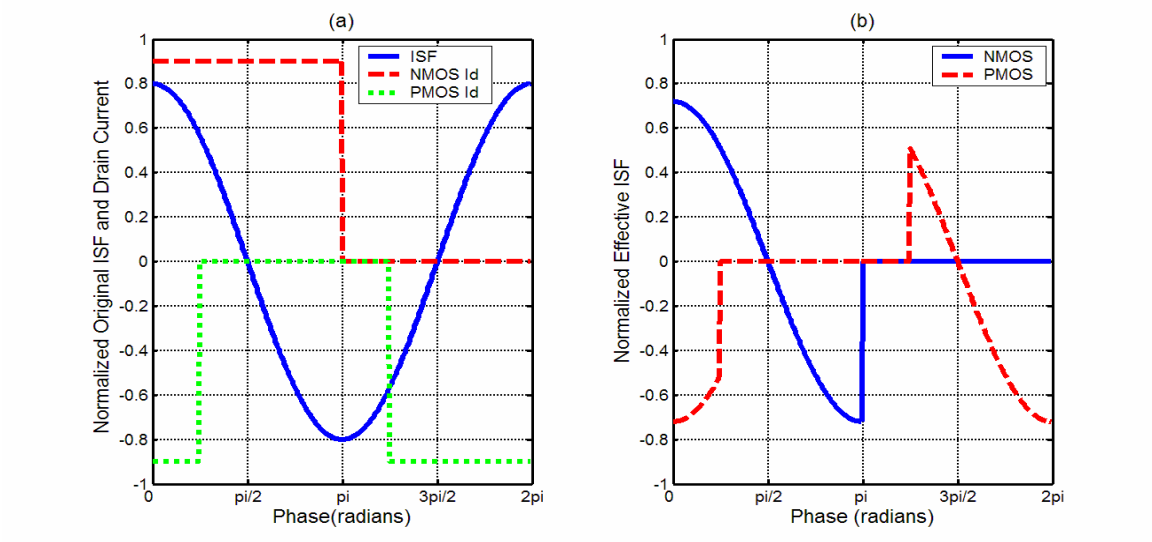

Figure 5.10 (a) Original ISF and drain currents with different propagation delays
(b) Effective ISF with DC component because of different delays.

5.3 Design Procedure

A recursive approach to designing the new VCO without the flicker-noise effect is necessary because it is difficult to derive analytically the ISF of the noise sources and the propagation delays of the switching transistors, the two most important elements for the optimization of phase noise performance. Figure 5.11 depicts a flow chart for this recursive algorithm, which is described in details below. It assumes that an optimal design of the on-chip tank inductor has been performed so that maximal Q is achieved at the lowest possible inductance value. The lower tank inductance is preferred because it allows a larger tank capacitance for a given resonant frequency, thereby increases the tuning range of the VCO. However, higher power dissipation for the same output voltage swing is required if its quality factor does not increase at least at the same rate as the inductance decreases, for the reason that the equivalent parallel resistance is lower.

The algorithm also assumes that the isolation inductors L1-L4 (Figure 5.1) have been designed and their simulation model is available. Unlike the tank inductor, their quality factor is not critical, while their inductance should be as large as possible to maximize the AC isolation at the frequency of oscillation. This objective can be accomplished using the stacked-inductor structure described in [46] with minimal chip-area requirement. Large inductance is possible because of the addition of the strong mutual inductances between the different layers.

It is also noteworthy that all the external loads to the VCO (i.e., output buffer, tuning circuit, startup circuit) should be previously designed and are present during this procedure because they can affect the optimal solution of the VCO design.

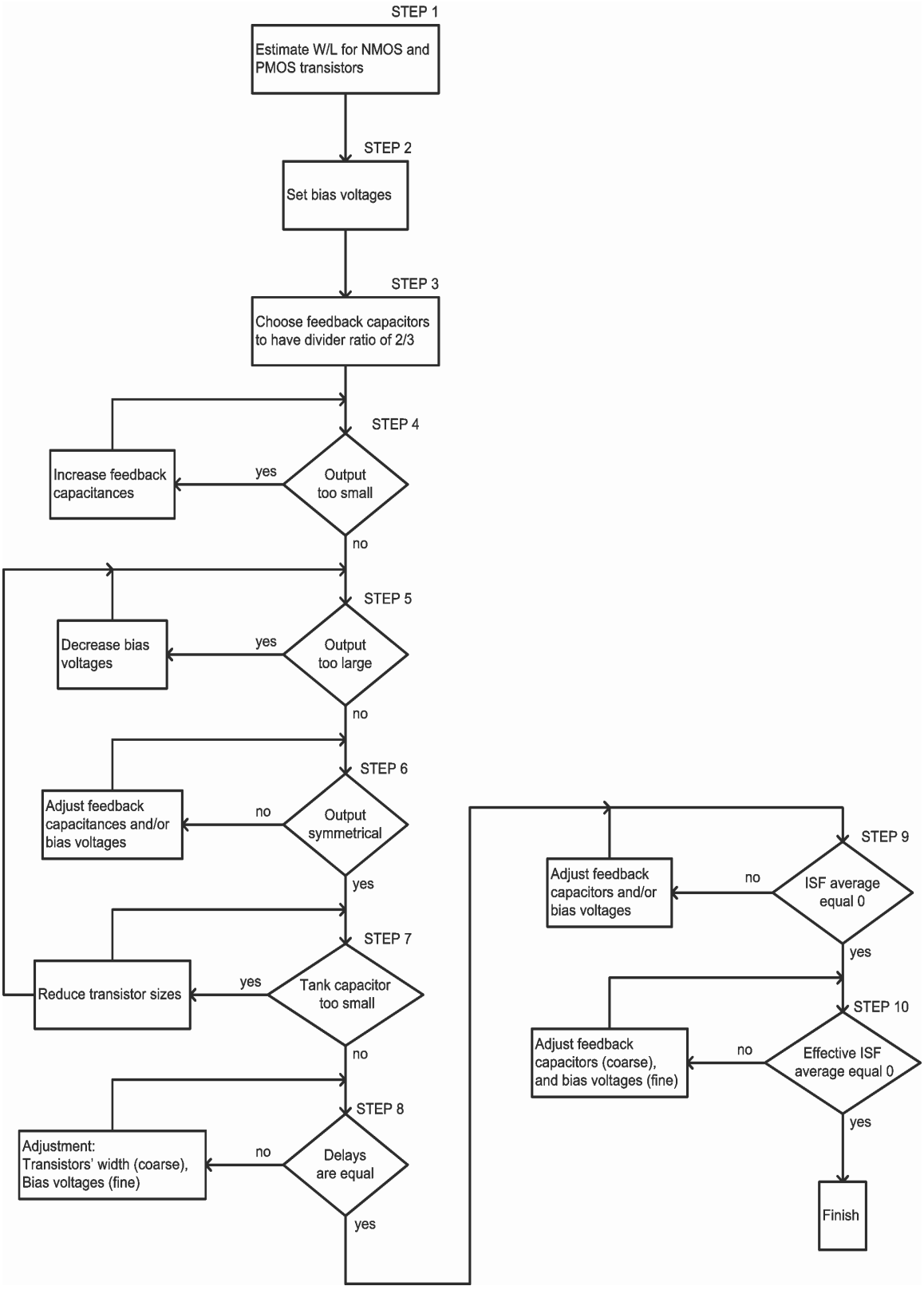

Figure 5.11 Flow chart of the design procedure of the proposed VCO

STEP 1: Determine the sizes of the switching transistors.

The aspect ratio of the switching transistors should be as large as possible so that they operate mostly in the triode region where the noise characteristics are lower, but not so large that their parasitic capacitances limit the tuning capability of the VCO, i.e., the tank capacitor is too small at the desired frequency. Additionally, since the NMOSFET has higher transconductance and noise than the PMOSFET, it is best to let its length be greater than the minimum length (L_{min}) of the process, typically between three and four times L_{min} to balance the performance between the two types of transistors.

For a given supply voltage V_{DD}, let the peak-to-peak single-ended output and the peak-to-peak feedback voltage be $V_{Opp} = 2/3 \cdot V_{DD}$ and $V_{FBpp} = 2/3 \cdot V_{Opp}$ respectively. Then, a good initial estimate of the aspect ratios of the transistors can be calculated as follows:

$$R_P = \frac{(\omega_0 L)^2}{r_s} = Q \cdot \omega_0 L$$

$$i_{Dpeak} = \frac{V_{Opp}}{R_P}$$

$$V_{DS} = \frac{V_{DD} - V_{Opp}}{2}$$

$$\left(\frac{W}{L}\right)_N = \frac{i_{Dpeak}}{K_N^{'} \cdot V_{DS} \cdot \left[\left(V_{FBpp} - V_{TN}\right) - V_{DS}/2\right]} \tag{5.1}$$

$$\left(\frac{W}{L}\right)_P = \frac{i_{Dpeak}}{K_P^{'} \cdot V_{DS} \cdot \left[\left(V_{FBpp} - V_{TN}\right) - V_{DS}/2\right]} \tag{5.2}$$

The reason for using V_{TN} in (5.2) is to have the same overdrive voltage for both of the NMOS and PMOS transistors. Though nominal values of the transconductance

parameters and threshold voltages can be used in evaluation of (5.1) and (5.2), a better estimate of the (W/L) ratios is possible if accurate values for the actual operating condition are available. Fortunately, they can be derived easily via simulation as described in Appendix C.

STEP 2: Set bias voltages.

The resistors R1-R3 (Figure 5.1) are used to set the bias voltages. Their value should be as large as possible to minimize power consumption, but not so large to dominate the phase noise of the VCO. The sum of these resistances typically should be less than 2 KΩ for their thermal noise to be negligible. However, the absolute values of these resistors are not important at this point since they can easily be scaled up or down at the final design stages.

Based on step 1, it is logical to set the bias voltages for the NMOS and PMOS transistors at $V_{FBpp}/2$ so that the feedback voltages do not exceed V_{DD} or GND. However, it may be difficult to have sustained oscillation at this time. Therefore, it is best to set them at $V_{DD}/3$ or even higher, to insure oscillation and let the recursive algorithm bring them back to the appropriate levels.

STEP 3: Determine the feedback capacitors.

First, the input capacitance of the switching transistors must be estimated. It is the sum of the gate-source capacitance and the Miller capacitance. The transconductance used in the computation of the Miller capacitance should correspond to the peak drain current i_{Dpeak}. The feedback capacitors are then chosen to obtain a feedback ratio of about 2/3. An approximate value for the tank capacitors, large enough for the desired

tuning range, is selected next before simulation can begin. Verify that the feedback ratio is reasonably close to the desired value to complete this step.

STEP 4: Output voltage is too small.

In the unlikely event that the single-ended output voltage swing is less than V_{Opp}, increasing the feedback capacitors will correct this problem. It is best to increase those associated with the voltage swing further away from the rail. It is not important to be very accurate for this parameter, and a tolerance of 10% is quite acceptable. Note that even though increasing bias voltages also accomplishes the same objective, doing so is not constructive since they are already set artificially high in step 2.

STEP 5: Output voltage is too large.

It is more likely that the output is too large, and in this case, it is an opportunity to reduce those bias voltages to more acceptable levels.

STEP 6: Output voltage is not symmetrical.

If the single-ended output voltage is not symmetrical, i.e., one peak is substantially further away from the respective rail than the other is; adjust the feedback capacitors and/or bias voltages to correct this problem.

STEP 7: Tank capacitor is too small.

If the tank capacitor is too small at the desired oscillation frequency, it means that the total parasitic capacitance is too high, and the sizes of the switching transistors must be reduced (including the length of the NMOS transistors). After this is performed, the

output voltage must be verified as in step 5, and this process continues until the desired tank capacitance is achieved.

STEP 8: Equalize propagation delays of NMOS and PMOS transistors.

In this step, the propagation delays of the NMOS and PMOS transistors are equalized. Since the transistor delay is proportional to its transconductance, it can be modified by adjusting its size and/or bias voltage. To obtain an accurate estimate of the delay, the transistor must be simulated with the capacitance load as is found in the VCO circuit. However, the exact load capacitance is difficult to obtain because of all the parasitic capacitances. An equivalent but easier approach is to simulate the device with identical terminal voltages as found in the oscillator circuit. A transient analysis can then be performed over once cycle of oscillation to obtain the drain current waveform. The oscillation frequency must be sufficiently low (10 MHz) so that the parasitic currents are negligible and the drain current can be accurately recorded. The delay is derived by comparison of this transient current waveform with a DC drain current response to the same gate voltage signal (Appendix D).

STEP 9: Remove DC from the ISF.

The purpose of removing the DC average from the ISF of the NMOS and PMOS transistors is to bring the design closer to the optimal solution without having to do a full simulation as in step 10. First, a transient analysis of the VCO circuit is performed without noise perturbation. Next, a similar simulation with noise impulse injected at equally-spaced time within a period of oscillation is carried out. The ISF is then derived from the phase difference of the two output signals. The DC component of the ISF can be

made more positive (negative) by increasing (decreasing) the feedback capacitors and/or the bias voltage corresponding to the PMOS transistors. Doing the same for the NMOS transistors has the opposite effects. Generally, reducing the bias voltages is preferred since it leads to lower phase noise. However, it may not always be possible to do so because of other factors such as output voltage swing and feedback capacitors being too large. Additionally, since increasing (decreasing) the bias voltage increases (decreases) the corresponding transistor delay, it is possible to equalize the delays even more while tuning to remove the DC component of the ISF.

STEP 10: Remove DC from the effective ISF.

To obtain the effective ISF, the original ISF is first derived by the same procedure described in step 9. Next, the drain current waveform of the transistor is estimated by applying the propagation delay effect to the DC current response to a voltage sweep of one oscillation cycle. This is necessary because at high frequency in the gigahertz range, the drain current cannot be accurately recorded from simulation result because of the presence of significant parasitic currents. The effective ISF is simply the product of the two waveforms, and its DC average can be affected in a similar manner as described in step 9. Additionally, the noise characterization of the active devices are also carried out at this time, and the results along with the effective ISF are used to compute the oscillator phase noise as described in Equation 2.27. The simulations and computations in this step are presented in more details in the next chapter. Once this step is completed, the noise contribution from the bias resistors can be evaluated, and their values can be scaled up or down appropriately to minimize their power consumption and phase noise degradation.

5.4 Design of a 5.5-GHz VCO

In this section, the above procedure is applied to design a 5.5 GHz oscillator using National Semiconductor Corp (NSC) 0.18-μm CMOS9 process. Before the procedure can be started, all of the peripheral components (inductors, buffer, startup, tuning, etc.) must be designed to be included in the VCO circuit. They are discussed in the sections below, followed by the section on the main design.

5.4.1 Inductors

The Q of the on-chip tank inductor greatly affects the phase noise of the VCO. Therefore, it is critical to optimize this parameter before all others. In this design, octagonal shape is used for the layout of the inductor since it can contain more trace metal in a given area than the more common square pattern, leading to smaller series parasitic resistance. The software ASITIC developed by University of California Berkley is used to design the inductor and develop its lumped model. It is found that a structure with two turns offers the best combination of Q and resonant frequency. A single-turn structure has little substrate loss, but its low inductance results in poor quality factor. Structure with more than two turns suffers more parasitic effects; thus reducing its Q and resonant frequency. The parameters of the tank inductor are summarized in Table 5.1, and its circuit model is shown in Figure 5.12.

On the other hand, the inductance of the on-chip isolation inductors is more important and should be as large as possible to maximize the isolation effect at the resonant frequency. Thus, a stacked structure is more suitable for this application. Their design parameters are shown in Table 5.1, and the schematic is shown in Figure 5.13.

Table 5.1 Design parameters for on-chip inductors.

Design Parameters	Tank Inductor	Bias Inductor
Shape	Octagon	Square
Outer dimension	185.44 μm	60 μm
No. of layer	1 (met5)	4 (met2-met5)
No. of turns/layer	2	4
Trace Width	25 μm	4 μm
Spacing between trace	1 μm	0.4 μm
Predicted Q (ASITIC)	8	1

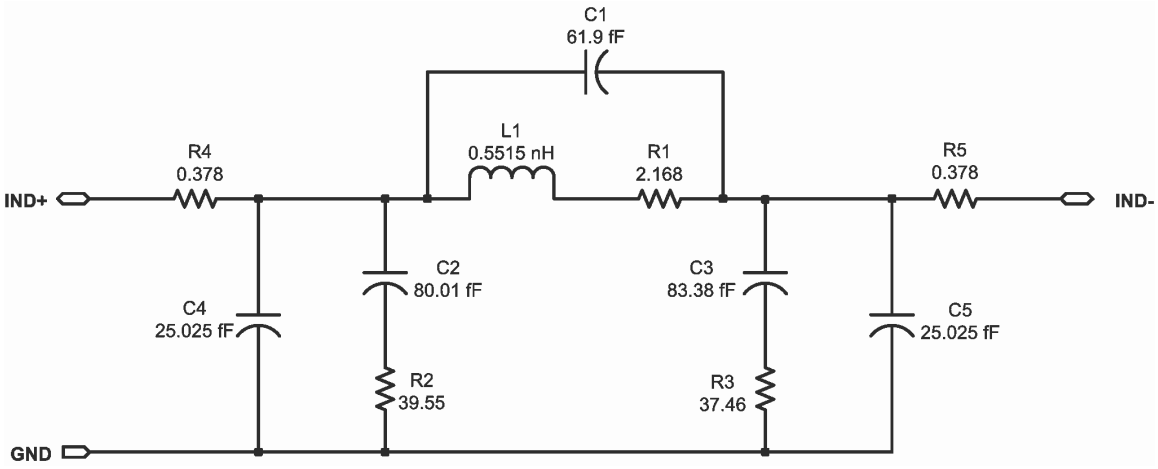

Figure 5.12 Schematic of lumped model of tank inductor.

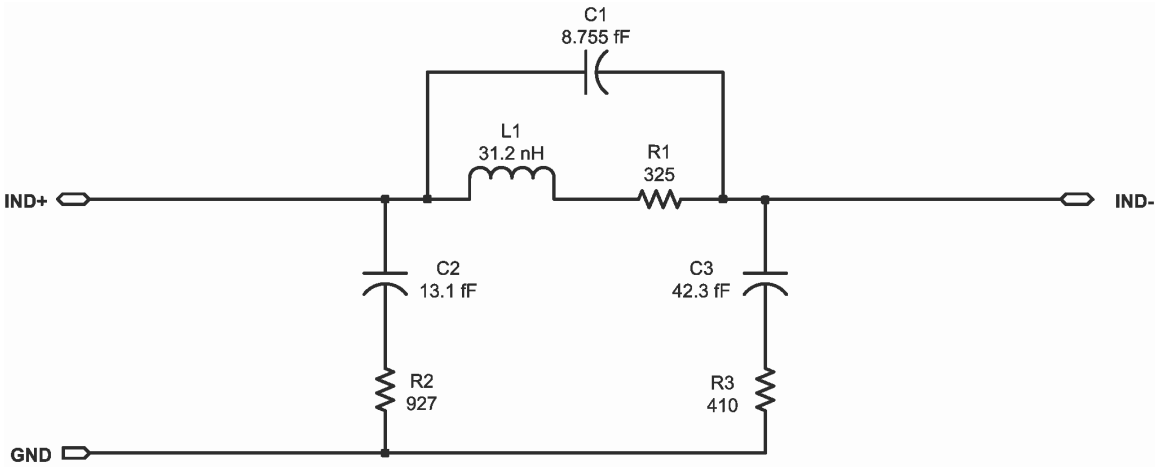

Figure 5.13 Schematic of lumped model of isolation inductor.

5.4.2 Output Buffer

The output buffer provides current to drive an external load to the VCO, which in this case is a 50-Ω input impedance of the spectrum analyzer. A differential PMOSFET source follower circuit is the selected topology because a PMOS device has lower noise characteristics than an NMOS transistor. To keep the noise low, the W/L ratio of the PMOSFET is chosen to be quite large (184μm/0.18μm) so that the device operates in the triode region. Additionally, a step-down transformer (8:1) is placed between the buffer and the 50-Ω load to reduce the current drive requirement (thus reducing device noise). The primary coil of the transformer is a spiral structure with 8 turns (2.5-μm trace width) on metal-5 (top) layer, while the secondary coil is a spiral with one turn (24-μm trace width) on metal-4 layer. With this design, the noise contribution from the buffer is negligible. The disadvantage is that it is not possible to measure phase noise at much further than 1-MHz offset frequency because it is below the noise floor of the test instrument. However, it is not a significant drawback since the interest is mostly on the close-in phase noise. Figure 5.14 shows the schematic of this output buffer circuit.

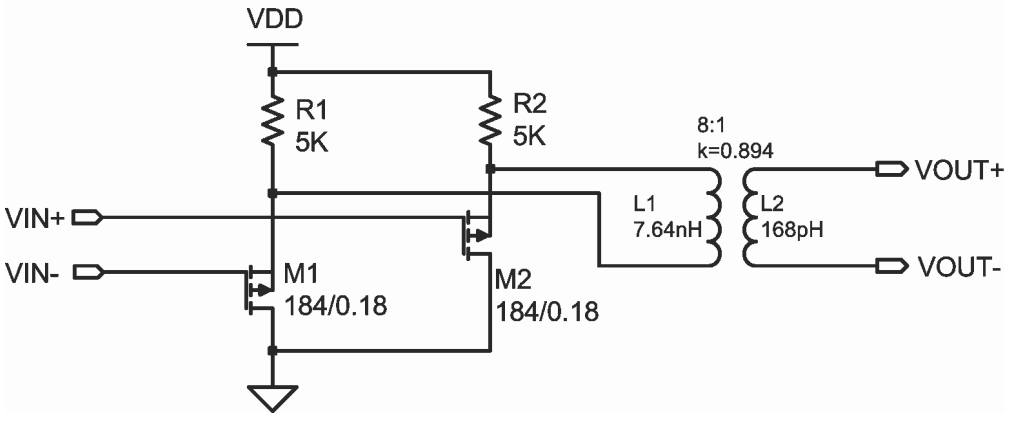

Figure 5.14 Schematic of output buffer of the VCO.

5.4.3 Startup Circuit

The startup circuit consists simply of four CMOS switches, each placed in parallel with one of the four feedback capacitors. During startup, the control signal goes HIGH, turning on the switches, which bypass the corresponding feedback capacitors and create a cross-coupled configuration. With their large aspect ratios, the equivalent negative resistance generated by the switching transistors is more than sufficient to compensate for the loss of the resonator and oscillation will occur. The switches are then turned off and the oscillator returns to normal operation. Figure 5.15 shows the partial schematic of the startup circuit (one of four switches).

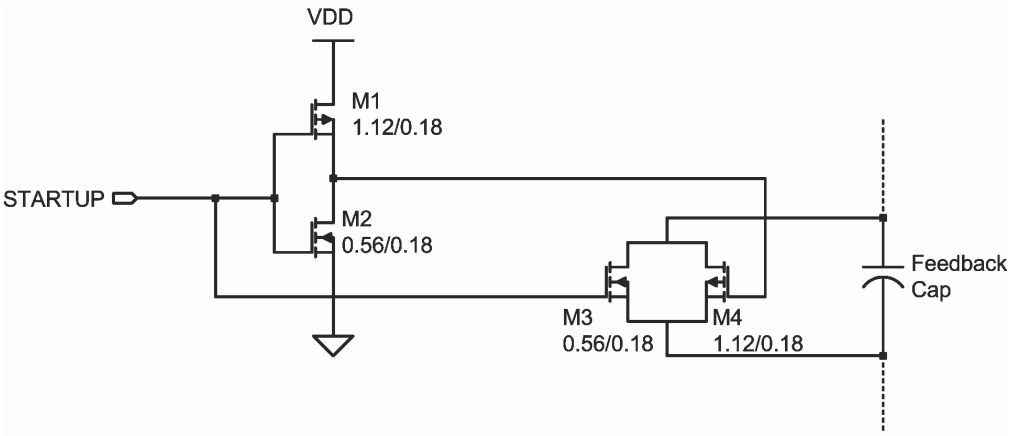

Figure 5.15 Partial schematic of startup circuit.

5.4.4 Tuning Circuit

Figure 5.16 depicts the schematic of the tuning circuit for the oscillator. It is not intended to be an automatic tuning circuit in order to simplify the testing of the VCO. The circuit consists of a differential amplifier/lowpass filter followed by an RC-lowpass filter, which converts the oscillator differential output to a single-ended DC signal. A similar

amplifier is used to generate the reference DC voltage and to track parameter variations of the differential amplifier. The bias voltages of the switching transistors are adjusted to keep the two DC voltages equal, thus keeping the VCO operate near the optimal condition.

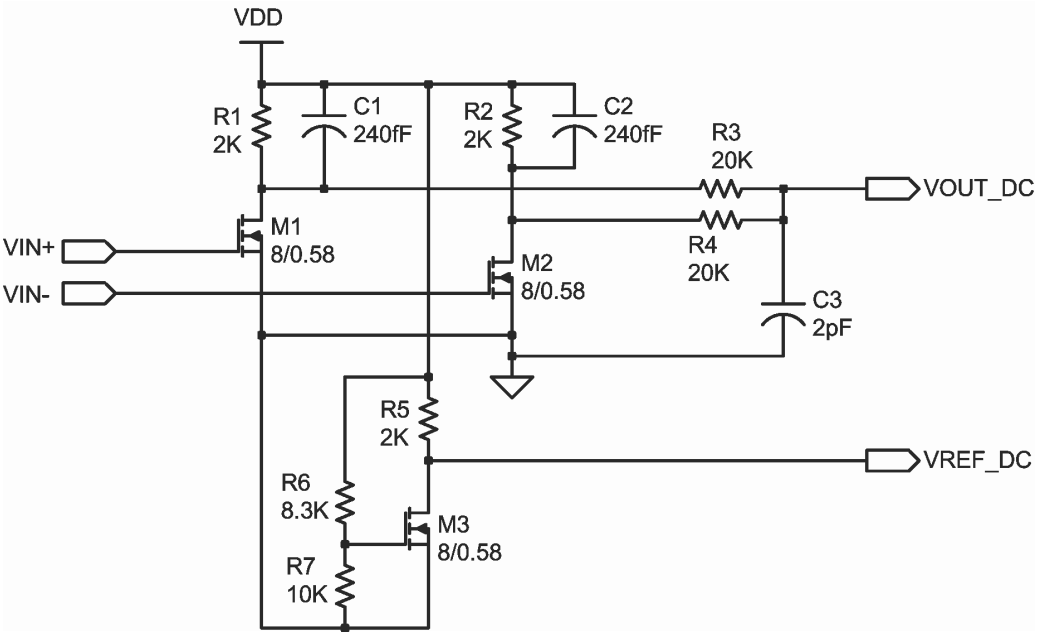

Figure 5.16 Schematic of tuning circuit for the VCO.

5.4.5 Main VCO Circuit

STEP 1:

The nominal power supply for this process is $V_{DD} = 1.8V$. Thus, the estimated design parameters of the oscillator are as follows:

$$V_{Opp} = 2/3 \cdot V_{DD} = 1.2V \ , \ V_{FBpp} = 2/3 V_{Opp} = 0.8V \ , \ V_{DS} = 1/6 \cdot V_{DD} = 0.3V$$

Using the method described in Appendix C, the transconductance parameters and threshold voltages of the transistors are derived to be

$$V_{TN} = 300mV \ , \ K_N^{'} = 212\mu A/V^2 , \ V_{TP} = 398mV \ , \ K_P^{'} = 61\mu A/V^2$$

Next, the peak drain current is estimated.

$$R_P = (\omega_0 L)^2 / r_s = \left(2\pi \cdot 5.5e^9 \cdot 0.551e^{-9}\right)^2 / 2.168 = 167\Omega$$

$$i_{Dpeak} = V_{Opp} / R_P = 1.2/167 = 7.176mA$$

Substitute these parameters into (5.1) and (5.2) to calculate the aspect ratios for the NMOS and PMOS switching transistors.

$(W/L)_N = 322$, $(W/L)_P = 1120$

Let $L_N = 0.62\mu m$, $L_P = 0.18\mu m$

Then $W_N = 200\mu m = 4 \times 25 \times 2\mu m$, $W_P = 200\mu m = 4 \times 25 \times 2\mu m$

Each of the transistors is implemented as four parallel devices of appropriate length. Each device has 25 fingers with 2-μm width.

STEP 2:

The bias voltages are arbitrarily set at a high level to insure that sustained oscillation is possible. The NMOS bias voltage is chosen to be one-third of the supply voltage, and the PMOS bias voltage is chosen to be 100mV higher so that both transistors have the same overdrive voltage for similar feedback signals (V_{TP} is greater than V_{TN} by about 100mV). The resulting values of the bias resistors R1-R3 are then 700Ω, 500Ω, and 600Ω respectively.

STEP 3:

Since the parasitic capacitance coefficients are not readily available from the given transistor model, an arbitrary value of 1.5pF is chosen for all feedback capacitors. This value is probably higher than necessary, but the recursive algorithm will bring it down to the appropriate level in the subsequent steps. The tank capacitance is also chosen to be

1.5pF to complete the initial design of the VCO. Since a good model of the MOS capacitor is not available for this process, all capacitances are implemented with poly-poly capacitors to make it easier to verify the design concept of this new VCO topology. A transient analysis is then performed with a 25-ns startup period. The single-ended output voltage swing is 1.319V, and the NMOS and PMOS feedback voltage swings are 0.807V and 1.048V respectively. With the PMOS feedback capacitors changed to 0.7pF, all the feedback voltages are found to be satisfactorily close to the desired value of 0.8Vp-p.

$V_{Opp} = 1.307V$, $V_{FBpp(NMOS)} = 0.794V$, $V_{FBpp(PMOS)} = 0.823V$

STEP 4:

The output signal is obviously not too small.

STEP 5 & 6:

The bias resistors are adjusted to make the single-ended output more symmetrical and its level closer to 1.2Vp-p. The resulting values for R1-R3 are 620Ω, 640Ω, and 540Ω respectively.

STEP 7:

The resonant frequency of the above analysis is found to be approximately 5.2 GHz instead of 5.5 GHz, indicating that the parasitic capacitance is too high. To bring the oscillation frequency closer to the desired number, the sizes of the switching transistors are reduced as follows:

$(W/L)_{NMOS} = 4 \times 16 \times 2\mu m/0.54\mu m$, $(W/L)_{PMOS} = 4 \times 18 \times 2\mu m/0.18\mu m$

The bias resistors and feedback capacitors are also adjusted to bring output signal close to the desired level.

$$R1 = 640\,,\ R2 = 600\,,\ R3 = 560\,,\ C_{FB(NMOS)} = 1.5pF\,,\ C_{FB(PMOS)} = 0.8pF$$

STEP 8:

The propagation delay of the NMOSFET and PMOSFET are estimated using the test circuit described in Appendix D to be 6.090ps and 6.328ps respectively. Since they are approximately the same, no changes are needed for this step.

STEP 9 & 10:

With the simulation method described in the next chapter, it is often more convenient to execute step 9 and 10 concurrently. By appropriately adjusting the feedback capacitors and bias voltages, the optimal design is obtained. The final values of components in the design are summarized in Table 5.2.

Table 5.2 Component values of the final design of the VCO.

Component	Value
NMOS switching transistors	4x14x1.96μm/0.54μm
PMOS switching transistors	4x18x2.16μm/0.18μm
NMOS feedback capacitors	0.720pF
PMOS feedback capacitors	1.320pF
Bias resistor R1	572Ω
Bias resistor R2	615Ω
Bias resistor R3	590Ω
Tank capacitor	1.5pF

CHAPTER 6
SIMULATION AND EXPERIMENTAL RESULTS

6.1 Simulation Methodology

The following simulation methodology can be implemented to compute the phase noise contributed by any noise source present in the VCO circuit. It is suitable for use with the iterative algorithm described in the previous chapter for minimizing phase noise resulting from the flicker noise of the switching transistors. A MATLAB script (Appendix E) is developed to facilitate this simulation procedure.

The first task is to derive the ISF corresponding to the noise source, which requires two transient simulations of the VCO circuit. The first analysis is performed without any noise perturbation whose simulation time (T_{trans}) is dependent on the number of desired samples per period of the ISF (NISF=16 typically), as shown in Equation 6.1. T_0 is the settling time of the oscillator at startup and should be greater than 100 ns for a 5.5-GHz VCO frequency. $tper$ is the oscillation period which is computed from the simulated output signal. FFT_LEN is the number of data samples (4096) used in the computation of the FFT of the output waveform. $N2$ is the number of data samples (256) per oscillation period. The term in parentheses defines the simulation time, in terms of oscillation period, needed to compute the phase shift caused by one injected noise impulse. It includes the data window itself and some settling time before the phase of the oscillator output can be calculated accurately.

$$T_{trans} = T_0 + NISF \cdot tper \cdot \left(\frac{5 \cdot FFT\_LEN}{N2} + 1 \right) \tag{6.1}$$

Once the analysis is completed, the following signals are to be recorded and entered into the MATLAB script: the VCO differential output, the common collector voltage of the NMOS and PMOS transistor (i.e. the single-ended VCO output), the gate-source voltage of the NMOS device, and the gate-source voltage of the PMOS device. For a white noise source such as that of a resistor, only the differential output is required. In any case, it is used to compute the oscillation period (lines 28-64 of MATLAB script), which is then used to calculate the initial delay time and period of the noise current source (lines 65-80) for the second transient simulation. The energy of the injected noise impulse should be large enough that numerical errors are negligible with respect to the resulting phase shift, but not too large that the VCO responds nonlinearly to the perturbation. A typical choice is a 1-mA current with a 1-ps pulse width. The rise and fall time of the current pulse should also be as small as possible (10 fs or less) to emulate an ideal impulse.

The second transient analysis can now be performed with the above noise source, included in the circuit and the resulting differential output is recorded and inputted into the MATLAB script. A scaled version of the ISF (*gamma*1) is then determined by calculating the phase difference between the two differential outputs of the transient simulations (lines 82-155). This function is also defined by Equation 6.2 where Γ is the ISF, *ipm* and *ipw* are the injected noise magnitude and pulse width respectively, and $q_{\max}$ is the maximal charge swing of the resonator. If the noise source is white, its Fast Fourier Transform (FFT) is then computed, from which its DC and AC components are determined as in (6.3) and (6.4), where N_2 is the number of data points used in the FFT.

The phase noise contribution from this noise source can then be calculated using (2.27) as follows (lines 384-395), where $S_{thermal}$ is the current noise spectral density:

$$gamma1 \equiv \Delta\phi \equiv \Gamma \cdot \frac{\Delta q}{q_{\max}} = \Gamma \cdot \frac{ipm \cdot ipw}{q_{\max}} \tag{6.2}$$

$$GAMMA1 = FFT(gamma1)$$

$$c_0 = \frac{q_{\max}}{ipm \cdot ipw} \cdot \frac{GAMMA1(0)}{N_2} \tag{6.3}$$

$$c_n = \frac{q_{\max}}{ipm \cdot ipw} \cdot \frac{2 \cdot GAMMA1(n)}{N_2} \tag{6.4}$$

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2I_0^2c_0^2 + \sum_{n=1}^{\infty} I_n^2c_n^2}{8q_{\max}^2\Delta\omega^2}\right] = 20\log_{10}\left[\frac{\left(\sqrt{2c_0^2 + \sum c_n^2}\right)\cdot I_0}{2\sqrt{2}\cdot q_{\max}\cdot\Delta\omega}\right]$$

$$L(\Delta\omega) = 20\log_{10}\left[\frac{\left(\sqrt{2\cdot GAMMA1(0)^2 + \sum 4\cdot GAMMA1(n)^2}\right)\cdot\sqrt{2}\cdot S_{thermal}}{2\sqrt{2}\cdot N_2\cdot ipm\cdot ipw\cdot\Delta\omega}\right]$$

$$L(\Delta\omega) = 20\log_{10}\left[\frac{\left(\sqrt{GAMMA1(0)^2 + \sum 2\cdot GAMMA1(n)^2}\right)\cdot S_{thermal}}{\sqrt{2}\cdot N_2\cdot ipm\cdot ipw\cdot\Delta\omega}\right] \tag{6.5}$$

If the noise source is cyclostationary such as that of the switching MOSFETs, the effective ISF needs to be computed, and the noise of the transistor has to be characterized. With the saved data from the first transient analysis, the terminal voltages of the active device can be determined and applied to the test circuit described in Appendix D to perform the four following simulations.

1) A transient analysis for one cycle of the gate voltage at a frequency of 10 MHz is performed to obtain the drain current waveform. The low signal frequency

insures that the parasitic currents at the drain terminal are negligible, and the drain current itself can be accurately recorded.

2) A DC analysis is performed, sweeping the gate voltage to cover a range of values that includes both the minimal and maximal values of the gate signal during normal operation of the VCO circuit. The drain current is recorded and used to construct an ideal drain current waveform with no propagation delay for one cycle of oscillation. This ideal waveform is compared to the result of the previous simulation to estimate the propagation delay of the transistor (lines 241-278). This delay is then used to estimate one cycle of the drain current at the actual frequency of oscillation (lines 280-328).

$$i_{D(delay)} = F_1(\omega_0 \tau) \tag{6.6}$$

3) A noise analysis is performed at 10 KHz with the same sweeping gate voltage as in the second simulation. The results are combined with those of the previous DC analysis to express the noise spectral density in terms of the DC drain current.

$$S_n(10KHz) = F_2(I_D) \tag{6.7}$$

By substituting (6.6) into (6.7), the noise spectral density for one cycle of oscillation can be derived, which can be expressed as the product of an arbitrary white noise source and a function describing the cyclostationarity of the device. This function is combined with the original ISF to obtain the effective ISF.

$$S_n(10KHz) = F_3(\omega_0 \tau) = S_0 F_4(\omega_0 \tau) \tag{6.8}$$

4) A noise analysis is performed with sweeping frequency from 10 KHz to 5 GHz where it is assumed that the thermal noise of the device dominates and its

flicker noise is negligible. The thermal noise is converted to phase noise by the AC components of the effective ISF while low-frequency noise is converted to phase noise by the DC component. The results of this simulation allow extrapolation of the phase noise computation at frequencies other than 10 KHz.

The results of all four above simulations are saved and inputted into the MATLAB script, and Equation 2.27 is again used to perform the phase noise computation as follows (lines 345-365):

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2I_0^2c_0^2 + \sum_{n=1}^{\infty} I_n^2c_n^2}{8q_{\max}^2\Delta\omega^2}\right]$$

Substitute (6.3) and (6.4) into the above equation to obtain the following, where $S_0(\Delta\omega)$ is the flicker noise spectral density, and $S_{thermal}$ is the thermal noise spectral density of the transistor.

$$L(\Delta\omega) = 10\log_{10}\left[\frac{S_0^2(\Delta\omega)\cdot GAMMA1(0)^2 + \sum 2S_{thermal}^2\cdot GAMMA1(n)^2}{2\cdot N_2^2\cdot(ipw\cdot ipm)^2\cdot\Delta\omega^2}\right] \qquad (6.9)$$

Either (6.5) or (6.9) is used to compute the phase noise contribution of each noise source in the VCO circuit, and the results are summed (root mean squared sense) together to obtain the overall phase noise performance of the oscillator.

Finally, a plot of the DC component versus the delay of the ISF, as shown in Figure 6.1, can be used to aid in the cancellation of the DC component of the ISF. A minimum to the right of the x-axis origin indicates that the transconductance of the corresponding transistor needs to be decreased (decreasing feedback capacitance and/or bias voltage), while a minimum to the left indicates that the transconductance has to be increased. A

minimum at the x-axis origin means that the DC component is minimized and the optimal solution has been obtained.

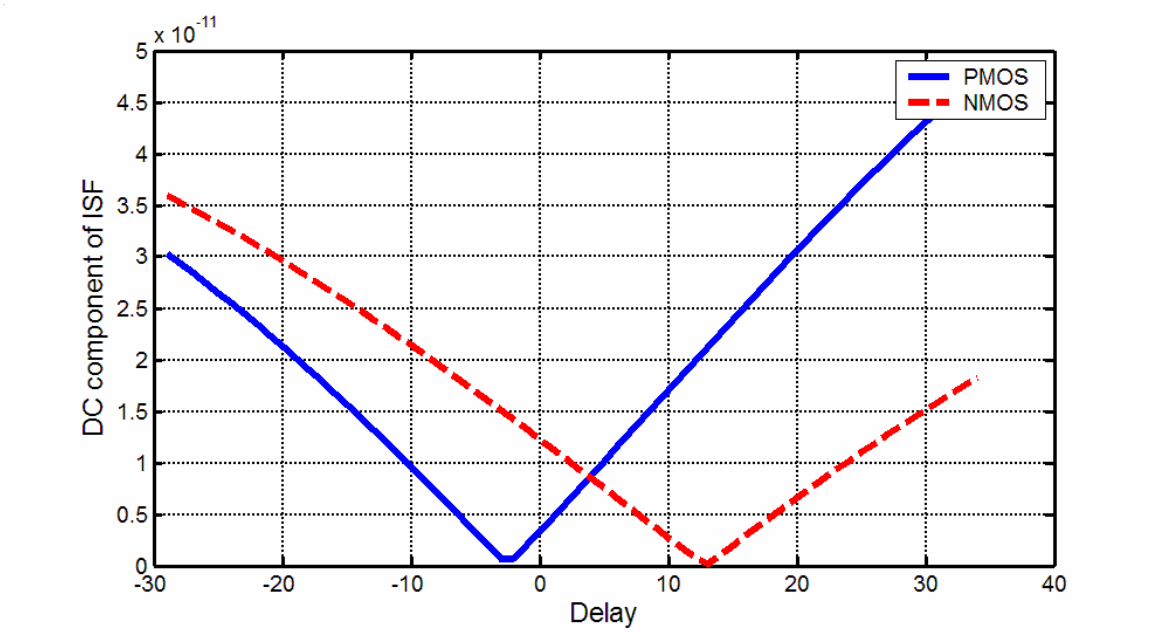

Figure 6.1 Plot of DC components of ISFs versus delay of ISFs.

6.2 Simulation Results of the New VCO Design

This section presents the simulated data for the VCO designed in Section 5.4. First, the ISFs corresponding to all noise sources in the circuit are shown in Figure 6.2. Note that this function is the same for the NMOS and PMOS transistors since both noise sources are connected to AC ground and the same output node. Its DC component is nearly zero as expected. On the other hand, the ISFs of the bias resistors show relatively strong DC components. Fortunately, their noise sources are white and the noise currents are much smaller than those of the active devices. The ISF corresponding to the middle bias resistor R2 contains much smaller DC component because this resistor sees the VCO

as a nearly symmetrical load while the other resistors do not. Nevertheless, the magnitude of the DC components of the other two ISF is nearly the same, indicating nearly optimal design with respect to phase noise contribution of the bias resistors. For the white noise sources of the bias resistors, their phase noise contribution can be readily calculated at this point. However, for the NMOS and PMOS switching transistors, the cyclostationarity of their noise sources requires further analyses to derive the corresponding effective ISFs before the phase noise computation can be performed.

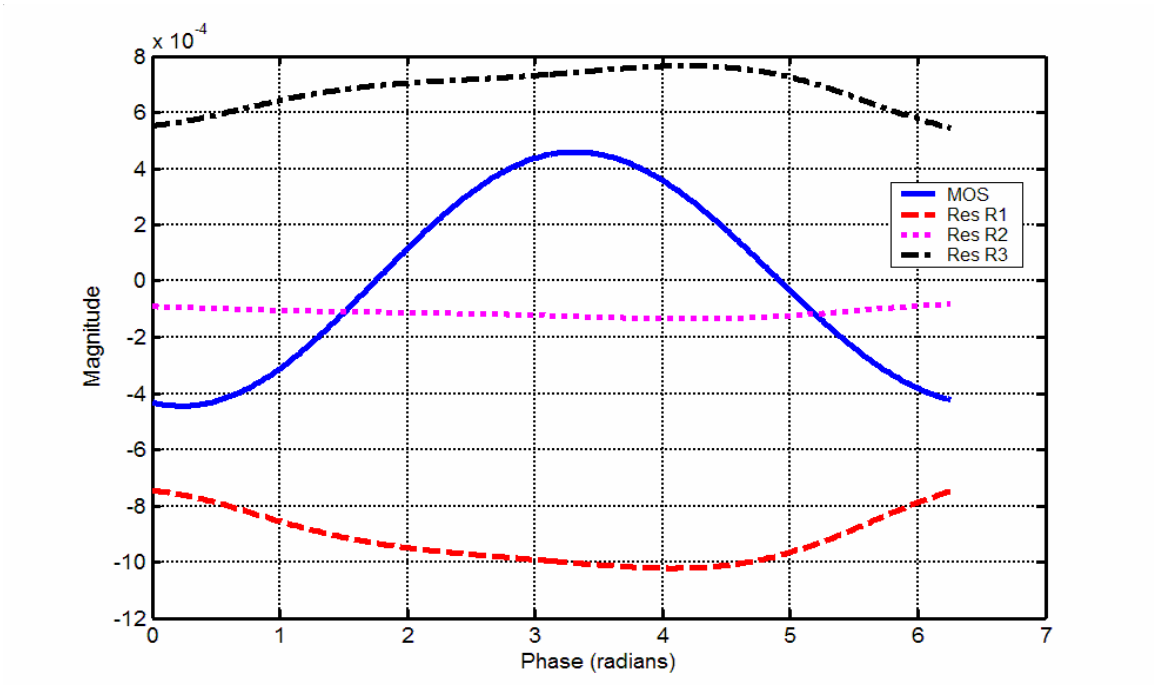

Figure 6.2 ISF of all noise sources in the new VCO circuit.

Next, Figure 6.3 shows one cycle of the drain current of the NMOS and PMOS transistor with respect to the phase of the output signal, or equivalently the phase of the corresponding gate signal. Because of the propagation delay from the gate of the transistor to its drain current, there is significantly more current conduction at one

zero-crossing point than at the adjacent one. This effect must be taken into account in deriving the effective ISF, especially for high-frequency design.

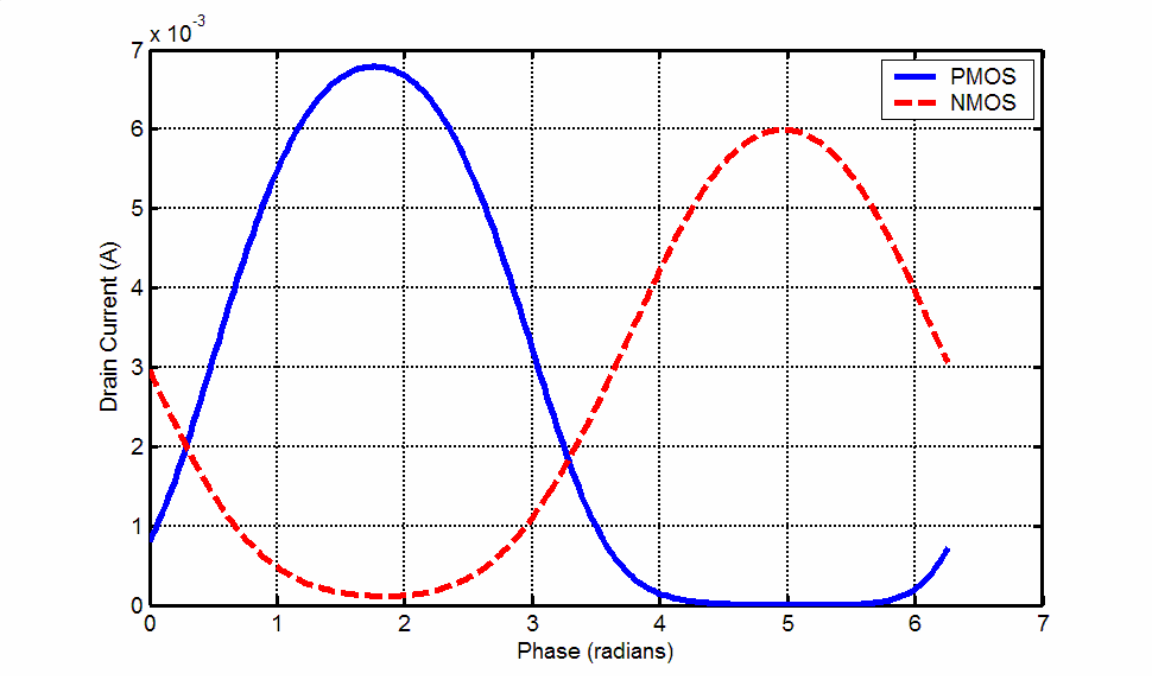

Figure 6.3 One cycle of drain current of the NMOS and PMOS transistor.

Figure 6.4 shows the noise spectral density of the NMOS and PMOS transistors over one oscillation cycle, illustrating the cyclostationary properties of their noise sources. It is obtained by combining the drain currents of Figure 6.3 with the results of noise analyses sweep over a range of DC drain currents. Notice the sharp transition edges of the noise densities near the zero-crossing points (0 and π radians) where the transistors transition between the weak- and strong-inversion regions. It confirms the benefit of choosing as large W/L ratios as possible to keep the transistors operating in the weak-inversion region where the noise densities are much lower than those in the strong-inversion region.

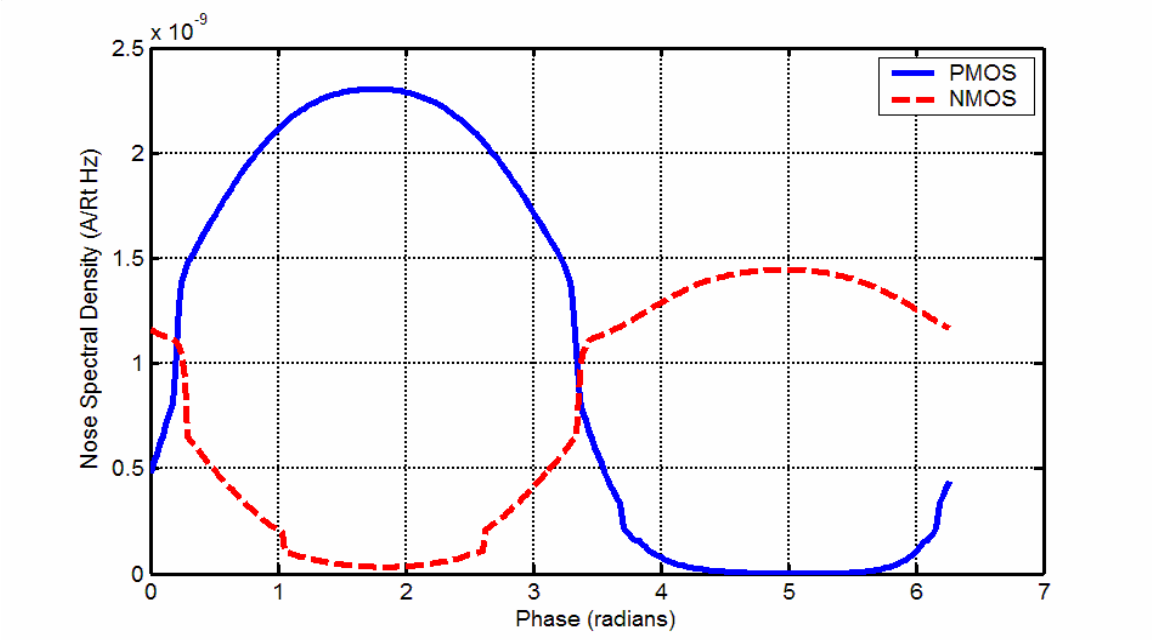

Figure 6.4 Noise spectral density of the PMOS and NMOS transistor for one oscillation cycle.

The effective ISFs are then derived by multiplying the original ISFs (Figure 6.2) with the noise densities of Figure 6.4. This is illustrated by Figure 6.5 for the time domain and by Figure 6.6 for the frequency domain. As expected and can easily be seen, the major noise contributions are from the fundamental and second harmonic components where the noise spectral densities are assumed to be Gaussian. The DC component (corresponding to low-frequency or flicker noise) is significantly suppressed by design to be nearly two order of magnitude less than the largest component. Thus, its phase noise contribution is negligible even though its noise spectral density can be much higher than that of high-frequency Gaussian noise. Note that in Figure 6.6, the plot is drawn continuously for visual clarity only. The functions themselves are discrete with components at integral multiple of the oscillation frequency because the corresponding time-domain functions are periodic.

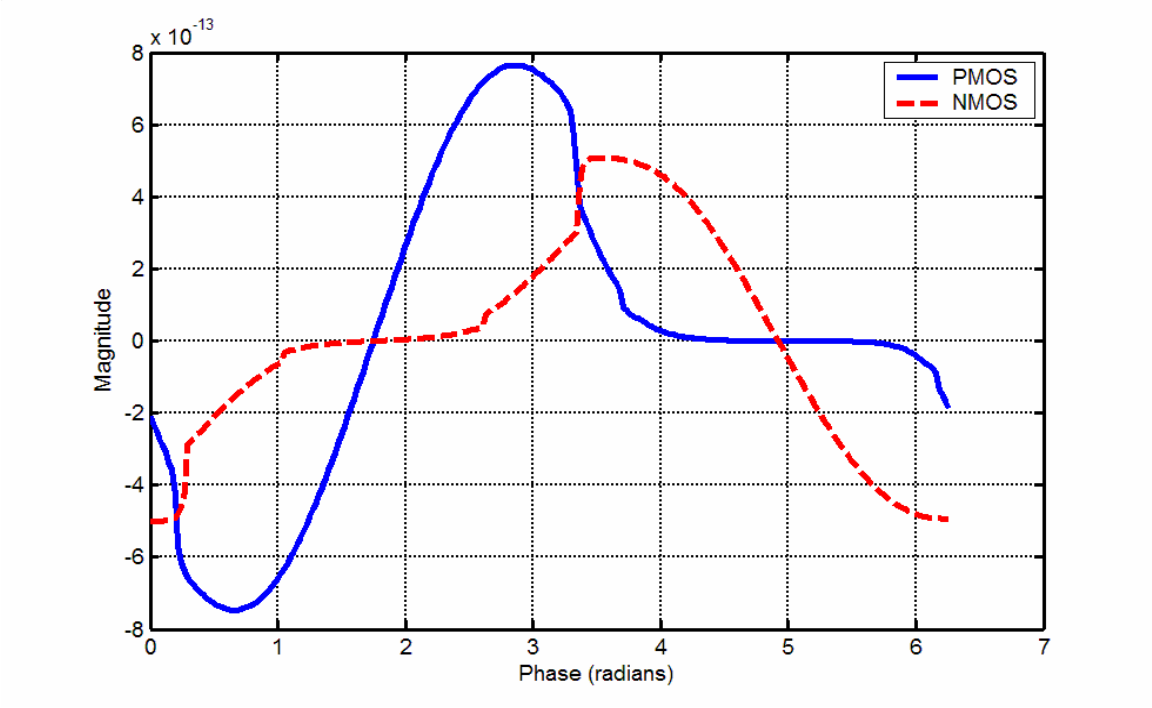

Figure 6.5 Effective ISFs for the NMOS and PMOS transistors in the time domain.

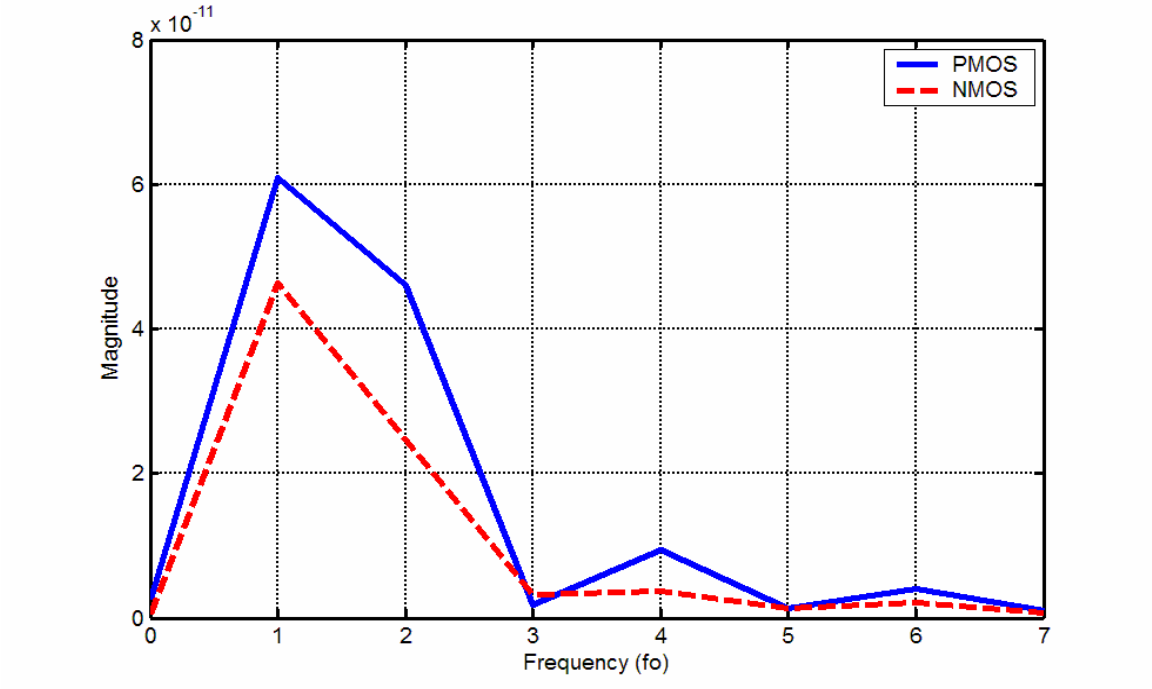

Figure 6.6 The effective ISFs for the NMOS & PMOS transistors in the frequency domain

Using the derived effective ISFs, the phase noise contribution of the NMOS and PMOS switching transistors can be easily calculated as described in Section 6.1. The results are plotted in Figure 6.7 along with the phase noise contributions from the bias resistors. The total phase noise of the VCO is then computed by adding together the individual noise contributions (in the root-mean-squared sense). At 100-KHz and 1-MHz offset frequencies, the VCO phase noise is -94.44 and -114.81 $dBc/\sqrt{Hz}$ respectively, showing no effect of flicker noise contribution. At 10-KHz offset frequency, the phase noise is -72.13 $dBc/\sqrt{Hz}$, about 2 dB higher than expected, resulting from the increasing noise spectral densities at this and lower frequencies. Even though this can be improved in theory by further reducing the DC component of the effective ISFs, it is not practically possible because of the requirement of precision components not available in a typical CMOS process.

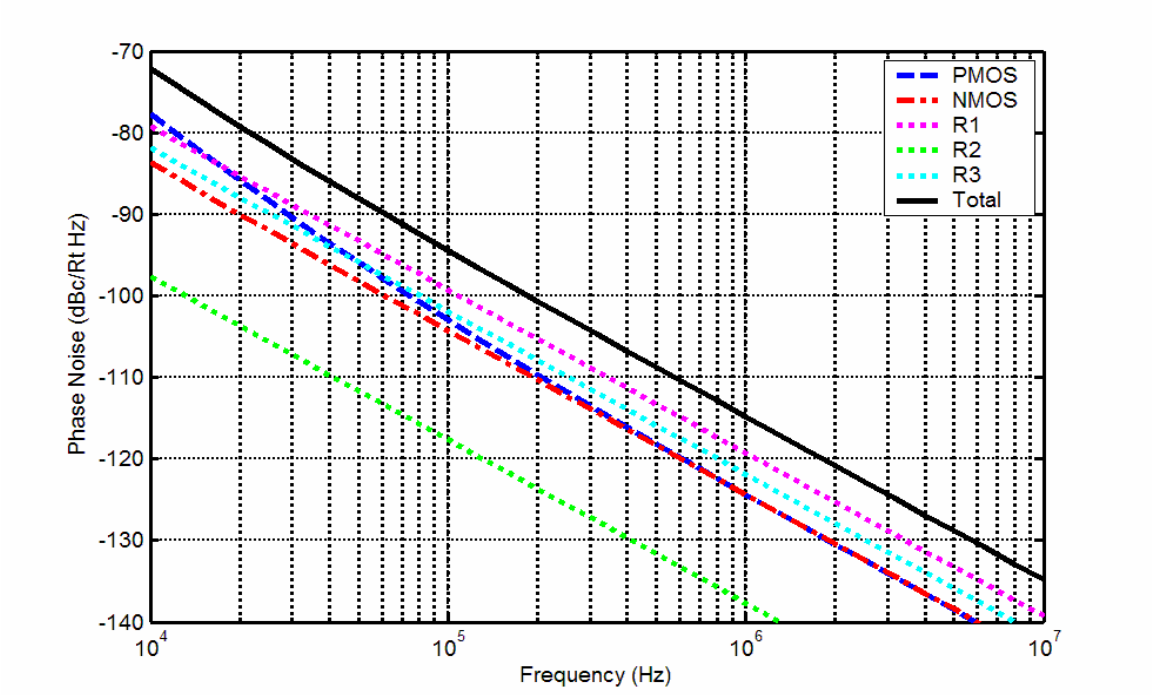

Figure 6.7 Phase noise of the new VCO along with noise contribution from each individual noise source.

6.3 Simulation Result of a Reference VCO Design

To facilitate the evaluation of phase noise improvement of the new VCO design, a reference VCO, using the same tank inductor, is implemented in the same CMOS process. The circuit topology is that of a complementary cross-coupled transconductance VCO. The schematic of the reference VCO is shown in Figure 6.8, and the components values are tabulated in Table 6.1. The reference current is generated with a resistor and a external power supply VDD1, separate from the core power supply VDD, to allow flexibility in selecting the magnitude of the reference current, and therefore, that of the bias current of the VCO. The output buffer circuit is not shown in the schematic of Figure 6.8, but it is the same design as described in Section 5.4.2.

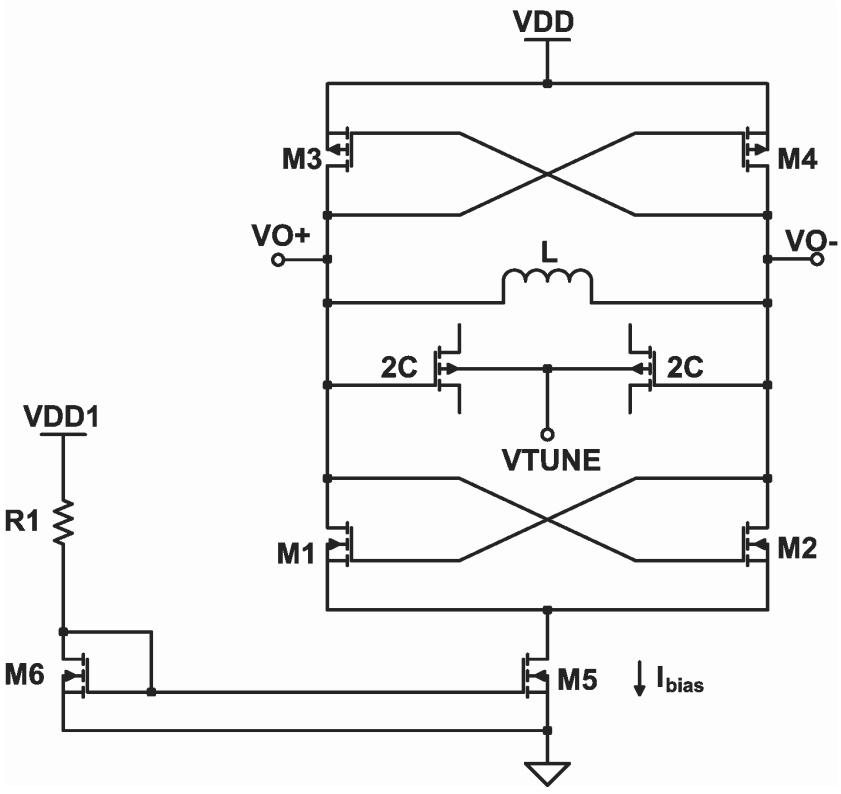

Figure 6.8 Schematic of the Reference VCO Design

Table 6.1 Components values of the reference VCO design.

Component	Value
NMOS switching transistors	1x24x2μm/0.18μm
PMOS switching transistors	1x48x2μm/0.18μm
NMOS bias transistor M5	8x24x2μm/0.74μm
NMOS reference transistor M6	4x24x2μm/0.74μm
Reference resistor R1	700Ω
Reference supply VDD2	1.8V
Core supply VDD	1.8V
Reference current	2mA
Tank capacitance	2.3pF

The same simulation methodology is used to compute the phase noise of the reference VCO. The resulting phase noise, along with the contributions from individual noise sources, is presented in Figure 6.9. At 100-KHz offset frequency, the phase noise is -83.23 $dBc/\sqrt{Hz}$, about 10 dB higher than that of the new VCO.

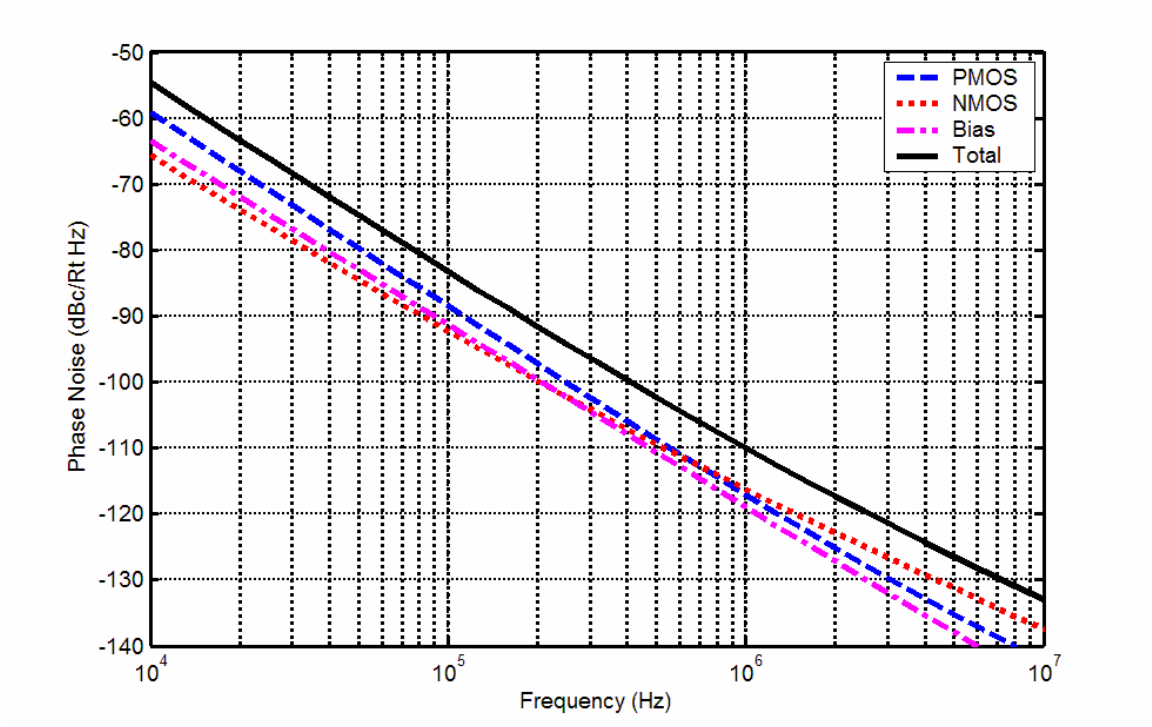

Figure 6.9 Phase noise of the reference VCO along with contribution from each individual noise source.

6.4 Experimental Results

6.4.1 Test Setup

The reference and new VCO designs were laid out and fabricated using National Semiconductor 0.18-µm CMOS9 process. A photograph of the die of each design is shown in Figure 6.10 and Figure 6.11 respectively. The chip was tested using the probing station, an 20Hz-8GHz RF spectrum analyzer (Rohde and Schwarz FSU8), and an 0.3MHz-3GHz RF network analyzer (Hewlett Packard 8714C) as shown in Figure 6.12. During test, the VCO output is connected directly to the FSU8 input via a RF probe, while power supplies and control signals are applied to the chip via a test PCB and a low-frequency DC probe. The schematic and a photo of the test PCB are shown in Figure 6.13 and Figure 6.14 respectively. A tuning input VTUNE is provided on the test PCB for controlling the capacitance of the tank varactor. However, it is not used since the fabricated design uses a capacitance array in place of the varactor. This is to simplify the test procedure and it is because of the lack of an accurate simulation model for the varactor.

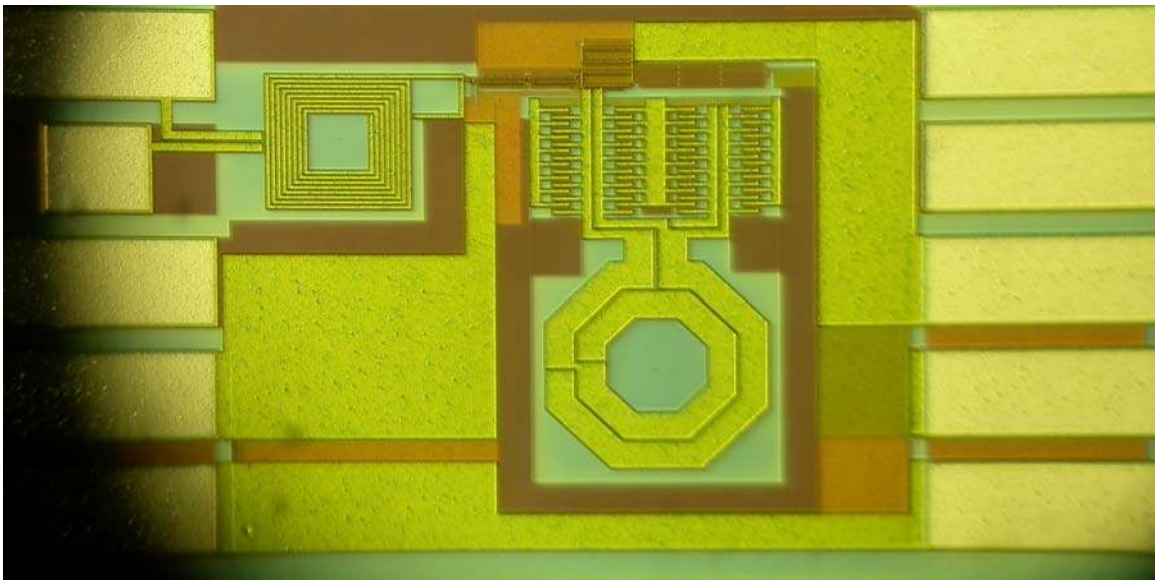

Figure 6.10 Photograph of the fabricated die of the reference VCO.

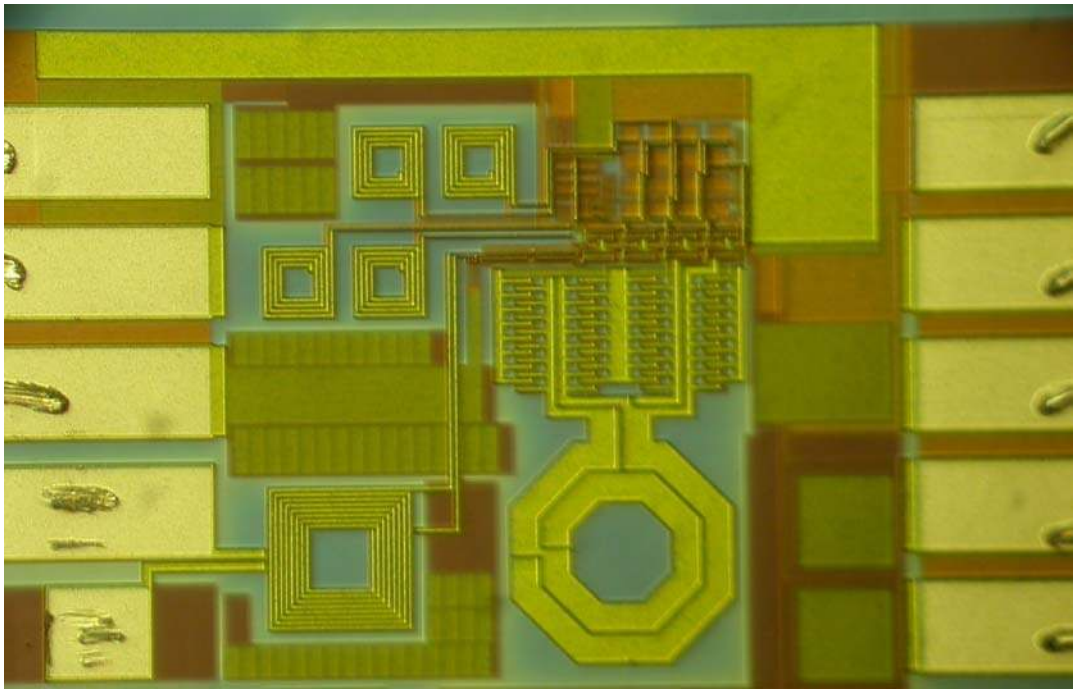

Figure 6.11 Photograph of the fabricated die of the new VCO.

Figure 6.12 Photograph of the probing station and the test instruments.

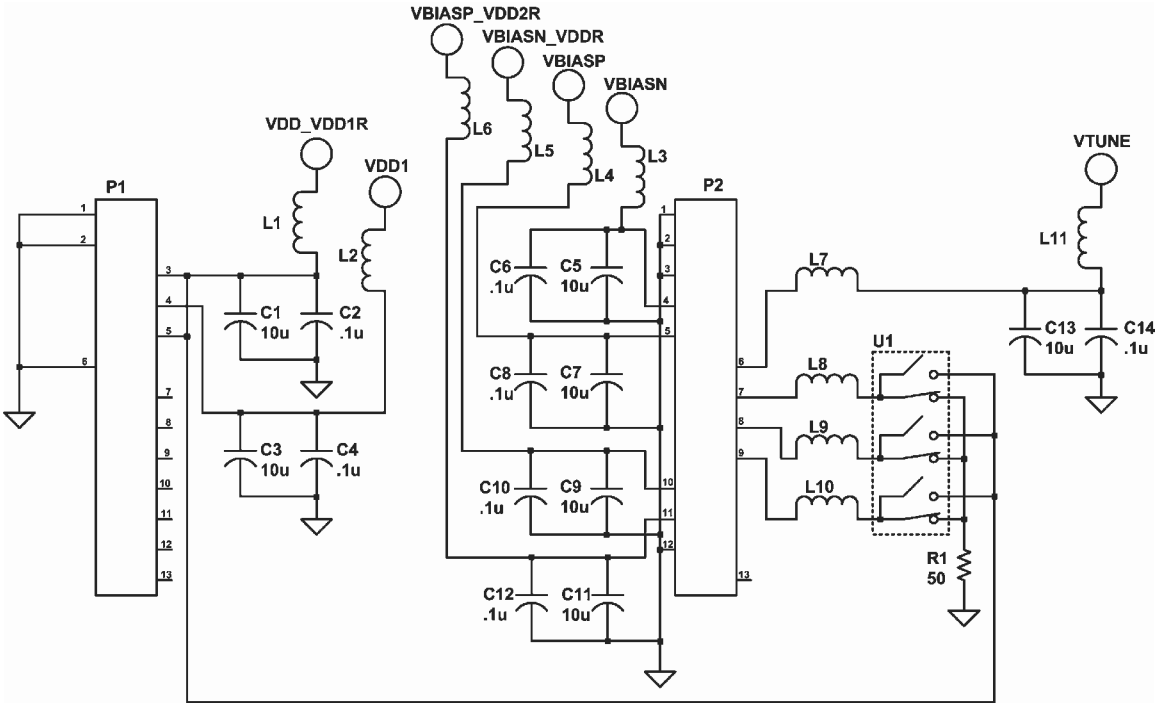

Figure 6.13 Schematic of the test PCB.

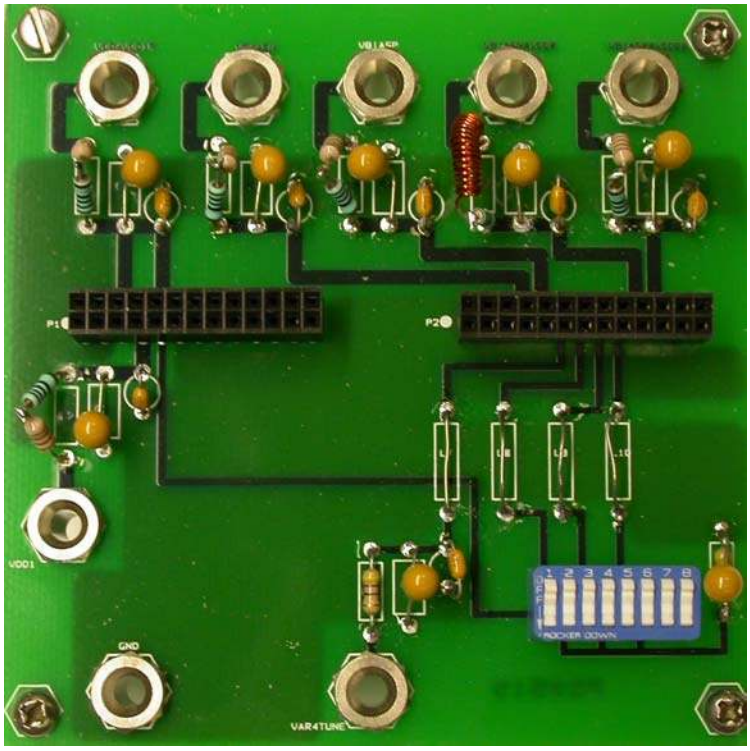

Figure 6.14 Photograph of the test PCB.

6.4.2 Test of the Output Balun

A stand-alone 8:1 output transformer, as described in Section 5.4.2, was implemented on the fabricated chip to verify its predicted performance. A similarly-designed 1:1 transformer was also included for comparison. This was done to insure that any discrepancy between predicted and measured losses through the 8:1 transformer was not mainly because of the large turn ratio. The RF network analyzer (HP 8714C) was used to provide the input to the device under test (DUT), and to measure the resulting output. The power gain of each transformer was measured, and the circuit of Figure 6.15 was used to analyze and approximate the corresponding coupling coefficient. The resulting data are summarized in Table 6.2, along with the design parameters. They indicate that both devices have about 7 dB more power loss than predicted by ASITIC, which is not a surprising result since substrate loss at high frequencies can be significant. However, it is not a problem with respect to the phase noise measurement of the VCO since both signal and noise are equally attenuated.

Table 6.2 Summary of measured data for the output transformer.

Parameters	**8:1 Transformer**			**1:1 Transformer**		
	Primary	**Second.**	**Measured**	**Primary**	**Second.**	**Measured**
Shape	Square	Square		Square	Square	
Outer dimension	120 μm	120 μm		100 μm	100 μm	
No. of layers	1 (met5)	1 (met4)		1 (met5)	1 (met4)	
No. of turns	8	1		5	5	
Trace width	4 μm	24 μm		6 μm	6 μm	
Trace spacing	0.4 μm	0.8 μm		0.4 μm	0.4 μm	
Power gain @1GHz			-20.1 dB			-9.5 dB
Power gain @3GHz			-20.7 dB			-7.6 dB
Coupling coefficient @3GHz	0.894 (ASITIC)		0.375	0.933 (ASITIC)		0.417

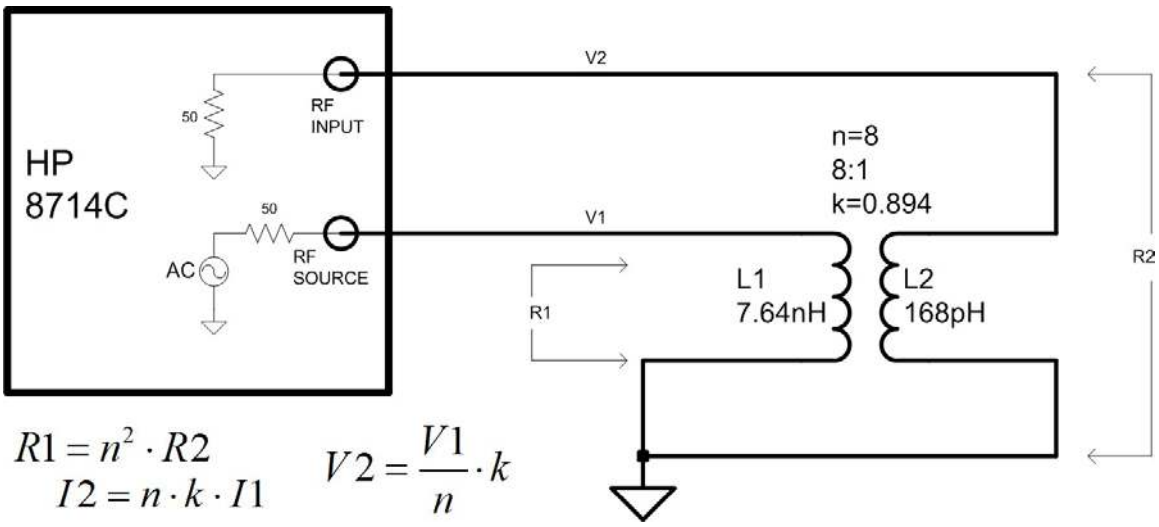

Figure 6.15 Test setup for the stand-alone output transformer.

6.4.3 Test of the Tank Inductor

The test circuit of Figure 6.16 was used to estimate the quality factor and inductance of the tank inductor. This approach avoids the complexity of measuring the S-parameters of the device at the expense of some accuracy. By sweeping the input source frequency, the resonance frequency (f_r) and the 3-dB bandwidth ($BW = f_2 - f_1$) of the resonator can be found. The quality factor and inductance can then be derived as shown below.

$$Q = \frac{f_r}{f_2 - f_1} \tag{6.1}$$

$$R_P = \frac{0.447 \cdot 50}{V_{O(f_r)}} - 100$$

$$L = \frac{R_P}{\omega \cdot Q} \tag{6.2}$$

It is important to note that the 3-dB frequencies (f_1 , f_2) are not those at which the output is 3 dB above the resonant minimum of the test circuit. They are rather the frequencies at which the impedance of the resonator is 3 dB below the parallel equivalent resistance R_P . The results, summarized in Table 6.3, are relatively consistent with simulated data by ASITIC. The difference may be attributed to the underestimation of the substrate loss of the device.

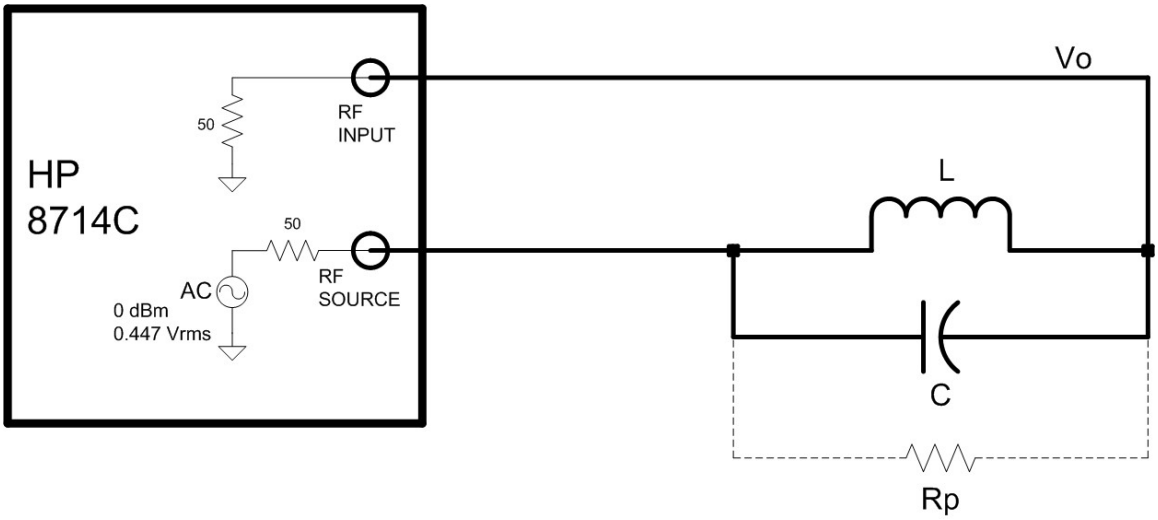

Figure 6.16 Test circuit to characterize tank inductor.

Table 6.3 Summary of measured data for the tank inductor test.

Parameters	Simulated	Measured
Resonant frequency f_r	The test circuit was not simulated since the Q and inductance are already known from ASITIC analysis, as shown below	1855.9867 MHz
3-dB frequency f_1		1722.0167 MHz
3-dB frequency f_2		1997.9533 MHz
$V_O(f_r)$		-4.172 dBm
$V_O(f_1)$		-3.229 dBm
$V_O(f_2)$		-3.225 dBm
R_P		61.7 Ω
Quality factor Q	7.9 @5.5 GHz	6.7 @1.855GHz
Inductance	0.552 nH	0.786 nH

6.4.4 Test of the VCOs

The reference VCO was tested by setting the core supply voltage VDD and the output buffer supply voltage VDD1 to 1.8V. On the other hand, the reference supply voltage VDD2 was adjusted to 2.7V to achieve the desired reference current of 2mA. It is because the on-chip reference resistance R1 is greater than the designed nominal value of 700Ω. The reference-VCO output phase noise was then measured and recorded as shown in Figure 6.17. An average of 32 sweeps was used to smooth out random noise variations. The resolution bandwidth (RBW) of 30 KHz was used to minimize leakage of carrier energy into the phase noise sidebands. Lower RBW is desired but not possible because the carrier frequency jitter causes the average operation to yield inaccurate measurements.

As shown in the figure, the oscillation frequency was measured to be about 5.191 GHz. Although the tank capacitance array can be trimmed with the built-in laser of the probe station to obtain the desired frequency of 5.5 GHz, repeated use of the laser tends to degrade the performance of the nearby active devices. Therefore, to get the most accurate phase noise measurements possible, laser trimming was not used and the oscillation frequency was left unchanged.

The carrier signal amplitude was measured to be about -30dBm at the output of the 8:1 transformer balun. Taking into account the 20-dB loss of this device, the carrier signal at the output buffer is about -10dBm, or approximately 620mV peak-to-peak, which is consistent with the simulated results. At 100-KHz and 1-MHz offset frequency, the phase noise was measured to be -78.45 dBc/Hz and -107.82 dBc/Hz respectively, which is about 3 to 5 dB worse than the simulated results. The difference may be attributed to the lower

actual quality factor of the inductor and to the measurement error because of carrier energy leakage at low offset frequencies.

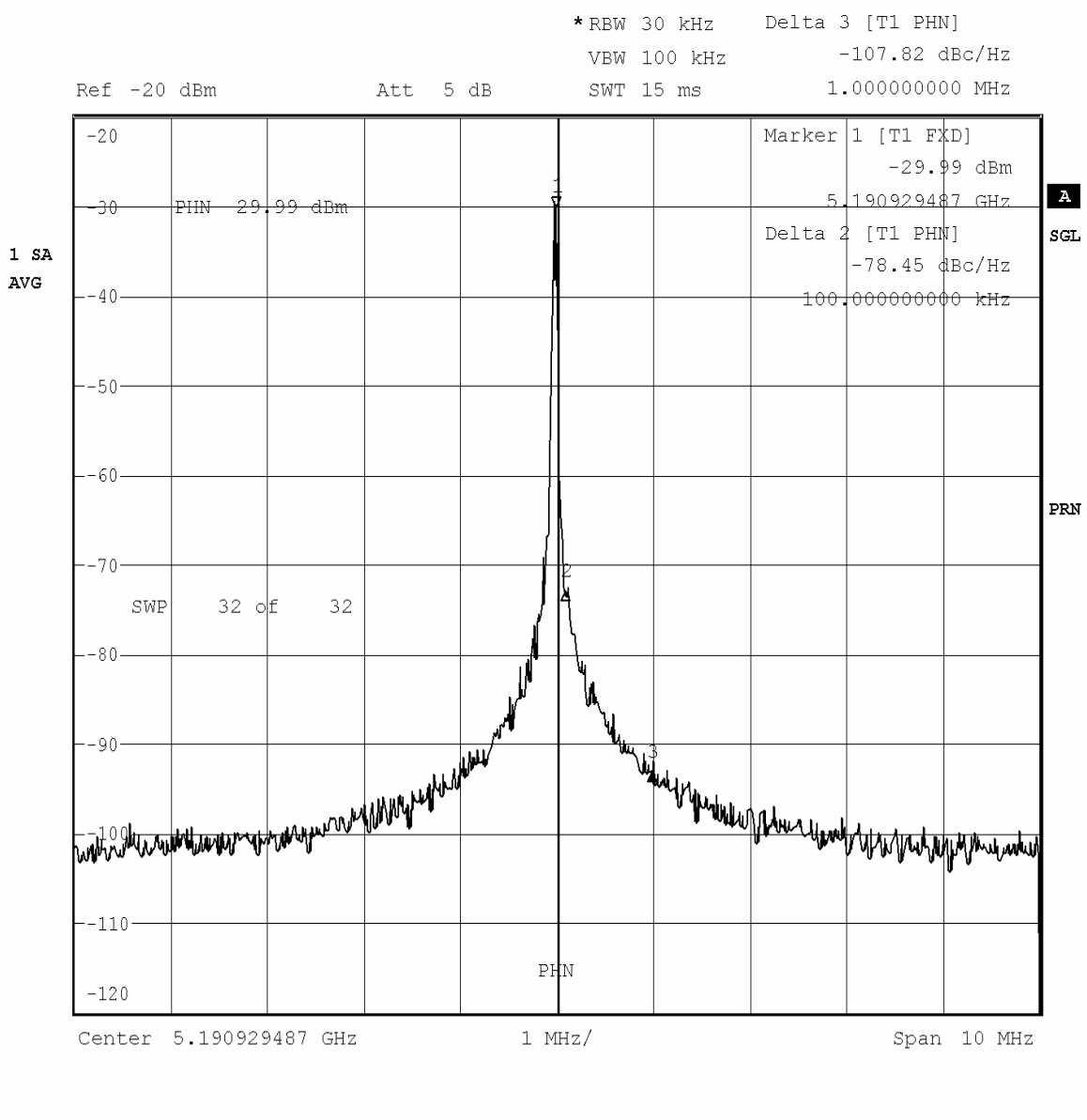

Figure 6.17 Output phase noise of the reference VCO.

Similarly, the new VCO was tested by setting the core supply voltage VDD and the output buffer supply voltage VDD1 to 1.8V. The tuning voltage VBIASP and VBIASN was initially set at the nominal values of 1.8V and 0V respectively. Note that the use of these voltages for tuning is to facilitate the testing/debugging process. For a practical design, these voltages are to be fixed at VDD and GND and the bias voltages are tuned by switching a resistor array appropriately. The un-tuned new VCO phase noise was measured and recorded as shown in Figure 6.18. As before, an average of 32 sweeps was used to smooth out noisy fluctuation, and the selected RBW is 30 KHz to optimize phase noise measurement accuracy.

The oscillation frequency was measured to be about 4.441 GHz. For best comparison of phase noise performance between the two VCO, the oscillation frequencies should be trimmed to be the same. However, as mentioned before, since the laser trimming tended to degrade the nearby active devices and the frequency difference is not significant in terms of phase noise performance, the oscillation frequencies were left unchanged. The measured carrier signal amplitude was -27.15 dBm, about 3 dB higher than that of the reference VCO, which is consistent with simulated results. The measured phase noise was -78.60 dBc/Hz and -108.74 dBc/Hz at 100-KHz and 1-MHz offset frequency respectively, which was essentially the same as that of the reference VCO. It was not unexpected since because of component tolerance, the new VCO with the nominal bias voltages could not cancel out the DC component of the switching transistors' ISF and low-frequency flicker noise had a significant effect on the phase noise performance.

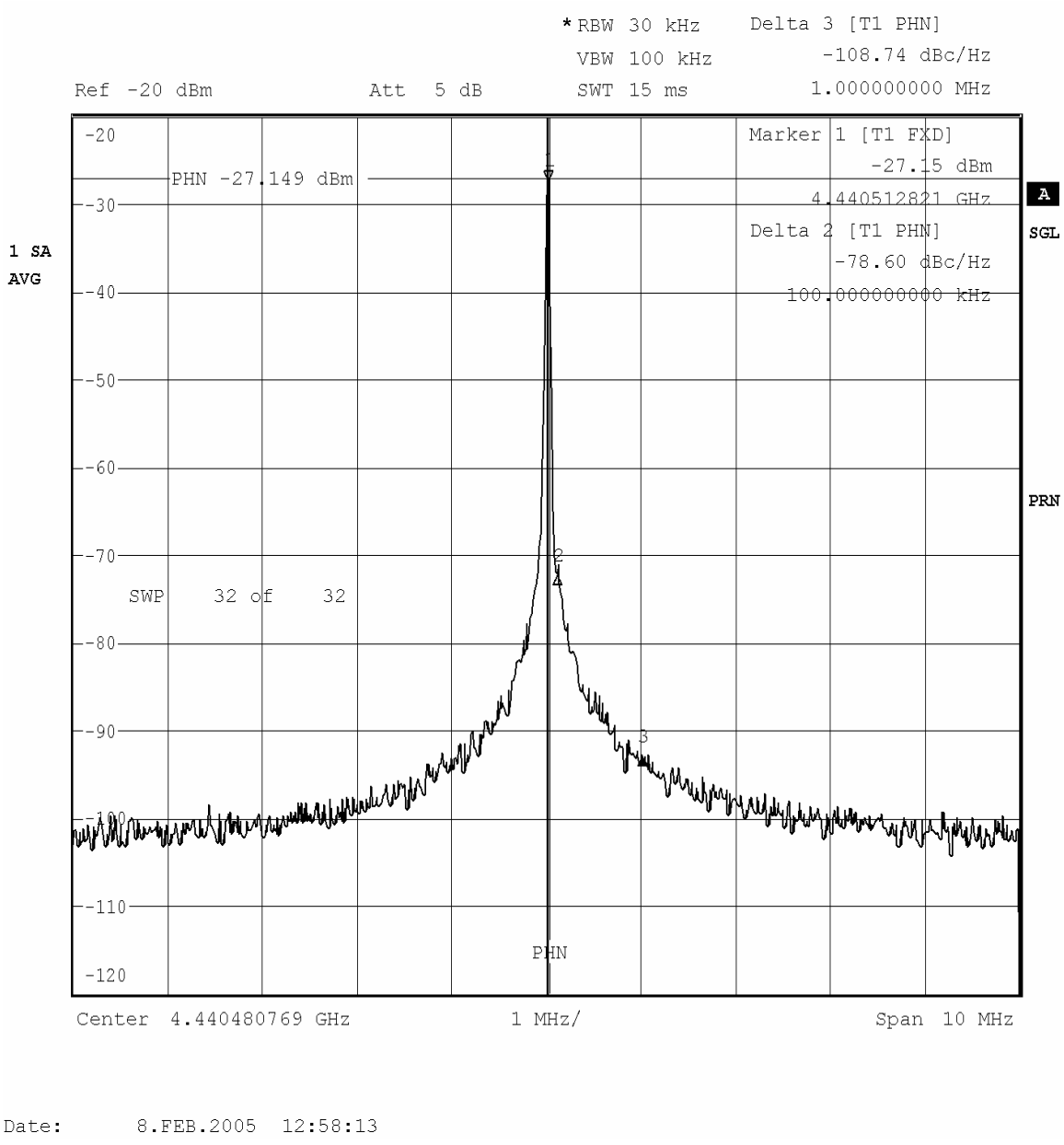

Figure 6.18 Output phase noise of the un-tuned new VCO.

The tuning circuit as described in Section 5.4.4 was included in the design of the new VCO, and were intended to help in the tuning process. The voltages VBIASP and VBIASN were to be adjusted such that the VCO output DC voltage was the same as the DC reference voltage. Unfortunately, an unexpected problem occurred in the layout of the tuning circuit causing the DC reference voltage to be at the transistor saturation voltage and did not reflect the proper value for optimal VCO output DC voltage. For optimal matching, the resistor R5 of Figure 5.16 were laid out as four parallel elements, each with minimum width of 180nm to minimize area consumption. This layout approach, however, caused the actual resistance to be much higher than the nominal value. Measurement of resistors with similar layout techniques showed resistance to be as much as 100% higher than the designed value. The reason is because the over-etching of the polysilicon layer becomes significant for a minimum-width device, and therefore substantially increases its actual resistance. As a result, the tuning had to be performed in an essentially random pattern, making it quite difficult to achieve good cancellation of the DC components of the transistors' ISF. Nevertheless, with the voltages VBIASP and VBIASN set at 1.59V and 0.16V respectively, the best phase noise improvement was observed and recorded as shown in Figure 6.19. At 100-KHz offset frequency, the phase noise was -85.17 dBc/Hz, an improvement of about 6dB over the un-tuned circuit. At 1-MHz offset frequency, the phase noise was -109.87 dBc/Hz, essentially no improvement over the un-tuned circuit which was expected since there was little flicker noise present at this and higher frequencies.

Table 6.2 summarizes the measured results presented in this section, plus additional measured data, and comparison with other state-of-the-art designs found in the literature.

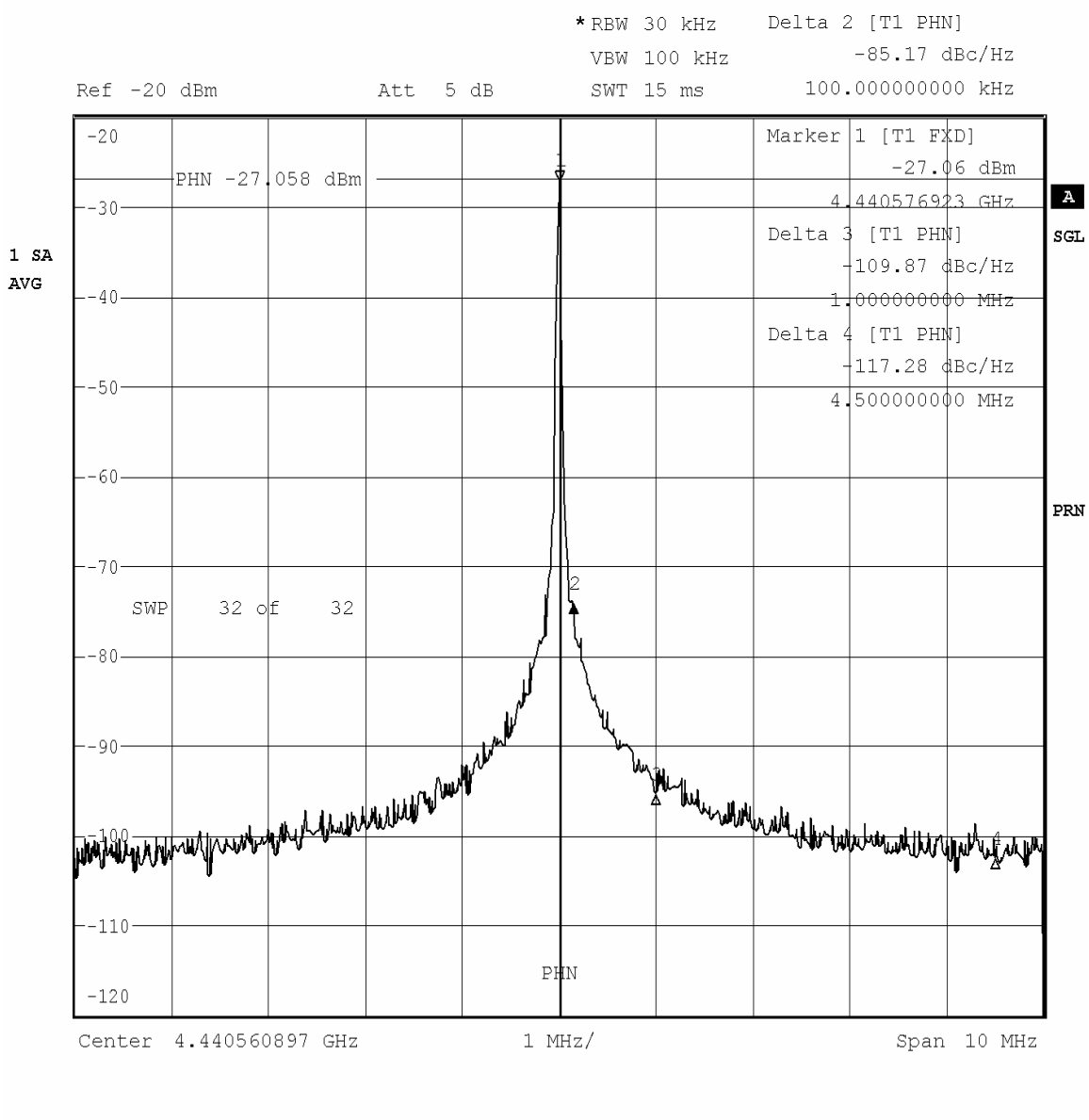

Figure 6.19 Output phase noise of the tuned new VCO with VBIASP=1.59V and VBIASN=0.16V.

Table 6.4 Summary of simulated and measured results and comparison with other designs in the literature.

Design	Phase Noise (dBc/Hz)		Osc Freq (GHz)	Power (mW)
	100KHz	1MHz		
Ref VCO (simulated) 0.18μm CMOS	-83.23	-110.02	5.5	10.8
Ref VCO #1	-78.45	-107.82	5.1	10.8
Ref VCO #2	-79.10	-108.01	5.1	10.8
Ref VCO #3	-79.06	-108.54	5.1	10.8
New VCO (simulated) 0.18μm CMOS	-94.44	-114.81	5.5	13.5
New VCO #1	-85.17	-109.87	4.4	14.4
New VCO #2	-84.80	-109.40	4.4	14.4
New VCO #3	-84.93	-109.17	4.4	14.4
[23] Ref VCO	-81.0 @10KHz	-126.0 @600KHz	5.5	2.8
[23] Proposed VCO 0.25μm SiGe 6 HP	-87.0 @10KHz	-127.6 @600KHz	1.88	2.8
[77] (simulated) 0.25μm CMOS	-93.00		5.5	10
[27] Ref VCO	-100.0	-130.0	1.54	16.2
[27] Proposed VCO 0.35μm Jazz BC35M	-110.0	-130.0	1.54	16.2

As indicated in the above table, the simulated phase noise of this work and that of [77] are quite similar, a result of the process used for the design being almost the same (0.25μm CMOS/0.18μm CMOS). On the other hand, the phase noise of the VCO in [23] is better than that of this work. However, the reference VCO in [23], which has the same topology as the reference VCO of this work, also has better phase noise, pointing to the fact that the difference in performance may be because a better process is used in the fabrication of the design of [23]. Additionally, the reported power consumption is quite low, meaning that either the tank inductor has very high quality factor or the design is

under-biased which tends to favor phase noise performance at the expense of practical output voltage. Similarly, the work of [27] shows the best phase noise performance, but the corresponding reference VCO also exhibits low phase noise, indicating that the process is probably better than that used in this work. At 100-KHz offset frequency, the reduction of phase noise is 10 dB, about the same gain as that in this work. However, at lower offset frequencies (less than 10 KHz as shown in Figure 6.20), the effect of flicker noise becomes dominant again, whereas this is not the case for the proposed VCO when it is properly tuned.

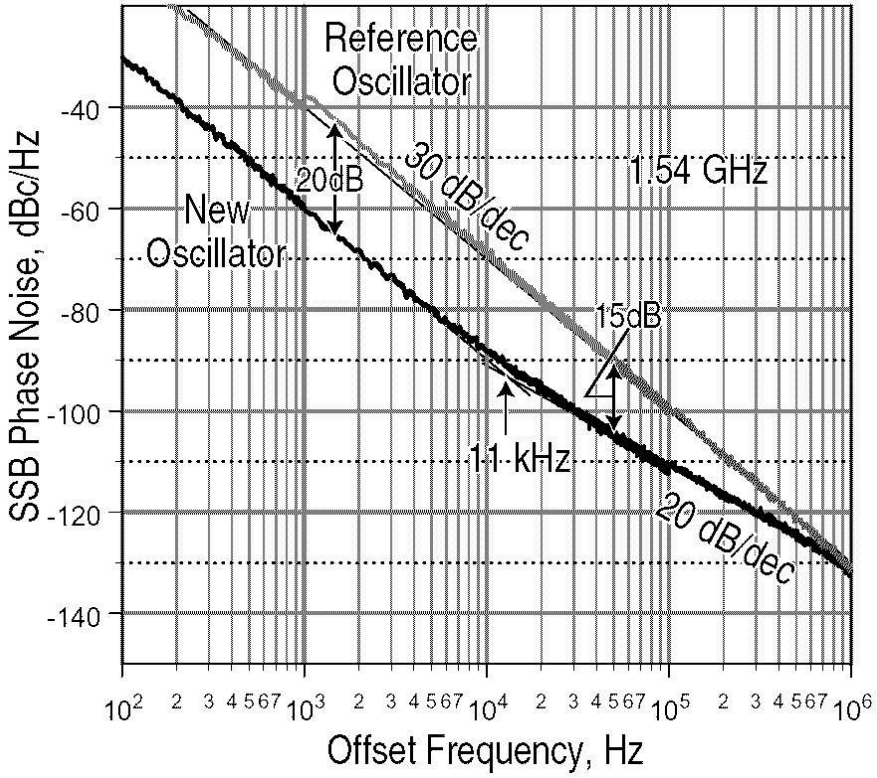

Figure 6.20 Measured phase noise of VCO in [27].

CHAPTER 7
CONCLUSIONS

7.1 Low-Phase-Noise CMOS VCO

A low-phase-noise CMOS VCO circuit was implemented to demonstrate a design technique that eliminates the effect of low-frequency flicker noise on the VCO phase noise. This is accomplished by biasing the circuit such that the DC component of the switching transistors' ISF is eliminated, resulting in the low-frequency noise not being up-converted into phase noise. A reference VCO, using a conventional complementary cross-coupled transconductance topology, was also implemented for performance comparison with the new VCO. The reference VCO phase noise was measured to be about -78 dBc/Hz at 100-KHz offset frequency, which was about 5 dB worse than the predicted value by simulation. The new VCO phase noise, when not properly biased, was found to be similar. After tuning, the phase noise of the new VCO was measured to be about -85 dBc/Hz, showing an improvement of about 6dB. The measured phase noise at 1-MHz offset frequency, which contained little or no contribution from flicker noise, was -109 dBc/Hz. Therefore, the best achievable phase noise at 100-KHz offset frequency was -89 dBc/Hz (4 dB lower than what was actually measured), indicating the tuned new VCO was nearly at the optimal bias condition. This optimal condition was not achieved because the tuning circuit did not function properly, but could easily be corrected in the next iteration.

7.2 Summary of Contributions

The contributions of this research include:

1. A new VCO circuit topology that allows the cancellation of low-frequency flicker noise effect on the VCO phase noise. The proposed circuit allows the designer to select the transistor sizes, the feedback ratios, and the bias voltages such that the effective ISF corresponding to the transistors' noise source has no DC component, thus preventing the upconversion of flicker noise into phase noise.
2. A step-by-step design algorithm is presented to help the designer achieve optimal design in a simple straightforward fashion.
3. A simulation methodology is also presented that helps in the previously mentioned design algorithm. A MATLAB script is included to help in the computation of the ISF and the oscillator phase noise.

7.3 Future Works

The problem discovered with the tuning circuit must be corrected. This can be done by using non-minimal width for the resistor layout. An alternative is to use source-follower circuits in place of the inverting amplifiers, thus eliminating the circuit sensitivity to passive components. A properly working tuning circuit will allow the optimal biasing of the switching transistor to be achieved more easily.

Additionally, in order to measure the VCO phase noise at low offset frequency more accurately, a phase-lock loop circuit may be necessary to reduce or eliminate the oscillation frequency jitter.

APPENDIX A
IMPEDANCE OF PARALLEL RLC TANK

The following will show the derivation for the approximate impedance of the parallel RLC tank at a frequency $(\omega_0 + \Delta\omega)$, where R_P is the resistance, L is the inductance, C is the capacitance, $\omega_0 = 1/\sqrt{LC}$ is the resonant frequency, $Q_L = R_P/\omega_0 L$ is the load Q of the tank, and $\Delta\omega << \omega_0$ is the offset frequency away from ω_0.

$$Z_{R_PLC}(\omega_0 + \Delta\omega) = R_P // j(\omega_0 + \Delta\omega)L // \frac{1}{j(\omega_0 + \Delta\omega)C} = R_P // \frac{j(\omega_0 + \Delta\omega)L}{-(\omega_0 + \Delta\omega)^2 LC + 1}$$

Replacing LC with $1/\omega_0^2$, L with $R_P/Q_L\omega_0$, and simplifying the above expression (ignoring the term containing $\Delta\omega^2$) to obtain:

$$Z_{R_PLC}(\omega_0 + \Delta\omega) = R_P // \frac{j(\omega_0 + \Delta\omega)R_P/Q_L\omega_0}{-(\omega_0^2 + \Delta\omega^2 + 2\omega_0\Delta\omega)/\omega_0^2 + 1} \cong R_P // \frac{(\omega_0 + \Delta\omega)R_P}{j2Q_L\Delta\omega}$$

$$= \frac{\frac{(\omega_0 + \Delta\omega)R_P}{j2Q_L\Delta\omega} \cdot R_P}{\frac{(\omega_0 + \Delta\omega)R_P}{j2Q_L\Delta\omega} + R_P} = \frac{(\omega_0 + \Delta\omega)R_P^2}{(\omega_0 + \Delta\omega)R_P + j2Q_L\Delta\omega R_P} = \frac{R_P}{1 + j2Q_L\frac{\Delta\omega}{\omega_0 + \Delta\omega}}$$

Finally, ignoring $\Delta\omega$ in $(\omega_0 + \Delta\omega)$ to get the desired result:

$$Z_{R_PLC}(\omega_0 + \Delta\omega) \cong \frac{R_P}{1 + j2Q_L\frac{\Delta\omega}{\omega_0}} \qquad \text{(A.1)}$$

APPENDIX B
CROSS-COUPLED TRANSCONDUCTOR INPUT RESISTANCE

The input resistance of a cross-coupled transconductor (Figure B.1) is derived as follows:

$$v_{in} = v_{gs2} - v_{gs1} = \frac{i_{d2}}{g_{m2}} - \frac{i_{d1}}{g_{m1}} \tag{B.1}$$

$$i_{in} = i_{d1} = -i_{d2} \tag{B.2}$$

Substitute (B.2) into (B.1), and assume $g_{m1} = g_{m2} = g_m$ to get

$$v_{in} = -\frac{i_{in}}{g_{m2}} - \frac{i_{in}}{g_{m1}} = -\frac{2 \cdot i_{in}}{g_m}$$

$$r_{in} = \frac{v_{in}}{i_{in}} = -\frac{2}{g_m} \tag{B.3}$$

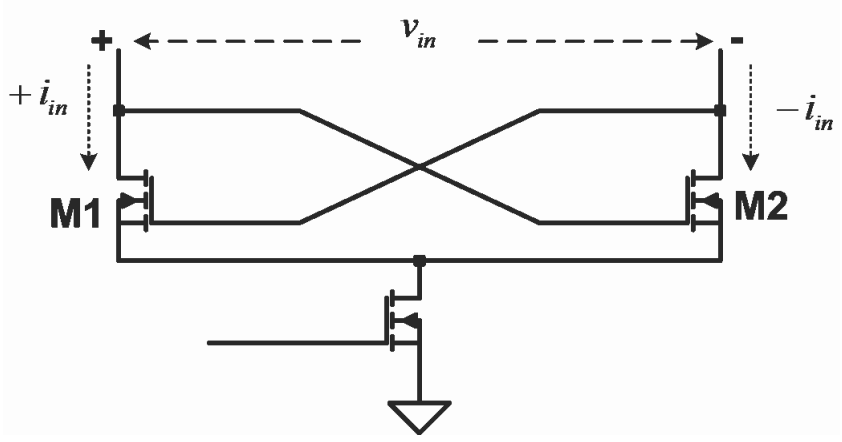

Figure B.1 Schematic of cross-coupled transconductor.

APPENDIX C
DERIVATION OF K' AND V_T BY SIMULATION

The transconductance parameter and threshold voltage of an NMOSFET can be derived with the test circuit shown in Figure C.1. A similar test can be performed for the PMOSFET. This test is designed to place the transistor under the same (or as similar as possible) operating condition as in the actual VCO circuit to get the most accurate results. The length of the transistor should be the same as that in the actual circuit, but its width can be chosen to be any nominal value (W/L≈100 is a good choice). Under the assumptions of the design procedure (section 5.3) and at the peak of the output waveform, the drain-source voltage of the transistor is described in Equation C.1. Its gate-source voltage is shown in Equation C.2.

$$V_{DStest} = \frac{V_{DD} - V_{Opp}}{2} = \frac{V_{DD} - 2/3 \cdot V_{DD}}{2} = \frac{V_{DD}}{6} \tag{C.1}$$

$$V_{GStest} = V_{FBpp} = 2/3 \cdot V_{Opp} = 4/9 \cdot V_{DD} \tag{C.2}$$

A DC analysis is then performed by sweeping the gate-source voltage in the vicinity of V_{GStest}, and the corresponding drain currents are recorded. For any two sets of data points, we have

$$I_{D1} = K' \frac{W}{L}\left[\left(V_{GS1} - V_T\right) - \frac{V_{DStest}}{2}\right]V_{DStest} \tag{C.3}$$

$$I_{D2} = K' \frac{W}{L}\left[\left(V_{GS2} - V_T\right) - \frac{V_{DStest}}{2}\right]V_{DStest} \tag{C.4}$$

Dividing (C.2) by (C.3), we have one equation with one unknown from which the threshold voltage can be derived.

$$\frac{(V_{GS1}-V_T)-V_{DStest}/2}{(V_{GS2}-V_T)-V_{DStest}/2}=\frac{I_{D1}}{I_{D2}}$$

$$V_T=\frac{I_{D1}/I_{D2}\cdot V_{GS2}-V_{GS1}-(I_{D1}/I_{D2}-1)\cdot V_{DStest}/2}{I_{D1}/I_{D2}-1} \tag{C.5}$$

Substituting (C.5) into (C.3), we can compute the transconductance parameter.

$$K'=\frac{I_{D1}}{W/L\left[(V_{GS1}-V_T)-V_{DStest}/2\right]V_{DStest}} \tag{C.6}$$

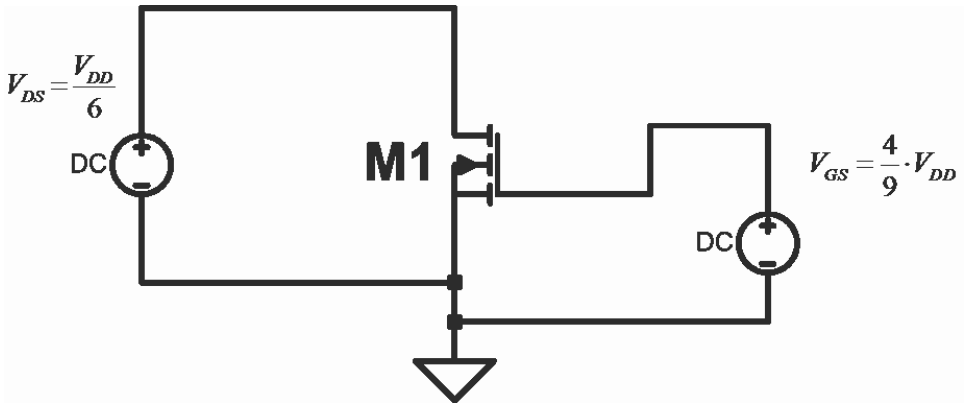

Figure C.1 Schematic of test circuit to derive transconductance parameter and threshold voltage of an NMOS transistor.

APPENDIX D
TRANSISTOR NOISE CHARACTERIZATION TEST CIRCUIT

Figure D.1 shows the schematic of a test circuit that can be used to characterize the noise density of an NMOSFET operating in a similar condition as in the actual VCO circuit, whose simulation results are to be used to compute the phase noise of the oscillator. The noise characterization for the PMOSFET can be performed with a similar test circuit. The gate of the device is driven by a DC source (V3) and an AC source (V4), representing the DC and AC component of the feedback signal for the NMOS transistor in the VCO circuit respectively. Similarly, the drain of the device is driven by a DC source (V1) representing the DC component of the drain signal in the VCO circuit (i.e. the output signal), in series with an AC source (V2) representing the AC component. However, the AC source V2 is a voltage-controlled voltage source dependent on V4 by a factor equal to the voltage gain of the transistor. In this way, the terminal voltages are maintained correctly when voltage source V4 is varied in a analysis. The value of these voltage sources is readily available from a transient simulation of the VCO circuit.

To characterize the noise density, two simulations are performed. One is executed over a range of frequency with the gate and drain voltages constant, while the other is run at a single frequency with the gate voltage being swept between the peaks of the feedback signal. When the results of these two analyses are combined, the noise spectral density of the transistor can be obtained for any frequency and gate voltage within the range of interest.

This test circuit is also used to estimate the propagation delay of the transistor. A transient analysis for one cycle of oscillation, but at a much lower frequency (10MHz), such that the parasitic currents at the drain of the device are negligible, thus the drain current can be accurately recorded. The delay can then be estimated by visually inspecting the drain current waveform, but this can be time-consuming and monotonous. Better yet, software can be written to compute the delay by comparing the drain current waveform with the DC drain current response to a sweep of one cycle of the gate voltage. A MATLAB script is written for this computation and is shown in Figure D.2.

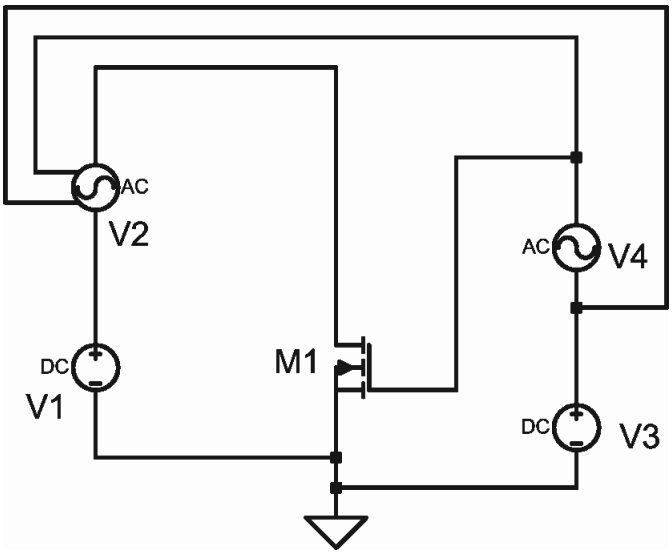

Figure D.1 Schematic of test circuit for noise characterization of NMOSFET.

```
clear
nspline = 8;              % Number of samples used for interpolation.

    fn       = input('Enter peak gate-source voltage: ','s');
    vgpk     = str2num(fn);
    fn       = input('Enter file name for device drain current versus gate-source voltage(nvcovgsidpmos.dat): ','s');
    if length(fn) == 0
        fn = 'nvcovgsidpmos.dat';
    end
    data     = dlmread(fn,' ', 4, 0);
    vgs_id   = data(:,1);
    id_vgs   = data(:,2);
    % Gate-source voltage for this simulation must be the same as specified
    % for noise characterization.
    fn     = input('Enter file name for 1 cycle of drain current at 10 MHz(nvcoidpmos.dat): ', 's');
    if length(fn) == 0
        fn = 'nvcoidpmos.dat';
    end
    data   = dlmread(fn,' ', 4, 0);
    t_id10m = data(:, 1);
    id10m_t = data(:, 2);
    l_idvgs = length(id_vgs)/2;
    maxindx = find(id_vgs==max(id_vgs));    % Limit index to the proper range.
    var2    = mean(id10m_t);
    var2    = (max(id10m_t)+var2)*0.5;
    var1    = abs(id_vgs-var2);             % Choose point to determine delay.
    i       = 0;
    while i==0                              % If index out of range, redo.
        var2 = find(var1==min(var1));
        if ((var2 < maxindx)&(maxindx > l_idvgs)) | ((var2 > maxindx)&(maxindx < l_idvgs))
            i = 1;
        end
        var1(var2) = 1;
    end
    var3       = abs(id10m_t-id_vgs(var2));
    var4       = find(var3==min(var3));
    var3(var4) = 1;
    var5       = find(var3==min(var3));
    var3(var5) = 1;
    var6       = find(var3==min(var3));
    var3(var6) = 1;
    var7       = find(var3==min(var3));
    var4       = min([var4 var5 var6 var7]);
    var5       = t_id10m(var4-nspline:var4+nspline);    % Interpolate
    var6       = id10m_t(var4-nspline:var4+nspline);
    tdelay     = spline(var6, var5, id_vgs(var2));
    var6       = asin(vgs_id(var2)/vgpk)/2/pi/10e6;
    if var6 < 0
        var6 = -var6;
    end
    tdelay     = tdelay - var6;
    if tdelay > 50e-9
        tdelay = tdelay - 50e-9
    else
        tdelay
    end

```

Figure D.2 MATLAB listing to compute propagation of transistor under test.

APPENDIX E
MATLAB SCRIPT FOR PHASE NOISE COMPUTATION

```
clear

% Constant definitions.
SQ_RT_2 = 2^0.5;
N2      = 256;              % Number of samples per oscillation period.
nspline = 8;                % Number of samples used for interpolation.
FFT_LEN = 4096;             % Number of data points to compute FFT.
fa_ofs  = logspace(4,8,41); % Offset freq range for phase noise analysis, from
                            % 10 KHz to 100 MHz with 10 data points per decade.
NFA_OFS = 41;               % Total number of frequency points.
NMIN_XSP= 1024;             % Min. no. of data points to compute excess phase.

t1 = -1;
while t1 < 0
    % Read in VCO output data without injected noise for reference
    fn   = input('Enter file name for reference output signal (no injected noise, nvcov
                  ref.dat): ', 's');
    if length(fn) == 0
        fn = 'nvcovref.dat';
    end
    NISF = input('Enter no. of samples per period for ISF: ');
    ipm  = input('Enter magnitude of injected noise current pulse amplitude (A): ');
    ipw  = input('Enter injected noise current pulse width (sec): ');

    data = dlmread(fn,' ', 4, 0);
    ta0  = data(:,1);
    sig0 = data(:,2);
    N    = length(sig0);
    % Find 1st zero crossing
    i  = floor(N/2);            % Init index to exclude transient response.
    sm = 1;                     % Initialize state machine.
    while sm ~= 0
        i = i + 1;
        if sig0(i) < 0              % Look for negative half cycle
            sm = -1;                % Detect negative half cycle.
        elseif sm*sig0(i) < 0   % Look for zero crossing.
            sm = 0;                     % Detect zero crossing.
        end
    end
    x     = sig0(i-nspline:i+nspline);
    y     = ta0(i-nspline:i+nspline);
    t1    = spline(x,y,0);          % Time origin, 1st zero-crossing.
    t_xcf = t1;                 % Save time of 1st zero crossing.
    i_xcf = i - nspline;        % Save index near 1st zero crossing.

```

```
    % Count number of cycles.
    i1       = i;
    sm       = 1;
    no_cycle = 0;
    for i=i1:N-nspline-1
        i = i + 1;
        if sig0(i) < 0
            sm = -1;            % Detect negative half cycle.
        elseif sm*sig0(i) < 0   % Look for zero crossing.
            sm = 1;                     % Detect zero crossing, reinitialize flag.
            no_cycle = no_cycle + 1;
            i2 = i;                     % Save current index of zero crossing point.
        end
    end
    x     = sig0(i2-nspline:i2+nspline);
    y     = ta0(i2-nspline:i2+nspline);
    t2    = spline(x,y,0);                      % Last zero-crossing.
    i_xcl = i2;                             % Save index near last zero crossing.

    tper    = (t2 - t1)/no_cycle;           % Compute signal period.
    1/tper
    tsamp   = tper/N2;
    dt_tper = tper*(0:N2-1)/N2;
    isf_win = tper*(5*FFT_LEN/N2+1);
    t1      = t2 - NISF*isf_win;            % Define time of 1st noise impulse.
    if t1 < 0
        fprintf('\nERROR !!!');
        fprintf('\nSimulation time must be increased by at least %5.1f ns\n', abs(t1*1e
                9));
    end
end

t2 = t1 + tper*4*FFT_LEN/N2 - tper/4;       % Time near start of 1st ISF window.
% Compute period of impulse function.
tper_isf = isf_win + tper/NISF;
fprintf('\nUse injected current pulse with period of \t%10.5f ns', tper_isf*1e9);
fprintf('\nand delay time of                         \t%10.5f ns', t1*1e9);

% Read in VCO output data with njected current pulses to compute ISF.
fn   = input('\n\nEnter file name for VCO output signal with injected noise (nvcoisfcmo
             s.dat): ', 's');
if length(fn) == 0
    fn = 'nvcoisfcmos.dat';
end
data = dlmread(fn,' ', 4, 0);
ta1  = data(:,1);
sig1 = data(:,2);

i_t2      = 1;                      % Initialize array index.
i1        = 1;                      % Init index for noise-injected waveform.
gamma     = zeros(1, NISF);         % Initialize array.
perr_last = 0;
for iisf = 1:NISF
    while t2 > ta0(i_t2)            % Find index corresponding to time t2.
        i_t2 = i_t2 + 1;
    end
    sm = 1;                         % Initialize state machine.
    while sm ~= 0                   % Find zero crossing.
        i_t2 = i_t2 + 1;
        if sig0(i_t2) < 0                   % Look for negative half cycle
```

```
            sm = -1;                    % Detect negative half cycle.
        elseif sm*sig0(i_t2) < 0        % Look for zero crossing.
            sm = 0;                     % Detect zero crossing.
        end
    end
    x  = sig0(i_t2-nspline:i_t2+nspline);
    y  = ta0(i_t2-nspline:i_t2+nspline);
    t1 = spline(x,y,0);                 % Zero-crossing.

    % Resampling reference waveform.
    sigr(1) = 0;
    tar(1)  = t1;
    for i = 2:FFT_LEN
        t1 = t1 + tsamp;
        while t1 > ta0(i_t2)
            i_t2 = i_t2 + 1;
        end
        y       = sig0(i_t2-nspline:i_t2+nspline);
        x       = ta0(i_t2-nspline:i_t2+nspline);
        tar(i)  = t1;
        sigr(i) = spline(x,y,t1);
    end
    SIGR      = fft(sigr,FFT_LEN);
    sigindx   = 1 + FFT_LEN/N2;
    phaseref  = angle(SIGR(sigindx));

    % Resampling noise-injected waveform.
    for i = 1:FFT_LEN
        t = tar(i);
        while t > ta1(i1)
            i1 = i1 + 1;
        end
        y       = sig1(i1-nspline:i1+nspline);
        x       = ta1(i1-nspline:i1+nspline);
        sig2(i) = spline(x,y,t);
    end
    SIG2        = fft(sig2,FFT_LEN);
    phase_err   = phaseref - angle(SIG2(sigindx));
    gamma(iisf) = phase_err - perr_last;
    perr_last   = phase_err;
    t2          = t2 + isf_win;         % Time near beginning of next ISF window.
    fprintf('%3d', iisf);
end
fprintf('\n');
var1  = mean(gamma.^2)^0.5;
if var1 > 1e-3
    fprintf('\nWARNING !!! The injected noise current is too large !!!');
    fprintf('\nReduce by a factor of about %5.1f for better accuracy\n', var1/6e-4);
elseif var1 < 2e-4
    fprintf('\nWARNING !!! The injected noise current is too small !!!');
    fprintf('\nIncrease by a factor of about %5.1f for better accuracy\n', 6e-4/var1);
end
gamma = [gamma gamma(1:3)];

    % Curve fit ISF with polynomial
    w0t    = (0:NISF+2)*2*pi/NISF;      % Normalized sampling phase argument.
    var1   = min([9 NISF-1]);
    pgamma = polyfit(w0t, gamma, var1);

    % Interpolate ISF to N2 samples per period
```

```
    w0tn2  = 2*pi*(0:N2-1)/N2;
    gamma1 = polyval(pgamma,w0tn2);
    figure(1)
    plot(w0tn2,gamma1);
    xlabel('Normalized phase (radians)');
    ylabel('Scaled Impulse Sensitivity Function');
    grid


    sym_score = (sum(gamma1.^2))^.5/abs(mean(gamma1))
    ave_score = mean(gamma1)
    gmin_indx = find(gamma1==min(gamma1))
    gdly      = tper*gmin_indx/N2

% Read actual VCO drain and gate signals into memory to characterize noise
% behavior of the transistor.  If noise source is white such as that of
% resistors, just press 'ENTER'.
fn     = input('Enter file name for drain signal or ''ENTER'' if white noise: ', 's');
if length(fn) > 0
    data   = dlmread(fn,' ', 4, 0);
    sigd   = data(i_xcf:i_xcl, 2);
    save vcopn6_tmp
    fn     = input('Enter file name for gate-source signal(nvcovgspmos.dat): ', 's');
    if length(fn) == 0
        fn = 'nvcovgspmos.dat';
    end
    data   = dlmread(fn,' ', 4, 0);
    t_sigg = data(i_xcf:i_xcl, 1);
    sigg   = data(i_xcf:i_xcl, 2);
    vddc   = (max(sigd)+min(sigd))*0.5;
    vdpk   = max(sigd) - vddc;
    vgdc   = (max(sigg)+min(sigg))*0.5;
    vgpk   = max(sigg) - vgdc;
    gain   = vdpk/vgpk;
    vgpk   = floor(vgpk*10000+0.5)/10000;

    fprintf('\nUse these results to do noise characterization:');
    fprintf('\nDC drain voltage is \t%9.4f V', vddc);
    fprintf('\nPeak drain voltage is \t%9.4f V', vdpk);
    fprintf('\nDC gate voltage is \t\t%9.4f V', vgdc);
    fprintf('\nPeak gate voltage is \t%9.4f V', vgpk);
    fprintf('\nVoltage gain from gate to drain is \t%9.4f\n\n', gain);

    % Read noise characterization data into memory
    fn = input('\nEnter file name for noise data at 10 KHz(nvconpmos.dat): ', 's');
    if length(fn) == 0
        fn = 'nvconpmos.dat';
    end
    data      = dlmread(fn,' ', 4, 0);
    vgs_idnsq = data(:,1);
    idnsq_vgs = data(:,2);
    % This data file is expected to match the desired phase noise frequency
    % range (10 KHz - 100 MHz with 10 points/decade) and further extended
    % into higher frquencies where white noise is dominant. This
    % requirement is for coding simplification.
    fn = input('Enter file name for noise vs frequency(nvconpmosfreq.dat): ','s');
    if length(fn) == 0
        fn = 'nvconpmosfreq.dat';
    end
    data      = dlmread(fn,' ', 4, 0);
```

```
f_idnpss  = data(:,1);
idnpss_f  = data(:,2);
fn = input('Enter file name for Id vs Vgs (nvcovgsidpmos.dat): ','s');
if length(fn) == 0
    fn = 'nvcovgsidpmos.dat';
end
data      = dlmread(fn,' ', 4, 0);
vgs_id    = data(:,1);
id_vgs    = data(:,2);
% Gate-source voltage for this simulation must be the same as specified
% for noise characterization.
fn = input('Enter file name for 1 cycle of Id at 10 MHz(nvcoidpmos.dat): ', 's');
if length(fn) == 0
    fn = 'nvcoidpmos.dat';
end
data    = dlmread(fn,' ', 4, 0);
t_id10m = data(:, 1);
id10m_t = data(:, 2);
l_idvgs = length(id_vgs)/2;
maxindx = find(id_vgs==max(id_vgs));    % Limit index to the proper range.
var2    = mean(id10m_t);
var2    = (max(id10m_t)+var2)*0.5;
var1    = abs(id_vgs-var2);             % Choose point to determine delay.
i       = 0;
while i==0                              % If index out of range, redo.
    var2 = find(var1==min(var1));
    if ((var2<maxindx)&(maxindx>l_idvgs)) | ((var2>maxindx)&(maxindx<l_idvgs))
        i = 1;
    end
    var1(var2) = 1;
end
var3       = abs(id10m_t-id_vgs(var2));
var4       = find(var3==min(var3));
var3(var4) = 1;
var5       = find(var3==min(var3));
var3(var5) = 1;
var6       = find(var3==min(var3));
var3(var6) = 1;
var7       = find(var3==min(var3));
var4       = min([var4 var5 var6 var7]);
var5       = t_id10m(var4-nspline:var4+nspline);    % Interpolate
var6       = id10m_t(var4-nspline:var4+nspline);
tdelay     = spline(var6, var5, id_vgs(var2));
var6       = asin(vgs_id(var2)/vgpk)/2/pi/10e6;
if var6 < 0
    var6 = -var6;
end
tdelay     = tdelay - var6
if tdelay > 50e-9
    tdelay = tdelay - 50e-9
end
fn = input('Press ENTER to accept or enter new delay time: ', 's');
if length(fn) > 0
    tdelay = str2num(fn);
end

% Determine no. of data points needed for accurate computation of the
% effect of delay on the device drain current.
scale_N2   = ceil(tper/(tdelay/128)/N2);

```

```
% Resampling one period of Vgs to determine noise current behavior
t     = t_xcf;
i1    = 1;
dt_sc = tsamp/scale_N2;
N2S   = N2*scale_N2;
for i = 1:N2S
    while t > t_sigg(i1)
        i1 = i1 + 1;
    end
    y        = sigg(i1-nspline:i1+nspline);
    x        = t_sigg(i1-nspline:i1+nspline);
    sigg1(i) = spline(x,y,t);       % Vg sampled at N2 samples per osc period.
    t        = t + dt_sc;
end

% Compute drain current within 1 oscillation cycle, taking delay into
% account.
sigg1      = [sigg1 sigg1(1)] - vgdc;
sigg1_indx = find(vgs_id==0) + floor(sigg1/(vgs_id(2)-vgs_id(1))+0.5);
var1       = 0;
var2       = 1;
var3       = sigg1_indx(1);
var4       = id_vgs(var3-nspline:var3+nspline);
var5       = vgs_id(var3-nspline:var3+nspline);
did        = spline(var5,var4,sigg1(1));
data       = zeros(1,N2S);
while var1 ~= var2
    var2 = var1;
    for i = 1:N2S
        data(i) = var1 + did*(1 - exp(-dt_sc/tdelay));
        var1    = data(i);
        var3    = sigg1_indx(i+1);
        var4    = id_vgs(var3-nspline:var3+nspline);
        var5    = vgs_id(var3-nspline:var3+nspline);
        did     = spline(var5,var4,sigg1(i+1)) - var1;
    end
end
var1 = 1;
for i=1:scale_N2:N2S                        % Reduce data points to N2.
    id_dly(var1) = data(i);
    var1         = var1 + 1;
end
figure(2)
plot(w0tn2,id_dly)
grid

% Compute current noise for 1 oscillation cycle.
var4  = 1;
for i = 1:N2
    var1 = abs(1 - id_vgs/id_dly(i));
    var2 = find(var1==min(var1));   % Find index of 1st closest match to id_dly(i)
    var1(var2) = max(var1);
    var3 = find(var1==min(var1));   % Find index of 2nd closest match to id_dly(i)
    if abs(var2-var4) > abs(var3-var4)      % Select one closer to previous index.
        var2 = var3;
    end
    var4       = var2;
    idnrms(i)  = idnsq_vgs(var2)^0.5;
end
figure(3)
```

```
    plot(w0tn2,idnrms)
    grid

    var1       = idnpss_f(length(idnpss_f));    % Thermal noise from assumption given.
    var3       = idnpss_f(1);                   % Average noise of ref frequency (10 KHz)
    gam_idn    = gamma1.*idnrms;                % Combine ISF and noise of ref freq (10 KHz)
    GAMMA1     = fft(gam_idn,N2);
    var2       = abs(GAMMA1(1:17));             % Consider only the 1st 16 harmonics.
    hfnoise    = sum((var2(2:17)*2/N2).^2)*((var1/var3)^2);
    dw         = 2*pi*fa_ofs;
    dw2        = dw.*dw;
    lfnscale   = 2*(var2(1)/N2/var3)^2;
    xspscale   = 4*(ipm*ipw)^2*dw2;

    % Compute phase noise
    for i = 1:NFA_OFS
        lfnoise = lfnscale*idnpss_f(i)^2;
        if abs((fa_ofs(i)-f_idnpss(i))/fa_ofs(i)) > 0.0001
            error('\n\nERROR !!! Phase noise offset frequency does not match\n');
        end
        xsp(i)  = (hfnoise+lfnoise);
    end
    xsp = xsp./xspscale;
    pn  = 10*log10(xsp);
    pn(11:10:21)

    gamma1 = [gamma1(30:N2) gamma1(1:29)];
    for i_gamma = 1:64
        gam_idn    = gamma1.*idnrms;
        GAMMA1     = fft(gam_idn,N2);
        dc_res(i_gamma) = abs(GAMMA1(1));
        gamma1 = [gamma1(N2) gamma1(1:N2-1)];
    end
    find(dc_res==min(dc_res))
    ccolor = input('Enter curve color: ', 's');
    figure(4)
    xvector = 1:64;
    xvector = xvector - 30;
    plot(xvector,dc_res,ccolor)

else
    % Noise source is white.
    var1       = input('Enter current spot noise level (A/sqrt Hz): ');
    % Determine noise folding scale factor.
    GAMMA1     = fft(gamma1,N2);
    var2       = abs(GAMMA1(1:17));     % Consider only the 1st 16 harmonics.
    var2(2:17) = var2(2:17)*SQ_RT_2;    % Account for double sideband noise around harmonics.
    scale      = sum(var2.^2)^0.5;
    % Merge with other scale factors.
    scale      = scale/N2/ipm/ipw*SQ_RT_2*var1;
    dw         = fa_ofs*2*pi;
    xsp        = scale./dw;
    pn         = 20*log10(xsp);
end
pn(11:10:21)
fn = input('Enter file name to save data (RETURN to skip): ', 's');
if length(fn) > 0
    clear data ta0 sig0 ta1 sig1 sigd t_sigg sigg
    save(fn)
end
```

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