# A New Area and Power Efficient Single Edge Triggered Flip-Flop Structure for Low Data Activity and High Frequency Applications 

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#### Abstract

In this work, a new area and power efficient single edge triggered flip-flop has been proposed. The proposed design is compared with six existing flip-flop designs. In the proposed design, the number of transistors is reduced to decrease the area. The number of clocked transistors of the devised flip-flop is also reduced to minimize the power consumption. As compared to the other state of the art single edge triggered flip-flop designs, the newly proposed design is the best energy efficient with the comparable power delay product (PDP) having an improvement of up to $61.53 \%$ in view of power consumption. The proposed flip-flop also has the lowest transistor count and the lowest area. The simulation results show that the proposed flip-flop is best suited for low power and low area systems especially for low data activity and high frequency applications.


Keywords: PDP, reliability, delay, process node, clock frequency

## 1. INTRODUCTION

The latest advances in mobile battery-powered devices such as the Personal Digital Assistant (PDA) and mobile phones have set new goals in digital VLSI design. The portable devices require high speed and low power consumption. So the power dissipation has become a prominent issue [1]. For big circuits implementing complex functionalities like control units, microprocessors, usually a very large number of flip-flops are used. So the flip-flops heavily affect the performance of the entire system. This paper focuses on the minimization of power dissipation in the edge triggered flip-flops. Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. The power, delay, and reliability of the flip-flops directly affect the performance and fault tolerance of the whole electronic system [2]. Therefore, it is imperative to carefully design flip flops for minimum area, delay, power, and maximum reliability. Several flip-flop designs have been proposed for power reduction. Some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems.

In this paper, a new high performance, low power and low transistor count single edge triggered flip-flop is devised. The proposed single edge triggered flip-flop is compared with the conventional designs. For all circuits, simulations are carried on 130 nm process node using BSIM3 models. This paper is organized into five sections. Section 2 outlines the conventional flip flop structures investigated in this paper. In section 3, a new flip-flop
is described. The nominal simulation conditions and results are discussed in section 4. Section 5 has concluding remarks.

## 2. CONVENTIONAL FLIP-FLOP STRUCTURES

To improve the performance of a conventional Transmission Gate Flip-Flop (TGFF shown in Fig. 1) [3, 4], addition of an inverter and transmission gate between the outputs of master and slave latches to accomplish a push-pull effect at the slave latch, was proposed in [5]. The static Push Pull Flip-Flop (PPFF) is shown in Fig. 2. The semi-static Pass Flip-Flop (Pass FF) was proposed by [6] as shown in Fig. 3. The number of transistors of this flip-flop was reduced to decrease the power consumption. The four transistors in the feedback path of conventional TGFF are replaced by single PMOS transistor. Hence, there is reduction of total 6 transistors in this flip-flop. To activate the feedback path of pass FF only during OFF cycle, a PMOS transistor was added in the feedback in Pass Isolation Flip-Flop (PIFF). This reduces short circuit current during ON cycle. It also improves speed as compared to Pass FF. The semi-static Pass Isolation Flip-Flop, shown in Fig. 4, was proposed by [6].

The Area Efficient flip-flop (AEFF) was proposed in [7]. This semi-static flip-flop is illustrated in Fig. 5. This flip-flop has lesser transistor count. In this design, the feedback circuit of the master section is removed and in slave section, feedback loop consists of a transmission gate. This reduces the number of transistor to make this flip-flop a low transistor count flip-flop. The Low Voltage Flip Flop (LVFF), proposed by [8], is shown in Fig. 6. In this flip-flop, the feedback is provided by only a single transistor. So this has lesser number of transistor as compared to other discussed flip flops. The main advantage of this design is reduced device count and decreased parasitic capacitance at internal nodes of the flip flop which results in improved power-delay product. Fig. 7 shows the static $\mathrm{C}^{2}$ MOS Flip- Flop [9]. This flip-flop consists of a $\mathrm{C}^{2}$ MOS feedback at the outputs of the master and the slave latches. There are 20 transistors in this circuit. So $\mathrm{C}^{2}$ MOSFF has largest area.

## 3. PROPOSED LOW AREA AND POWER EFFICIENT FLIP-FLOP STRUCTURE

A new SET flip-flop structure is proposed in this paper. The proposed flip-flop (proposed FF) is shown in Fig. 8. Because of the drop due to the threshold of the transistors and due to the leakage in the capacitors of the transistors, there is need for the feedback loop. An NMOS transistor with complemented clock signal is used to make feedback path functional only during OFF cycle of the clock. This reduces short circuit current during ON cycle. If PMOS transistor with clock signal is used in feedback, the logic level at the output node Q would be maintained when the clock is in the logic level 'HIGH' rather than the logic level 'LOW'. Hence, when the clock is stopped (grounded), the circuit would show a dynamic behavior instead of static behavior. This limitation is overcome by using a NMOS transistor in feedback instead of PMOS transistor. To reduce the number of transistor, only NMOS transistor is used in both master and slave latches. The proposed flip-flop is positive edge triggered and semi-static in nature. There are only 9 transistors in this flip-flop, in which 3 are clocked transistors. The area occupied by the design is directly proportional to the number of transistors in the design i.e. the transistor count. [7] The transistor count of the proposed design is lesser than any existing design therefore the proposed design consumes lowest chip area with substantial cost saving.

In the proposed FF when clock level is 'LOW', master latch is activated and inverse of the data is stored to intermediate node N . When clock goes to 'HIGH' logic level, slave latch becomes functional and produces data at
output Q . In the proposed design, device count is reduced and parasitic capacitances at internal nodes of the flip-flop are decreased which results in improved power dissipation. If there is reduction in the number of clocked transistors design, the clock load capacitance is reduced, leading to low power consumption in the clock distribution network The proposed FF has the lowest number of clocked transistor. Thus by reducing the number of clocked transistors, power dissipation of the proposed design is further reduced.

## 4. EXPERIMENTAL DATA AND DISCUSSION

Simulation parameters used for comparison, are shown in table 1. All simulations are performed on TSpice using BSIM 3 v 3 level 53 models in 130 nm process node. The supply voltage is varied from 1.3 V to 1.6 V . The clock frequency is varied from 200 MHz to 1 GHz . The results are carried out for the period of 16 data sequences. Under nominal condition, a 16 -cycle sequence 0100000000000000 that is a low data activity is supplied at the input for average power and PDP measurements. However the dynamic power consumption is dependent on switching activities at various nodes of the circuit. It varies with different data rates and circuit topologies. Hence to obtain a fair idea of power dissipation for a circuit topology, different data patterns should be applied with different activity rates [11]. So in simulations, following five different data sequences also have been adopted to compare the power consumption of flip-flop structures discussed in this paper:
i) $\quad 1111111111111111(\mathrm{~A}=0)$
ii) $0000000000000000(\mathrm{~A}=0)$
iii) $1111010110010000(\mathrm{~A}=0.18)$
iv) $\quad 1100110011001100(\mathrm{~A}=0.5)$
v) $1010101010101010(\mathrm{~A}=1)$

Where ' A ' is the data activity.

In this paper, total power is taken as the power metric. The designs are simulated so as to achieve minimum powerable II shows power consumption in $\mu \mathrm{W}$ as a function of data activity for nominal conditions. For $0 \%$ data activities (when all are 0's or all are 1's) and $18.75 \%$ data activity, the proposed FF consumes the least power. For and $100 \%$ data activities AEFF consumes the least power. So, the proposed FF consumes the lowest power for low activities. For fair comparison, the average of power consumption at all data activities is taken. This average result shows that the proposed FF has $15.02 \%, 14.69 \%, 19.46 \%, 10.60 \%, 10.78 \%$ and $25.75 \%$ improvement in average power consumption when compared to the previously proposed flip-flops discussed in section 2 . The proposed FF shows the lowest power consumption while $\mathrm{C}^{2}$ MOSFF shows the highest power consumption. Table III shows consumption in $\mu \mathrm{W}$ as a function of data activity for 1 GHz clock frequency. The proposed FF has the lowest power consumption for $0 \%$ data activities (when all are 0 's or all are 1 's) and $18.75 \%$ data activity. For $50 \%$ and $100 \%$ data
activities AEFF and the proposed FF consumes the lowest and the second lowest power respectively. For fair comparison, the average of power consumption at all data activities is taken. This average result shows that the proposed FF has $15.98 \%, 23.30 \%, 28.45 \%, 9.12 \%, 24.15 \%$ and $36.44 \%$ lesser power consumption as compared to previously proposed flip-flops discussed in section 2. C2MOS FF and the proposed FF consume the highest and the lowest power respectively. For $0 \%$ data activity (when all are 1 's), the proposed FF consumes $28.65 \%, 39.86 \%$, $42.96 \%, 35.16 \%, 45.99 \%$ and $50.60 \%$ lesser power, while for $0 \%$ data activity (when all are 0 's), the proposed FF $37.11 \%, 45.74 \%, 50.81 \%, 35.89 \%, 50.81 \%$ and $61.53 \%$ improvement in power consumption as compared to the existing flip-flops.

Table IV shows the power and PDP for nominal conditions. Table shows that the proposed FF consumes $29.82 \%, 34.69 \%, 37.67 \%, 9.60 \%, 36.81 \%$ and $48.59 \%$ lesser power as compared to the existing flip-flops discussed in section 2. Table shows that the proposed FF exhibits $8.81 \%$ and $30.92 \%$ lesser PDP as compared to PPFF and Pass FF respectively. However, the proposed FF has $14.42,18.06,38.38 \%$ and $22.46 \%$ higher PDP as compared to PIFF, AEFF, LVFF and $C^{2}$ MOSFF respectively. Table $V$ shows power consumption in microwatts as a function of clock frequency. For 200 MHz and 250 MHz clock frequencies, LVFF shows the lowest power consumption, while AEFF and the proposed FF show the second lowest and third lowest power consumption respectively. As the clock frequency increases, the power performance of the proposed FF improves in comparison to other flip-flops, for 400 MHz and 1 GHz clock frequencies the proposed FF consumes the lowest power. For fair comparison, the average of power consumption at all clock frequencies is taken. C2MOS FF consumes the highest power and the proposed FF consumes the lowest power. This average result shows that the proposed flip-flop has $13.38 \%, 13.95 \%, 20.92 \%$, $2.63 \%, 8.16 \%$ and $23.49 \%$ improvement in average power consumption when compared to the existing flip-flops presented in section 2 respectively. While, for 1 GHz clock frequency, the proposed FF consumes $14.08 \%, 21.19 \%$, $25.64 \%, 4.99 \%, 19.96 \%$ and $33.93 \%$ lower power consumption.

Table VI indicates the power consumption in microwatts at different supply voltages for 400 MHz clock frequency. Table shows that the proposed FF has the lowest power dissipation for 1.3 V and 1.4 V supply voltages; however the proposed FF has the second lowest power dissipation for 1.6 V . For fair comparison, the average of consumption at all voltages is taken. The proposed Flip-Flop has $19.38 \%, 21.17 \%, 28.13 \%, 25.67 \%$ and $9.85 \%$ lesser average power dissipation when compared to the discussed existing flip-flops respectively except AEFF, the flip-flop has $2.30 \%$ more power than AEFF, however at nominal voltage, the proposed FF consumes $9.60 \%$ lower power than AEFF. The power consumption in microwatts at different supply voltages for 1 GHz clock frequency is shown in VII. Table shows that the proposed FF has the lowest power dissipation for 1.3 V and 1.4 V supply voltages; however the proposed FF has the second lowest power dissipation for 1.6 V , at this voltage AEFF has the lowest power consumption. For fair comparison, the average of power consumption at all voltages is taken. The proposed has $17.76 \%, 28 \%, 31.43 \%, 11.11 \%, 27.07 \%$ and $43.19 \%$ improvement in power efficiency as compared to the
discussed existing flip-flops respectively. The proposed FF has the lowest number of transistors and also has the number of clocked transistors as shown by table VIII.

## 5. CONCLUSION

A comparative analysis of single input single edge triggered flip-flops has been done. Among previously proposed flip-flops discussed in section 2, AEFF and $\mathrm{C}^{2}$ MOSFF show the lowest and the highest power consumption respectively. LVFF shows the lowest PDP. $\mathrm{C}^{2}$ MOSFF has the largest number of transistor and the highest power consumption, so this flip-flop is not suited for low power and low area applications. Pass FF has the highest PDP, so this flip-flop is not suited for high performance applications. The new flip-flop structure has been proposed in this paper. The proposed flip-flop structure is compared on the basis of power, PDP and transistor count with the existing flip-flop structures. The proposed FF has lesser power consumption than all the existing flip-flops discussed in section 2 and has up to $61.53 \%$ improvement in average power consumption. The proposed FF exhibits up to $30.92 \%$ lesser PDP and up to $38.38 \%$ higher PDP as compared to discussed existing flip-flops. For low clock frequencies ( 200 MHz and 250 MHz ), LVFF shows the lowest power consumption, while AEFF and the proposed FF show the second lowest and third lowest power consumption respectively. However, as the clock frequency increases, the power performance of the proposed FF improves in comparison to other flip-flops and for higher clock frequencies ( 400 MHz and 1 GHz ), the proposed FF consumes the lowest power. For higher data activities ( $50 \%$ and $100 \%$ ) AEFF and the proposed FF consume the lowest and the second lowest power respectively. For lower data activities ( $0 \%$ (when all are 0 's or all are 1 's) and $18.75 \%$ ), the proposed FF consumes the lowest power among all the discussed flip-flops. The simulation results show that the proposed FF consumes the lowest power having the lowest transistor count. So, the proposed FF is an area and power efficient flip-flop best suited for low data Activity and high frequency applications.

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| S. No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Particu <br> lars | CMOS <br> Technology | Min. <br> Gate <br> Width | Max. <br> Gate <br> Width | MOSFET <br> Model | Nominal <br> Supply <br> Voltage | Tempera ture | Duty <br> Cycle | Nominal | Sequence <br> Length | Rise Time of Clock \& Data | Fall Time of Clock \& Data |
|  |  |  |  |  |  |  |  | Clock |  |  |  |
|  |  |  |  |  |  |  |  | Frequency |  |  |  |
| Value | 130 nm | $\begin{aligned} & 260 \\ & \mathrm{~nm} \end{aligned}$ | $\begin{aligned} & 1.04 \\ & \mu \mathrm{~m} \end{aligned}$ | BSIM 3v3 <br> level 53 | 1.3 V | $25^{\circ} \mathrm{C}$ | $50 \%$ | 400 MHz | 16 Data | 100 ps | 100 ps |
|  |  |  |  |  |  |  |  |  | Cycles |  |  |

Table I: CMOS Simulation Parameters

| Data <br> Activity | PPFF | Pass FF | PIFF | AEFF | LV FF | C$^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \%$ <br> (all 1's) | 3.30 | 3.60 | 3.80 | 6.20 | 4.00 | 4.30 | 1.91 |
| $0 \%$ <br> (all 0's) | 3.20 | 3.50 | 3.64 | 2.58 | 4.00 | 4.80 | 1.90 |
| $18.75 \%$ | 5.70 | 5.50 | 5.94 | 5.00 | 5.24 | 6.30 | 4.69 |
| $50 \%$ | 5.70 | 5.70 | 6.13 | 4.98 | 5.20 | 6.30 | 5.79 |
| $100 \%$ | 8.40 | 7.90 | 8.22 | 6.26 | 6.60 | 8.40 | 8.05 |
| Average | 5.26 | 5.24 | 5.55 | 5.00 | 5.01 | 6.02 | 4.47 |

Table II: Power consumption in microwatts as a function of data activity at 400 MHz clock frequency

| Data <br> Activity | PPFF | Pass FF | PIFF | AEFF | LV FF | C$^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \%$ <br> (all 1's) | 6.98 | 8.28 | 8.73 | 7.68 | 9.22 | 10.08 | 4.98 |
| $0 \%$ <br> (all 0's) | 6.79 | 7.87 | 8.68 | 6.66 | 8.68 | 11.10 | 4.27 |
| $18.75 \%$ | 9.52 | 10.38 | 11.00 | 8.61 | 10.22 | 12.38 | 8.18 |
| $50 \%$ | 9.51 | 10.26 | 10.99 | 8.79 | 10.19 | 11.98 | 8.92 |
| $100 \%$ | 12.25 | 12.54 | 13.51 | 9.89 | 11.57 | 14.03 | 11.5 |
| Average | 9.01 | 9.87 | 10.58 | 8.33 | 9.98 | 11.91 | 7.57 |

Table III: Power consumption in microwatts as a function of data activity at 1 GHz clock frequency

| Parameter | PPFF | Pass FF | PIFF | AEFF | LV FF | C$^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power <br> $(\mu \mathrm{W})$ | 3.89 | 4.18 | 4.38 | 3.02 | 4.32 | 5.31 | 2.73 |
| PDP <br> $\left(10^{-18} \mathrm{~J}\right)$ | 515.15 | 680.04 | 402.04 | 384.93 | 289.46 | 364.27 | 469.78 |

Table IV: Power and PDP at nominal conditions

| Clock Freq. | PPFF | Pass FF | PIFF | AEFF | LV FF | C$^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 200 MHz | 4.20 | 4.00 | 5.01 | 3.66 | 3.30 | 4.00 | 3.82 |
| 250 MHz | 4.50 | 4.20 | 4.25 | 4.01 | 3.80 | 4.40 | 4.04 |
| 400 MHz | 5.70 | 5.50 | 5.94 | 5.00 | 5.24 | 6.30 | 4.69 |
| 10000 MHz | 9.52 | 10.38 | 11.00 | 8.61 | 10.22 | 12.38 | 8.18 |
| Average | 5.98 | 6.02 | 6.55 | 5.32 | 5.64 | 6.77 | 5.18 |

Table V. Power consumption in $\mu \mathrm{W}$ as a function of clock frequency for $18.75 \%$ data activity

| VDD | PPFF | Pass FF | PIFF | AEFF | LV FF | C $^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1.3 V | 3.89 | 4.18 | 4.38 | 3.02 | 4.32 | 5.31 | 2.73 |
| 1.4 V | 4.42 | 4.82 | 5.05 | 3.54 | 4.98 | 6.18 | 3.47 |
| 1.6 V | 6.24 | 5.89 | 6.88 | 4.89 | 6.48 | 8.02 | 5.52 |
| Average | 4.85 | 4.96 | 5.44 | 3.82 | 5.26 | 6.50 | 3.91 |

Table VI. Power consumption in $\mu \mathrm{W}$ as a function of supply voltage at 400 MHz clock frequency

| VDD | PPFF | Pass FF | PIFF | AEFF | LV FF | C $^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1.3 V | 7.56 | 8.42 | 9.23 | 7.06 | 9.10 | 11.93 | 5.31 |
| 1.4 V | 8.93 | 11.05 | 11.32 | 8.43 | 10.22 | 12.84 | 6.47 |
| 1.6 V | 12.41 | 13.53 | 14.11 | 11.25 | 13.25 | 17.04 | 11.98 |
| Average | 9.63 | 11.00 | 11.55 | 8.91 | 10.86 | 13.94 | 7.92 |

Table VII. Power consumption in $\mu \mathrm{W}$ as a function of supply voltage at 1 GHz clock frequency

| Flip-Flop | PPFF | Pass FF | PIFF | AEFF | LV FF | C $^{2}$ MOS FF | Proposed FF |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| No of Transistor | 16 | 10 | 12 | 10 | 9 | 20 | 9 |
| No of Clocked Transistor | 6 | 4 | 6 | 4 | 5 | 8 | 3 |

Table VIII. Transistor count of discussed flip-flops


Fig. 1: Conventional Transmission Gate Flip-Flop (TGFF)


Fig. 2: Push Pull Flip-Flop (PPFF)


Fig. 3: Pass Flip-Flop (Pass FF)


Fig. 4: Pass Isolation Flip-Flop (PIFF)


Fig. 5: Area Efficient Flip-Flop (Area Efficient FF)


Fig. 6: Low Voltage Flip-Flop (LVFF)


Fig. 7: $\mathrm{C}^{2}$ MOS Flip-Flop ( $\mathrm{C}^{2}$ MOS FF)


Fig. 8: Proposed Flip-Flop (Proposed FF)

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