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A New Cascaded Multilevel H-Bridge Drive

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***Abstract*—In this paper, a general structure for cascaded power converters is presented in which any number of H-bridge cells having any number of voltage levels are series connected to form an inverter phase leg. Equations are introduced for determining an optimal voltage ratio of dc voltages for the H-bridge cells which will maximize the number of voltage levels obtainable resulting in high power quality. Special cases of the generalized inverter are presented including novel 11-level and 15-level inverters. Laboratory measurements demonstrate the proposed inverter performance.**

***Index Terms*—Cascaded, hybrid, medium voltage, multilevel, power quality, three-level.**

I. Introduction

MULTILEVEL power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concerns, low switching losses, and high-voltage capability [1]–[4]. The primary disadvantage of this technology is the large number of semiconductor devices required. This does not yield a significant cost increase since lower-voltage devices may be used. However, an increase in gate drive circuitry and more elaborate mechanical layout are required.

Although the diode clamped multilevel inverter [2]–[5] is commonly discussed in the literature, there has been considerable interest in the series connected or cascaded H-bridge inverter topologies [6]–[25]. The primary advantage of this structure is its simplicity and that fewer or more H-bridge cells can be cascaded in order to decrease or increase the voltage and power level respectively. The main disadvantage of this topology is that each H-bridge cell requires an isolated dc source. The isolated sources are typically provided from a transformer/rectifier arrangement [6], but may be supplied from batteries, capacitors [8] or photovoltaic arrays [17]. This topology was recently patented by Robicon Group in 1996 [6] and is one of the companies standard drive products.

Recent advances in cascaded H-bridge inverters include utilizing different dc voltages on each series H-bridge in order to increase the number of voltage levels and improve the power quality [19]–[23]. This concept was recently patented in 1998 [22] and 1999 [23].

In other research, two five-level H-bridge cells, operating at the same dc voltage, were cascaded forming a novel type of inverter [24] which can operate as a nine-level inverter. In this paper, the general idea of cascading multilevel H-bridge cells is introduced. This differs from previous research [19]–[24] in that there may be any number of cells, each with an arbitrary number of levels, and each with a unique dc voltage value in order to maximize power quality. This new topology will be referred to as a cascaded multilevel H-bridge inverter.

This paper contains generalized mathematical equations for determining the dc voltage ratio required in order to maximize power quality based on the number of multilevel cells. Laboratory validation of the new topology is presented in which a five-level H-bridge inverter is cascaded with a three-level inverter yielding up to 15-level performance.

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II. Generalized Cascaded Topology

Fig. 1 shows the structure of the generalized multilevel inverter. Therein, each phase consist of p multilevel H-bridge cells each with an isolated dc source. One advantage of this structure is that more or fewer H-bridge cells can be cascaded depending on the desired power quality. For system symmetry, it is reasonable to utilize the same set of dc voltages for each phase (i.e., $v_{\mathrm{dc}\,ai} = v_{\mathrm{dc}\,bi} = v_{\mathrm{dc}\,ci}$ where $i = 1, 2, \ldots p$). As can be seen, the inverter ground is isolated from the machine neutral point and each phase-to-ground voltage $v_{\mathrm{ag}}, v_{\mathrm{bg}}$, and v_{cg} is directly controlled by the ac output of the individual multilevel H-bridge cells as

$$v_{\mathrm{xg}} = \sum_{i=1}^{p} v_{\mathrm{xg}i} \tag{1}$$

where x represents the phase and can be a, b, or c. The machine phase voltages may be expressed in terms of the line-to-ground voltages by [25]

$$v_{\mathrm{as}} = \frac{2}{3}v_{\mathrm{ag}} - \frac{1}{3}v_{\mathrm{bg}} - \frac{1}{3}v_{\mathrm{cg}} \tag{2}$$

$$v_{\mathrm{bs}} = \frac{2}{3}v_{\mathrm{bg}} - \frac{1}{3}v_{\mathrm{ag}} - \frac{1}{3}v_{\mathrm{cg}} \tag{3}$$

$$v_{\mathrm{cs}} = \frac{2}{3}v_{\mathrm{cg}} - \frac{1}{3}v_{\mathrm{ag}} - \frac{1}{3}v_{\mathrm{bg}}. \tag{4}$$

For analysis purposes, it is sometimes helpful to transform the machine voltages into the q-d stationary reference fame using

$$v_{\mathrm{qs}}^{s} = \frac{2}{3}v_{\mathrm{as}} - \frac{1}{3}v_{\mathrm{bs}} - \frac{1}{3}v_{\mathrm{cs}} \tag{5}$$

$$v_{\mathrm{ds}}^{s} = \frac{1}{\sqrt{3}}(v_{\mathrm{cs}} - v_{\mathrm{bs}}). \tag{6}$$

As with the standard cascaded H-bridge inverter [6]–[18], the power quality of the cascaded multilevel H-bridge inverter may be greatly improved through utilization of different dc voltages on each cell [19]–[23]. In particular, according to the maximal distention principle introduced in [3], it can be shown that the

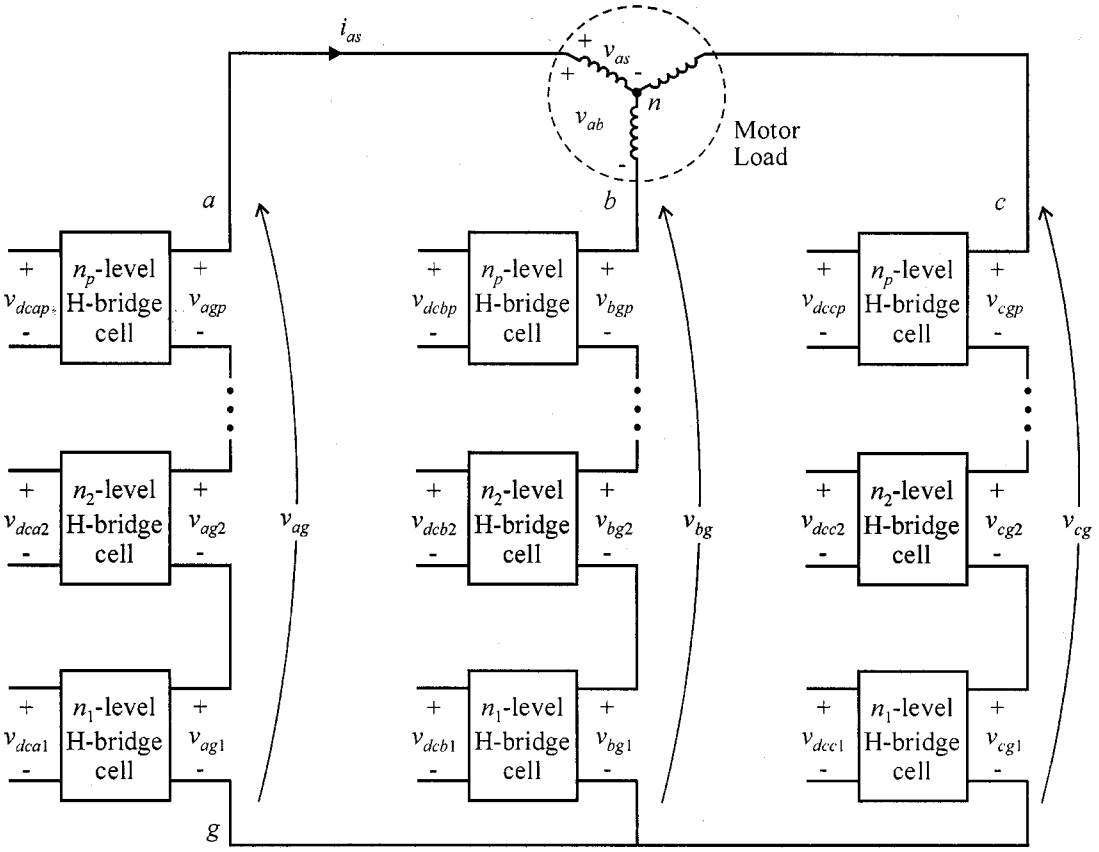

Fig. 1. Topology of the proposed cascaded multilevel H-bridge drive.

number of voltage levels is maximized if the dc voltages are set according to

$$v_{\mathrm{dc}\,x(i-1)} = \frac{n_i - 1}{n_i(n_{i-1} - 1)} v_{\mathrm{dc}\,xi} \quad i = 1,3,\ldots(p-1) \quad (7)$$

where n_i is the number of voltage levels that the ith H-bridge cell is capable of producing. Using the voltage ratios set by (7), the number of line-to-ground voltage levels is the product of the number of levels of the individual inverters or

$$n = \prod_{i=1}^{p} n_i. \quad (8)$$

As the number of levels is increased in a particular design, the power quality is improved which may be seen by an increase in the number of voltage vectors in the q-d plane [3]. The number of voltage vectors for a given number of levels can be calculated from

$$n_{\mathrm{vec}} = 3n(n-1) + 1. \quad (9)$$

In the following sections, specific examples of the generalized topology are considered.

A. Three-Level H-Bridge Cells

Fig. 2 shows the *a*-phase of a cascaded H-bridge inverter utilizing two three-level cells. This structure may be related to Fig. 1 by noting the points labeled a and g. The *b*- and *c*-phases are identical to the *a*-phase. Herein, cascaded H-bridge inverters

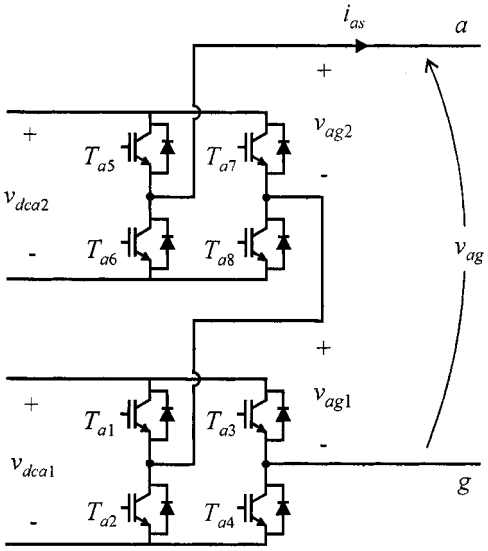

Fig. 2. Cascade-3/3H topology.

will be designated according to the voltage levels of the individual H-bridge cells. Under this labeling scheme, the inverter of Fig. 2 will be referred to as a Cascade-3/3H inverter. This is the topology originally patented by Robicon [6] and is a popular power converter for motor drives [6], [9], [15], [18], power supplies [7], [13], [17], and ac power systems [8], [11], [12], [14], [16]. In terms of the general mathematical description, it can be noted that $p = 2, n_1 = 3$, and $n_2 = 3$. If the dc voltage

TABLE I
CASCADE-3/3H STATES
($v_{\mathrm{dc}x1} = v_{\mathrm{dc}x2} = E$)

v_{ag}	v_{ag1}	v_{ag2}
0	E	-E
	0	0
	-E	E
E	E	0
	0	E
$2E$	E	E

TABLE II
CASCADE-3/3H STATES ($v_{\mathrm{dc}x1} = 3v_{\mathrm{dc}x2} = 3E$)

v_{ag}	v_{ag1}	v_{ag2}
0	0	0
E	0	E
$2E$	$3E$	-E
$3E$	$3E$	0
$4E$	$3E$	E

of each cell is set to the same value ($v_{\mathrm{dc}x1} = v_{\mathrm{dc}x2} = E$), then the resulting inverter can operate with five voltage levels. Table I shows the zero and positive voltage levels obtainable from this inverter as well as the voltage levels from the individual H-bridge cells. As can be seen, positive levels of E and $2E$ are possible output voltages as well as 0. Due to the inverter symmetry, it is also possible to have negative output voltages of $-E$ and $-2E$ for a total of five voltage levels. The negative voltage levels are excluded in Table I for compactness. From Table I, it can be seen that there are three redundant possibilities for switching to $v_{\mathrm{ag}} = 0$ and two possibilities for $v_{\mathrm{ag}} = E$. It will be shown below that the amount of redundancy will decrease as the power quality is increased.

According to (7) the number of voltage levels can be maximized if $v_{\mathrm{dc}x1} = 3v_{\mathrm{dc}x_2}$. Furthermore, it should be possible to achieve nine voltage levels according to (8). Table II shows the details of nine-level operation with $v_{\mathrm{dc}x1} = 3v_{\mathrm{dc}x2} = 3E$.

It is evident by the absence of redundancy in Table II that this operation fully utilizes the voltage level capability of this structure. However, the lack of redundancy may be problematic if the inverter is supplied from transformer/rectifier sources. As an example, consider switching state $v_{\mathrm{ag}} = 2E$ where $v_{\mathrm{ag2}} = -E$. It is likely in inverter operation that the current i_{as} would be positive when $v_{\mathrm{ag2}} = -E$ causing current to flow into the isolated source $v_{\mathrm{dc}a2}$. since transistors T_{a6} and T_{a7} are gated on for this state. Due to this problem, nine-level performance may not be achievable in all applications.

Although it may not be possible to utilize the maximum number of voltage levels in this inverter, it is possible to improve the power quality by utilizing a voltage ratio of $v_{\mathrm{dc}x1} = 2v_{\mathrm{dc}x2}$ which results in seven-level performance [23]. Table III shows the zero and positive switching states for the case where $v_{\mathrm{dc}x1} = 2v_{\mathrm{dc}x2} = 2E$.

With the redundancy reinstated, a choice exist for the state $v_{\mathrm{ag}} = E$ which can be made according to the direction of i_{as} so as to avoid current flowing into the positive terminal of a rectifier source. Although there is no redundant state for $v_{\mathrm{ag}} = 3E$, it is unlikely that the phase current would be negative when the phase voltage is near its peak in an inverter application.

TABLE III
CASCADE-3/3H STATES ($v_{\mathrm{dc}x1} = 2v_{\mathrm{dc}x2} = 2E$)

v_{ag}	v_{ag1}	v_{ag2}
0	0	0
E	0	E
	$2E$	-E
$3E$	$2E$	E

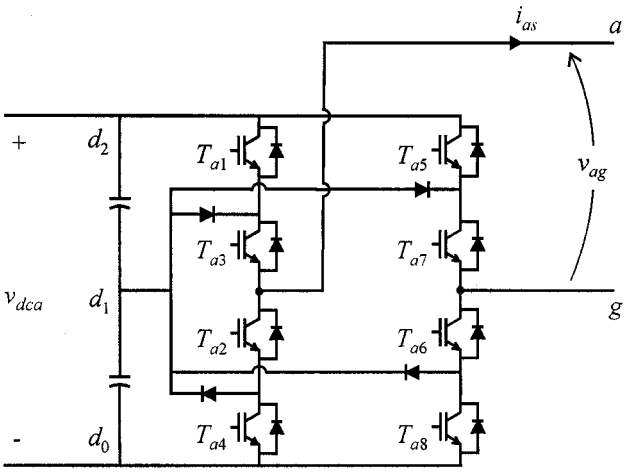

Fig. 3. Five-level H-bridge inverter.

B. Multilevel H-Bridge Cells

Fig. 3 shows an example of a multilevel H-bridge inverter which is constructed from two halves of a diode-clamped inverter connected to the same bank of series capacitors. As in Fig. 2, only the *a*-phase is shown since the *b*-phase and *c*-phase have identical structures. This topology is presently being produced by General Electric in their Innovation Series [18]. Although the inverter in Fig. 3 is a five-level structure, the concept may be expanded to any odd number of voltage levels [5].

By suitable switching of the inverter transistors, the points *a* and *g* in Fig. 3 may be connected into any of the points d_0, d_1, and d_2 [5]. Assuming that the dc voltage is set to $v_{\mathrm{dca}} = 2E$ and each capacitor remains charged to half of the dc voltage, the inverter output voltage v_{ag} may be set to the five distance levels $-2E, -E, 0, E$, and $2E$.

Capacitor voltage balancing in this topology may be accomplished in a straightforward way through redundant state selection [2]. As can be seen from Fig. 3, switching to output voltages of $-2E, 0$, and $2E$ will not result in current draw from the neutral point d_1 and therefore will not effect the capacitor voltage balance. However, when a voltage of $-E$ or E is required, the neutral junction will be utilized. As an example of how the redundant state switching is accomplished, consider the case where an output voltage of E is desired and the phase current i_{as} is positive. One possibility is to switch the point a to junction d_2 and the ground *g* to d_1. This choice will tend to charge the lower capacitor sine the current is flowing into the neutral junction. The other possibility is to switch the point a to junction d_1 and the ground *g* to junction d_0. This will result

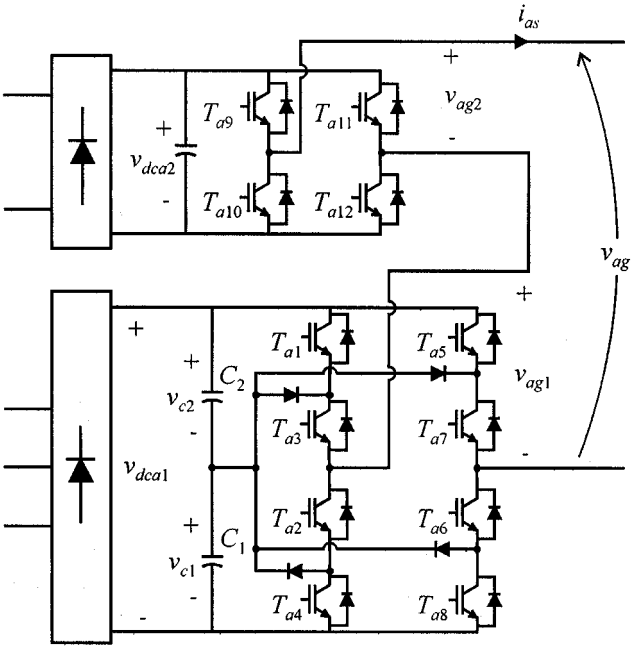

Fig. 4. Cascade-5/3H inverter topology.

TABLE IV
CASCADE-5/3H STATES> ($v_{\mathrm{dc}\,x1} = 6v_{\mathrm{dc}\,x2} = 6E$)

v_{ag}	v_{ag1}	v_{ag2}
0	0	0
E	0	E
$2E$	$3E$	$-E$
$3E$	$3E$	0
$4E$	$3E$	E
$5E$	$6E$	$-E$
$6E$	$6E$	0
$7E$	$6E$	E

in a current out of the neutral junction which will discharge the lower capacitor. The choice can then be readily made depending on whether the lower capacitor is under- or over-charged relative to the upper one.

C. Cascaded Multilevel H-Bridge Inverters

As stated above, the purpose of this paper is to introduce the general idea of cascading any number of multilevel H-bridge cells each having an arbitrary number of voltage levels and a unique dc voltage. The simplest example which demonstrates this is the cascade-5/3H inverter shown in Fig. 4 where the five-level inverter from the previous section is cascaded with a three-level H-bridge cell. Rectifier dc sources are shown in Fig. 4 in order to correspond to the laboratory system which will be described in a later section. In terms of the general mathematical description, $p = 2, n_1 = 5$, and $n_2 = 3$. According to (7), the voltage ratio which yields the maximum number of voltage levels is $v_{\mathrm{dc}\,x1} = 6v_{\mathrm{dc}\,x2}$ which will yield 15-level performance according to (8). By setting $v_{\mathrm{dc}\,x1} = 6v_{\mathrm{dc}\,x2} = 6E$, the 15-level output voltages may be expressed in terms of the individual inverter cells as shown in Table IV.

As with the cascade-3/3H inverter, the maximum power quality will not be obtainable if $v_{\mathrm{dc}\,x1}$ is a nonregenerative source (such as a transformer/rectifier source). In this case, the number of voltage levels must be reduced in order to re-gain switching state redundancy. The next lowest dc voltage ratio that will produce even voltage steps in this topology is $v_{\mathrm{dc}\,x1} = 4v_{\mathrm{dc}\,x2}$. Table V shows the H-bridge cell output voltages for this case.

TABLE V
CASCADE-5/3H STATES ($v_{\mathrm{dc}\,x1} = 4v_{\mathrm{dc}\,x2} = 4E$)

v_{ag}	v_{ag1}	v_{ag2}
0	0	0
E	0	E
	$2E$	$-E$
$2E$	$2E$	0
$3E$	$2E$	E
	$4E$	$-E$
$4E$	$4E$	0
$5E$	$4E$	E

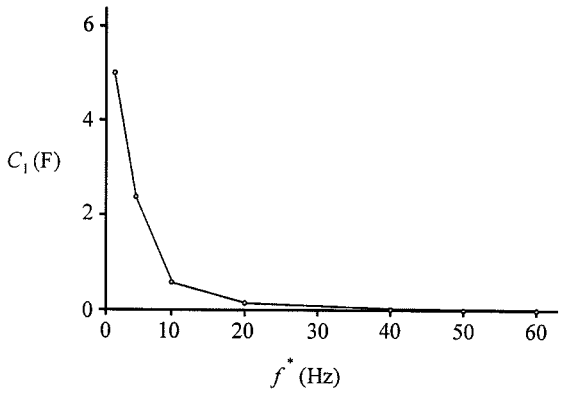

Fig. 5. Required dc bus capacitance versus frequency.

With the switching states shown in Table V, the performance has been reduced from its maximum of 15-level to 11-level. However, a choice between the E and $-E$ output voltages can be made at the appropriate times in order to ensure positive average current draw from a rectifier source supplying $v_{\mathrm{dc}\,x2}$.

At this point, some practical aspects of cascaded multilevel inverters will be discussed. One disadvantage of series H-bridge type inverters is that the dc supplies feed one phase of the inverter. The resulting capacitor voltage ripple is then twice the fundamental frequency and can be large in magnitude; especially at low fundamental frequencies. In order to illustrate this point, a detailed simulation of the cascade-5/3H system was created. The capacitance C_1 and C_2 (as labeled in Fig. 4) were varied together in order to maintain 0.75% voltage ripple in $v_{\mathrm{dc}\,a1}$ for a range of commanded fundamental frequencies f^*. Fig. 5 shows the simulation results. As can be seen, the capacitance required becomes unreasonably large at low frequencies. At 60 Hz, a value of $C_1 = C_2 = 3\,300\,\mu$F is needed, and at 2 Hz, the capacitance should be $C_1 = C_2 = 5$ F. However, it should be pointed out that the magnitude of the inverter ac commanded voltage in this simulation was held constant. In systems where the commanded voltage is lowered with frequency, the required capacitance may not be an issue.

Another aspect of the cascaded multilevel inverter proposed herein is that dc sources of different values must be provided.

For voltage isolation, it is preferable to have dc sources of the same value. However, cascaded H-bridge inverters using separate dc voltages have been constructed with dc voltage levels up to 3 kV [21] for high-power industrial drive applications. In general, cascaded multilevel inverters can be utilized in medium-voltage drives as has been demonstrated by Robicon Group [6] and General Electric [18]. Other applications include Naval ship and submarine propulsion [5].

III. Multilevel Voltage-Source Modulation

The objective of voltage-source modulation methods is to obtain commanded load voltages. Typically, the commanded voltages are a three-phase set that may be represented by

$$v_{\rm as}^* = mv_{\rm dc}\cos(\theta_c) \tag{10}$$

$$v_{\rm bs}^* = mv_{\rm dc}\cos\left(\theta_c - \frac{2\pi}{3}\right) \tag{11}$$

$$v_{\rm cs}^* = mv_{\rm dc}\cos\left(\theta_c + \frac{2\pi}{3}\right) \tag{12}$$

where $v_{\rm dc}$ is the total dc voltage available, or

$$v_{\rm dc} = \sum_{i=1}^{p} v_{{\rm dc}\,xi}. \tag{13}$$

The modulation index m controls the voltage magnitude and has a range of 0 to 1. Additionally, a third harmonic term may be commanded to extend the output voltage range [5]. In (10)–(12), θ_c is the converter electrical position which may be related to a desired fundamental frequency by

$$\theta_c = 2\pi f^* t. \tag{14}$$

Commanded voltages are obtained by first defining a three-phase set of duty cycles which will be offset so that they range from 0 to 100%. In particular, the duty cycles are defined herein as

$$d_a = \frac{1}{2}[1 + m\cos(\theta_c)] \tag{15}$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right)\right] \tag{16}$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right)\right]. \tag{17}$$

The duty cycles defined by (15)–(17) can be compared to a set of $(n-1)$ high-frequency triangle waveforms in order to produce a generalized switching state for each phase [5]. An example of this is shown in Fig. 6. In this example, the *a*-phase duty-cycle is compared to ten triangle waveforms in order to produce an 11-level switching state s_a which has a range of 0 to 10 [3]. Similarly, the *b*- and *c*-phase duty cycles are compared to the same triangle waveforms to produce switching states $s_{\rm b}$ and $s_{\rm c}$. As a final step, the generalized switching states from the modulation method are related to the switching of the individual inverters. First, it can be noted that the *a*-phase line-to-ground voltage resulting from the modulator switching state is

$$v_{\rm ag} = \left[s_a - \left(\frac{n-1}{2}\right)\right] E \tag{18}$$

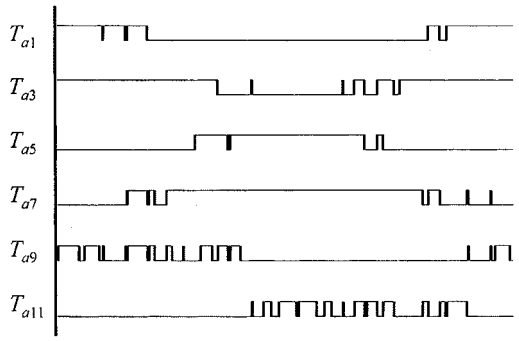

Fig. 6. Eleven-level inverter transistor signals.

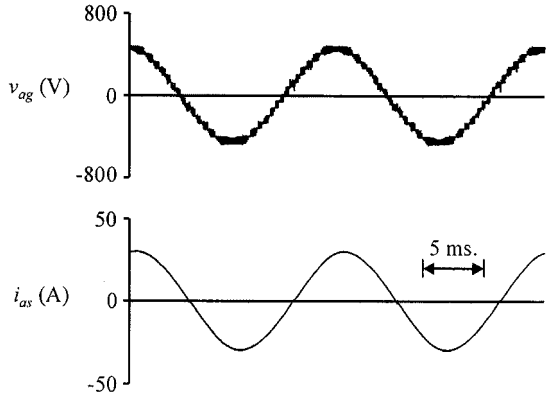

Fig. 7. Cascade-5/3H inverter laboratory measurements (demonstrating 15-level performance).

if $v_{{\rm dc}\,x2}$ is given the value of E. Once this is known, the 11-level switching table (Table V) can be used to determine the switching of the individual inverter cells. For laboratory implementation, the table (along with redundant state selection necessary to balance capacitor voltages and ensure positive dc source currents) may be programmed into an erasable programmable logic device (EPLD) or included in the DSP code. This table can also map the switching states to individual transistor signals according to typical multilevel inverter operation [3]. Fig. 6 also shows the transistor signals for a cascade-5/3H inverter operating in the 11-level mode as predicted by a detailed simulation. In this example, the fundamental frequency is $f^* = 60$ Hz and the triangle waveform frequency was set to a relatively low value of 2.4 kHz in order to clearly illustrate the switching. The resulting transistors signals are shown for the odd number transistors. Even numbered transistor gating signals are the complement of the odd numbered signals.

IV. Laboratory Validation

In order to validate the proposed concept, the inverter of Fig. 4 was constructed and tested in both the 15-level and 11-level modes. For the 15-level mode, a single-phase resistive-inductive load with parameters $R = 14.9\,\Omega$ and $L = 11.65$ mH was connected to the output voltage $v_{\rm ag}$. The dc voltage $v_{{\rm dc}\,a2}$ was supplied by a battery source and had a voltage of 72 V. The dc voltage $v_{\rm dca1}$ was supplied by a transformer/rectifier source and set to 432 V in accordance with (7). The capacitance value of

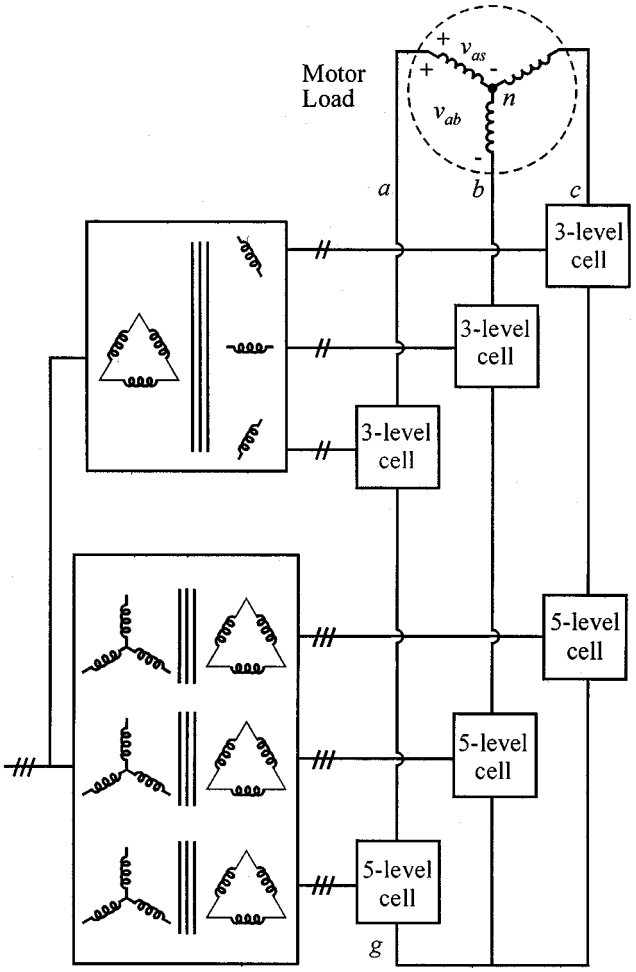

Fig. 8. Laboratory system diagram for 11-level inverter.

this source was $C_1 = C_2 = 3\,300\ \mu$F. The modulation parameters for this study were $m = 0.91$ and $f^* = 60$ Hz. In this study, redundant state selection balancing was implemented for the capacitor voltages on the five-level H-bridge cell. Fig. 7 shows the resulting load voltage $v_{\rm ag}$ and current $i_{\rm as}$. As can be seen, fifteen voltage levels are present yielding a outstanding power quality.

The next study involved utilization of transformer/rectifier sources to supply all dc voltages and verification of 11-level operation. Fig. 8 shows a full system diagram of the system. Therein, the three-level and five-level cells contain a rectifier and inverter as shown in Fig. 4. As can be seen, each five-level cell is supplied by a separate three-phase transformer. The three-level cells are supplied from the individual phases of a three-phase transformer in a similar manner as described in [6]. The load for this study was a 5.2 kW three-phase induction motor. The dc voltages were set to $v_{{\rm dc}x1} = 260$ V and $v_{{\rm dc}x2} = 65$ V. The modulation parameters were the same as in the 15-level study. Fig. 9 shows the motor *a*-phase line-to-line voltage $v_{\rm ab}$ and *a*-phase current $i_{\rm as}$. The voltage and current THD's in this study were 6.83% and 3.74%, respectively. Although the power quality is not as high as the 15-level case, it is still considerably high when compared to the cascade-3/3H inverter which uses the same number of isolated dc sources. It should also be pointed out that the power quality may be further increased without increasing the number of isolated dc sources by using cells with

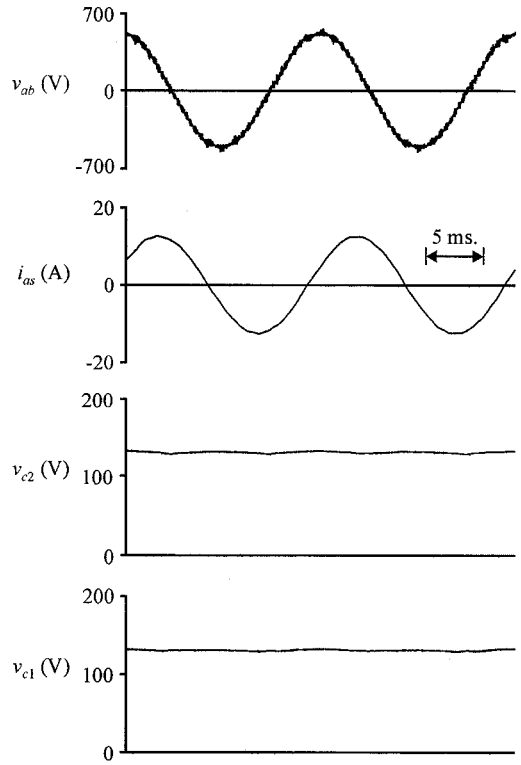

Fig. 9. Cascade-5/3H inverter laboratory measurements (demonstrating 11-level operation).

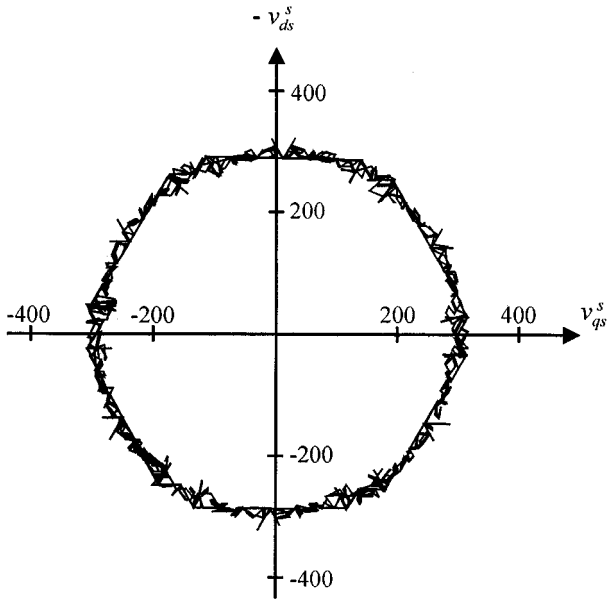

Fig. 10. Cascade-5/3H measured voltage vector diagram.

a higher number of voltage levels (such as a cascade-5/5H inverter).

The lower and upper capacitor voltages on the *a*-phase five-level cell are also shown in Fig. 9. Fig. 10 shows the voltage vector plot from this study which was obtained by transforming the inverter line-to-ground voltages to the stationary q-d reference frame according to (2)–(6). From (9), it can be determined that there are 331 voltages vectors available for this inverter. The high number of voltage vectors leads to a utilization of voltage

vectors in a nearly perfect circular pattern when compared to that of inverters with a lower number of voltage levels [3].

V. Conclusion

This paper has presented the concept of using multilevel H-bridge cells in cascaded inverters. This concept, as well as supplying each cell with a unique dc voltage, can result in a high number of voltage levels. However, it was shown that in some cases the power quality must be lowered slightly in order to ensure that the current drawn from transformer/rectifier sources remains positive. The new inverter was experimentally verified by cascading a five-level H-bridge cell with a three-level H-bridge cell. Fifteen-level performance was achieved when using a battery source for the three-level cell. Operation of the three-level cell from a rectifier source required that the overall voltage levels be reduced to 11-level. For this inverter, a line-to-line voltage THD of 6.83% was obtained.

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