A New Cascaded Multilevel Inverter Topology with Galvanic Isolation

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Abstract— This paper presents a new compact three-phase cascaded multilevel inverter (CMLI) topology with reduced device count and high frequency magnetic link. The proposed topology overcomes the predominant limitation of separate DC power supplies, which CMLI always require. The high frequency magnetic link also provides a galvanic isolation between the input and output sides of the inverter, which is essential for various grid-connected applications. The proposed topology utilizes an asymmetric inverter configuration that consists of cascaded H-bridge cells and a conventional three-phase two-level inverter. A toroidal core is employed for the high frequency magnetic link to ensure compact size and high-power density. Compared with counterpart CMLI topologies available in the literatures, the proposed inverter has the advantage of utilizing the least number of power electronic components without compromising the overall performance, particularly when a high number of output voltage levels is required. The feasibility of the proposed inverter is confirmed through extensive simulation and experimentally validated studies.

Keywords— Cascaded multilevel inverter, Isolated dc-supply, Asymmetric multilevel inverter, High frequency magnetic link.

I. INTRODUCTION

One of the key features of cascaded multilevel inverter (CMLI) topologies is the ability to generate high voltage through utilizing low rated power electronic devices. As such, CMLIs have been given much attention in renewable energy systems and industrial applications [1-4].

A general topology of CMLI comprises a number of cascaded cells along with an isolated and balanced dc-supply for each cell [5, 6]. The number of cascaded cells increases as the number of the desired output voltage levels increases. Therefore, it becomes quite challenging to manage the isolated balanced dc-supplies while achieving higher number of levels in the output voltage waveforms. Based on the magnitudes of the dc-supplies connected to the cascaded cells, CMLI can be categorized into symmetric (equal magnitudes) or asymmetric (unequal magnitudes) structures. The performance of asymmetric CMLI is found to be superior than symmetric structure in terms of output voltage levels when the same number of semiconductor switches and dc power supplies are utilized [7]. For example, H-bridge based symmetric modular multilevel converter (MMC) presented in [8-11] generates less number of output voltage levels when compared with the asymmetric MMC presented in [12, 13].

Currently, power frequency-based classic transformers are employed to provide the required galvanic isolation between the multilevel inverter (MLI) and the grid [14, 15]. The size and weight of the transformer would be considerable for MLI-based medium voltage applications [9]. Recently, high frequency magnetic link (HFML)-based power converters have become more popular due to their high power density, compact size, cost effectiveness and high reliability [16]. For example, an HFML-based power converter comprising a small toroidal core (8 cm internal diameter and 14 cm external diameter) was utilized in a 100-kW power converter [17]. Several high frequency magnetic core materials such as Hitachi, Finmet and Metglas have been proposed in the literatures aiming at improving the overall performance of HFML-based power converters [18]. The utilization of HFML facilitates the implementation of CMLIs with a single dc-source while maintaining a high number of output voltage levels. In [17], HFML-based CMLI is realized using multi-winding toroidal magnetic core for a cascaded H-bridge multilevel inverter. In this topology, the CMLI generates 27-levels in the output voltage waveforms through utilizing one dc-source at the primary side and multiple windings at the secondary side of the HFML. Although, HFML enables CMLI to operate with a single dc-source, the problem related with tripling power electronic components for three-phase structure cannot be avoided.

Extensive research has been conducted to develop new CMLI topologies to comply with specific requirements and applications [19, 20]. Device count, simple structure, physical size, number of levels in the output voltage waveform and cost effectiveness are crucial factors that should be considered while proposing a new CMLI topology [21, 22]. Various single phase CMLI topologies have been proposed in the literatures [5, 23-26]. When extending such single phase topologies to three phase structures, the number of devices is to be tripled which eventually increases the design complexity, cost and physical size of the resultant three phase inverter [13, 17, 27-35].

In this paper, a new concept for HFML-based CMLI that can be employed for three phase applications is proposed. The main feature of the proposed concept is the flexibility to extend the single-phase inverter to three-phase structure without tripling the power electronic components as the case with the current topologies proposed in the literature [13, 17, 27-35].

The rest of the paper is organized as follows: the proposed topology is presented in section II while section III presents the detailed design for the HFML. Experimental and simulation analyses along with discussion are presented in section IV. The potential applications of the proposed CMLI are highlighted in section V. Comparison with other topologies is presented in section VI. The main conclusions are drawn in section VII.

II. Proposed Cascaded Multilevel Inverter

The proposed CMLI consists of HFML, full-bridge rectifiers along with compact cascaded MLI as shown in Fig. 1(a). The HFML comprises a single dc-source connected to a high frequency (20 kHz) square wave voltage generator that energizes the primary winding of a toroidal multi-winding transformer (MWT). The multiple windings on the secondary side of the MWT provide the isolated dc voltages required to create various levels in the output voltage. As can be seen from Fig. 1(a), the MLI has two main stages: cascaded stage and conventional three-phase, two-level inverter stage. The cascaded stage consists of two H-bridge (CHB) cells. While the three-phase two-level inverter is implemented using a conventional well-known structure [36], the cascaded stage can be any cascaded inverter topology proposed in the literature. The voltages generated by the cascaded stage are transferred to the output terminals, A, B, C through Bi-directional (BD) switches. More cascaded cells can be added as required to increase the number of levels in the output voltage waveforms.

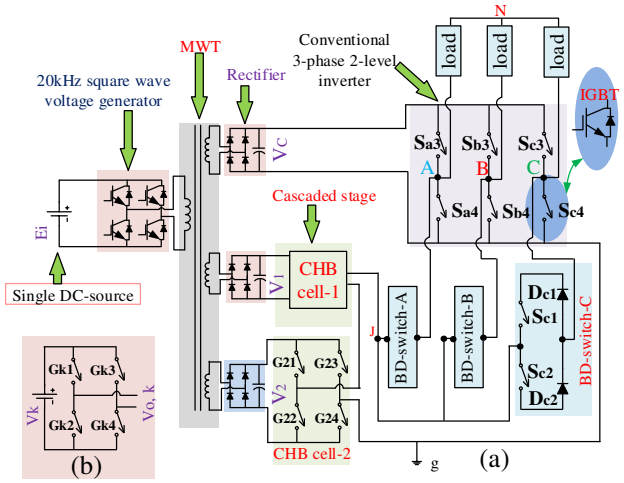


Fig.1 Proposed cascaded multilevel inverter, (a) Proposed inverter when H-bridges are considered as cascaded cells, (b) A basic H-bridge

The input voltages to the H-bridge celles can be adjusted by controlling the MWT turns ratio. If '*n*' number of H-bridge cells are considered in the cascaded stage, then the equal magnitudes of the CHB input voltages can be expressed by

$$V_1=v;\ V_2=v;\ \ldots\ldots;\ V_n=v \qquad (1)$$

Binary or trinary related input dc-supplies to the H-bridge cells can also be adopted, which is expressed by:

$$V_1=v;\ V_2=2^1v;\ \ldots\ldots;\ V_n=2^{n-1}v \qquad (2)$$

$$V_1=v;\ V_2=3^1v;\ \ldots\ldots;\ V_n=3^{n-1}v \qquad (3)$$

The conventional three-phase, two-level inverter is fed by a dc-supply of a magnitude of *Vc* that should be higher than the summation of all input dc voltages of the CHB cells. Hence V_C can be calculated from,

$$V_C = \sum_0^n V_x + V_1 = (V_1 + V_2 + \cdots + V_n) + v \qquad (4)$$

A key feature of the proposed topology is that it allows for replacing the cascaded stage in Fig. 1(a) by any existing cascaded MLI topology for developing a new three-phase cascaded MLI without tripling the number of device count required for MLI single-phase structure.

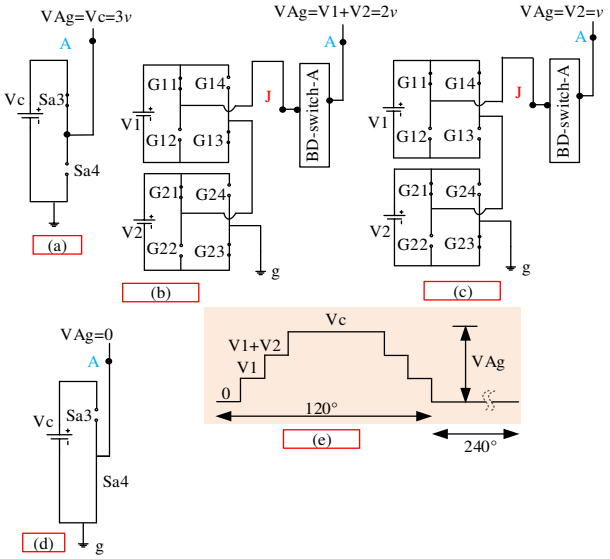


Fig. 2 Switching logics for generating four levels in the pole voltages: (a) level 3*v*; (b) Level 2*v*; (c) Level *v*; (d) Level 0; (e) Complete cycle of the pole voltage

The conventional three-phase, two-level inverter has three-phase legs. Each leg comprises two switches, (S_{a3}, S_{a4}), (S_{b3}, S_{b4}), (S_{c3}, S_{c4}) operating in a toggle mode to generate two voltage levels (V_C and zero) in the pole voltages, V_{Ag}, V_{Bg}, V_{Cg}. Similar switching logic is applied for the three legs with a 120^0 phase shift.

The output points, *A, B, C* of each phase leg are connected to BD-switches as shown in Fig. 1(a). Each BD-switch consists of two Insulated Gate Bipolar Transistors (IGBT) and two diodes. All voltage levels between V_C and zero are produced in the pole voltages by the cascaded stage when the BD-switches are turned on (BD-switch is considered to be 'on' when both of the IGBTs are switched on). Fig. 1(b) shows an H-bridge cell which comprises four switches (G_{K1}, G_{K2}, G_{K3}, G_{K4}) and a dc-input supply, V_K. Each H-bridge cell is able to generate three voltage levels, 0, $\pm V_K$ in the output voltage, $V_{O,K}$.

It is worth noting that switches in the conventional three-phase, two-level inverter are completely turned off while generating voltage levels between V_C and zero. If same input voltages to the H-bridge cells are considered, then according to (1) and (4) the input voltages to the H-bridge cells and the conventional three-phase, two-level inverter can be expressed by,

$$V_1=V_2=v,\ V_C=3v \qquad (5)$$

The switching logics for generating different levels as shown in Fig. 2 reveal that the cascaded stage has no contribution in generating the V_C and 0-levels in the pole voltage V_{Ag} (Figs.

2(a), (d)). On the other hand, levels '2v' and 'v' in the pole voltage are generated when the BD-switches in the conventional three-phase, two-level inverter are turned on and H-bridge cells contributes, as shown in Figs. 2(b) and (c), respectively. Both switches, Sa3 and Sa4 in phase leg-A of the conventional three-phase, two-level inverter are turned off while generating '2v' and 'v' voltage levels. The switching logics are applied for 120^0 to create four voltage levels: 3v, 2v, v, 0 during ascending and descending modes of the pole voltage waveform, V_{Ag} as shown in Fig. 2(e). The cascaded stage utilizes the same switching logic to generate the three phase pole voltages V_{Ag}, V_{Bg} and V_{Cg} with a 120^0 phase shift between them.

The line voltages, V_{AB}, V_{BC}, V_{CA} are derived from the pole voltages as per the following equation,

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \end{bmatrix} \quad (6)$$

The proposed cascaded MLI topology is controlled by a low frequency staircase modulation technique [37, 38]. The designated switching states for generating four levels in the pole voltage waveform can be presented in a hexagonal form within the d-q plane as shown in Fig. 3. If the number of levels in the pole voltages is N_p, then there will be 6(N_p-1) number of switching states [37, 38].

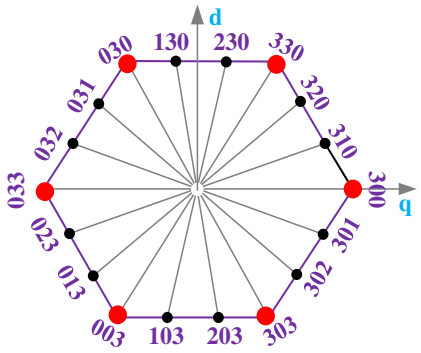


Fig. 3 Switching vectors in d-q complex plane of 18 switching states for generating four levels, N_p=4 in the pole voltage

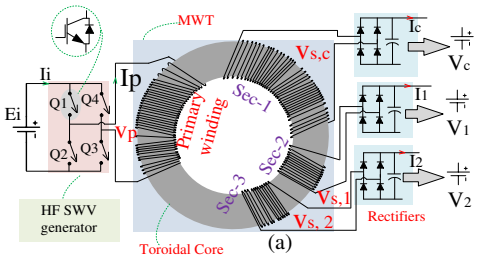
Hence for generating 4 levels in the pole voltage, there will be 18 switching states as shown in Fig. 3. Each of the switching state has three switching vectors, S_A, S_B, S_C for three phase voltage generation. The pole voltages are taken as reference to achieve the three switching vectors in each switching state at any instant of time [37]. In general, the switching angles for all switching states are equal and can be expressed as,

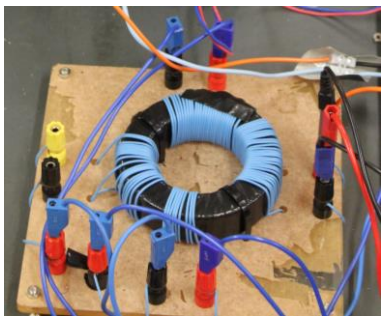
$$\text{Switching angle} = 360^0/6(N_P\text{-}1) \quad (7)$$

Thus the switching angle for each of the 18 switching states is 20^0 which means, a new switching state comes into operation every 20^0. In the switching sequence of the 18 switching states, the switching vectors 3, 2, 1, 0 are combined in an organised manner to generate three phase pole voltages.

III. HF-MAGNETIC LINK DESIGN

The square wave voltage (SWV) generator is made of four insulated gate bipolar transistor, HGTG20N60B3D, 600V/40A, four IGBT gate driver circuits and a digital signal processor (DSP), TMS320F2812. The SWV generator converts the input 240-volt dc into a square wave high frequency voltage which is fed into the primary winding of the MWT as shown in Fig. 4(a). The two pairs of switches, (Q1, Q3) and (Q2, Q4) in the SWV generator are operated in toggle mode to generate the 240 volt, 20 kHz square wave voltage. The number of secondary windings is identified based on the required number of the isolated dc-supplies. Three secondary windings are used in the developed inverter as shown in Fig. 4(a). The magnitude of the conventional inverter input dc voltage, V_C would be '3v', if the input dc voltages to the cascaded cells are maintained at the same voltage level of v by adjusting the MWT turns ratio to be 3:3:1:1. Fig. 4(b) shows the prototype of the MWT, which is made of a ferrite toroidal core.





(b)

Fig. 4 High frequency magnetic link: (a) multiple isolated dc supplies management from a single dc source, (b) Prototype of the laboratory MWT

A. *Toroidal Transformer Winding Wire Selection*

The ac resistance of the transformer windings is increased due to the skin and proximity effects, while operating with high frequency voltage and current. Multi-strained wire is utilized to reduce these effects. The diameter (d) of the conductor in the transformer primary and secondary windings depends on the load demand and can be calculated based on winding current (I), current density (J) and number of strains in the winding (S_n) as [25]:

$$d = \sqrt{\frac{4I/S_n}{\pi J}} \quad (8)$$

For simplicity, 100 copper strains of 0.5mm^2 cross-sectional area is chosen for the primary and secondary windings of the toroidal transformer. Multi-strain litz wire can be utilized in the

transformer primary and secondary windings to maximize the current rating while minimizing the skin and proximity effects [18]. Moreover, the primary winding can also be split into multiple parallel windings to reduce the excitation current [39]. Fig. 5 shows a schematic diagram for a possible MWT arrangement that has *m*-number of primary windings and (*n*+1) number of secondary windings. The square voltage wave generator (SWVG) in the primary side can be fed by any dc source that can be battery bank or photo voltaic (PV)-array [9].

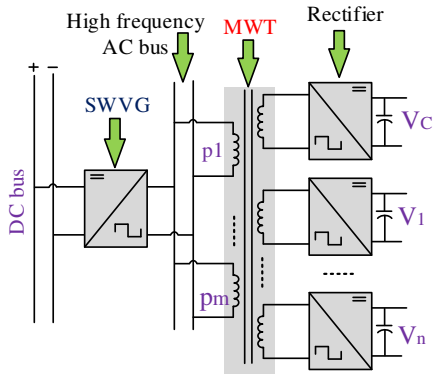


Fig. 5: Basic structure of MWT with multiple primary windings

The transformer leakage inductance is another key parameter that should be considered while designing the HFML. Analysis on the transformer leakage inductance for high and medium frequency operated MWT can be found in [39, 40]. According to [39], the excitation current and output power of a multi-winding transformer are inversely proportional with the leakage inductance. Hence optimum selection for the leakage inductance should be carefully made in order to maintain the excitation current below the windings rated value while achieving a desired level of the output power. In the developed prototype, the maximum excitation current was 2A and the rated output power is 250VA.

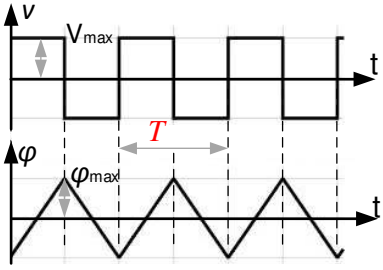


Fig. 6 Square wave voltage and flux in a toroidal transformer

B. Number of Turns and core selection

The HFML performs with a SWV, hence according to Faraday's law, the generated magnetic flux (φ) in the core would be a triangular waveform as depicted in Fig. 6, where T, V_{max} and φ_{max} are the time-period, maximum voltage and magnetic flux, respectively.

For a complete cycle of the SWV, the triangular flux can be expressed as:

$$\varphi(t) = \begin{cases} \frac{\varphi_{max}}{\frac{T}{4}}\left(t - {}^{T}/_{4}\right), 0 \le t \le \frac{T}{2} \\ -\frac{\varphi_{max}}{{}^{T}/_{4}}\left(t - {}^{3T}/_{4}\right), \frac{T}{2} \le t \le T \end{cases} \tag{9}$$

According to Faraday's law, the correlation between the excitation voltage, $v(t)$ and the magnetic flux within a transformer winding of N-turns can be derived as below:

$$\begin{aligned} v(t) &= N\frac{d\varphi}{dt} = N\frac{d}{dt}\left[\begin{cases} \frac{\varphi_{max}}{{}^{T}/_{4}}\left(t - {}^{T}/_{4}\right), 0 \le t \le \frac{T}{2} \\ -\frac{\varphi_{max}}{{}^{T}/_{4}}\left(t - {}^{3T}/_{4}\right), \frac{T}{2} \le t \le T \end{cases}\right] \\ &= \begin{cases} N\frac{\varphi_{max}}{{}^{T}/_{4}}, 0 \le t \le \frac{T}{2} \\ -N\frac{\varphi_{max}}{{}^{T}/_{4}}, \frac{T}{2} \le t \le T \end{cases} \\ &= \begin{cases} V_{max}, 0 \le t \le \frac{T}{2} \\ -V_{max}, \frac{T}{2} \le t \le T \end{cases} \end{aligned} \tag{10}$$

The rms voltage of the square wave can be written as:

$$\begin{aligned} V_{rms} &= V_{max} = N\frac{\varphi_{max}}{{}^{T}/_{4}} \\ &= 4f\varphi_{max} = 4fNA_eB_{max} \end{aligned} \tag{11}$$

where A_e and B_{max} represent the cross-sectional area of the toroidal core and the magnetic flux density, respectively.

According to (11), the core area of the toroidal core is inversely proportional with the SWV frequency (20 kHz). Toroidal core FERROXCUBE, T102/66/25-3C90, with A_e= 445.32mm², B_{max}= 200 mT is utilized for the HFML. According to (11), for V_{rms} =240V, the least number of turns in the primary winding of the implemented toroidal transformer is N= 34. The primary winding of the developed HFML in this paper is designed with 36 turns to ease the calculation of the secondary winding turns. The two secondary windings connected to the CHB cells have the same turns' ratio with respect to the primary winding (3:1) while the winding connected to the conventional inverter via a full bridge rectifier comprises the same turns as the primary winding. The area occupied by the primary and the three secondary windings is 48 mm^2. The minimum hole-area (A_{min}) of the toroidal core is calculated by considering a clearance factor of 8 [17], which leads to a minimum hole-area, of 348mm^2. The chosen toroidal core is well suited for this design as it has 822.5mm^2 inner area with inner and outer diameters of 65.8 mm, 102mm and a thickness of 25mm. It is worth mentioning that although ferrite material has been widely utilized as toroidal core, some other magnetic materials such as Hitachi *Finmet*, and *Metglas* may provide better performance in terms of size, power capacity and efficiency [41].

Different parts of the laboratory scaled down prototype are shown in Fig. 7. Table 1 provides detailed specifications of various components of the developed proposed inverter topology. In the developed prototype, DSP TMS320F2812 control board is employed to generate the real-time gate pulses for the inverter switches. IGBT, HGTG20N60B3D, 600V/40A is utilized as the inverter switching device. Two IGBTs in each bidirectional switch require identical gate signals. Hence, DSP

generates nine-gate signals for the conventional three-phase, two-level inverter (CTPTLI) and the three BD-switches.

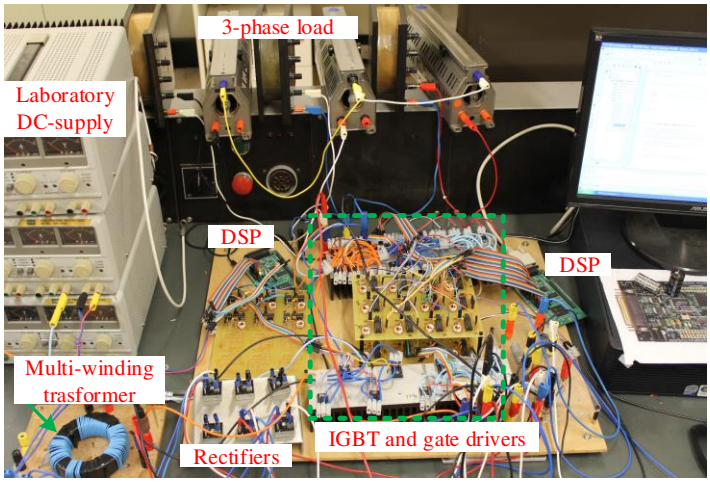


Fig. 7 Experimental prototype of the HF magnetic linked CMLI

TABLE 1 SPECIFICATIONS OF THE DEVELOPED SCALED DOWN TEST RIG

Transformer	Toroidal core material	FERROXCUBE, T102/66/25-3C90
	Turns in primary winding	36
	Turns in secondary winding-1	36
	Turns in secondary winding-2 & 3	12
Rectifier unit	Full bridge rectifier module	KBPC5010, 1kV, 50A
IGBT rating	Switching devices in the CHB and CTPTLI	HGTG20N60B3D, 600V/40A
Bi-directional switches	Switching device	HGTG20N60B3D, 600V/40A
	Power Diode	RHRP1540, 400V/15A
Gate pulse generator		(DSP), TMS320F2812
Connected load		115+j94.2 Ω/phase
Line voltage		240V (peak)
Voltage levels in the line voltage		7
Apparent power of the test rig		250 VA

IV. PERFORMANCE OF THE PROPOSED INVERTER

The performance of the proposed inverter under various loading and operating conditions is assessed as per the below case studies.

A. *Case study 1: Performance of the proposed inverter with constant impedance load*

Experimental analysis on the developed prototype is conducted while a balanced three phase load (Z=115+j94.2 Ω) is connected to each phase leg. Fig. 8(a) presents the gate pulses of different switches within the cascaded stage; BD-switch-A and a switch in phase leg-A of the conventional three-phase two-level inverter. The waveforms of the pole voltages show four levels (0, 80v, 160v, 240v), while the voltage at the junction point J in Fig. 1, V_{Jg} contains two levels (80v, 160v) as shown in Fig. 8(b). The line voltages comprise seven levels, (0, ±80v, ±160v, ±240v) in their waveforms as shown in Fig. 8(c) which also shows the line current, I_{AN} waveform.

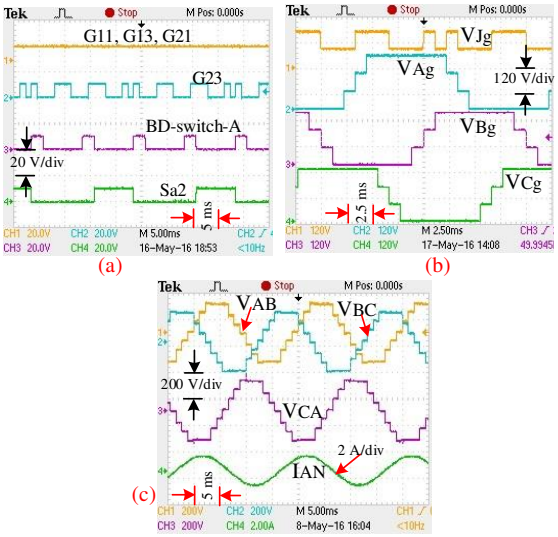


Fig. 8 Experimental waveforms of the proposed MLI with constant impedance load. (a) gate pulses for different switches in the H-bridge cells, BD-switch-A and a switch in conventional inverter within phase leg-A, (b) V_{Jg}, V_{Ag}, V_{Bg}, V_{Cg}, (c) line voltages (V_{AB}, V_{BC}, V_{CA}) and line current (I_{AN})

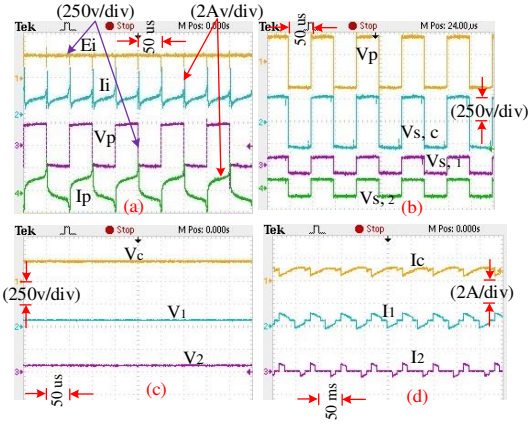


Fig. 9 Experimental performance with constant impedance load (a) input/output voltage/current (E_i, I_i, V_p, I_p) of the high frequency voltage generator, (b) primary, V_p and secondary voltages, (V_{sc}; V_{s1}; V_{s2}) of the toroidal transformer, (c) rectifier output voltages (V_C, V_1, V_2) and (d) rectifier output current (I_C, I_1, I_2)

Fig. 9(a) shows the experimental input and output waveforms of the SWV generator when the input dc voltage, E_i is maintained at constant level. Fig. 9(b) shows the high frequency voltage output from the primary and secondary sides of the MWT. The output voltages of the rectifier units are shown in Fig. 9(c) while the inverter input currents at the cascaded cells and conventional three-phase two-level inverter stage are shown in Fig. 9(d).

B. *Case study 2: Performance of the proposed inverter with intermittent input dc source*

In the experimental setup, a 'GW Laboratory dc power supply GPS-3030 is used as an input dc-power source for the SWV generator. For photo voltaic (PV) applications, a fluctuated input voltage to the MLI is expected due to the intermittent characteristics of the PV [42, 43]. To investigate the performance of the proposed inverter under such condition, voltage fluctuation is emulated using a programmable dc power

supply while keeping the load similar to the previous case study.

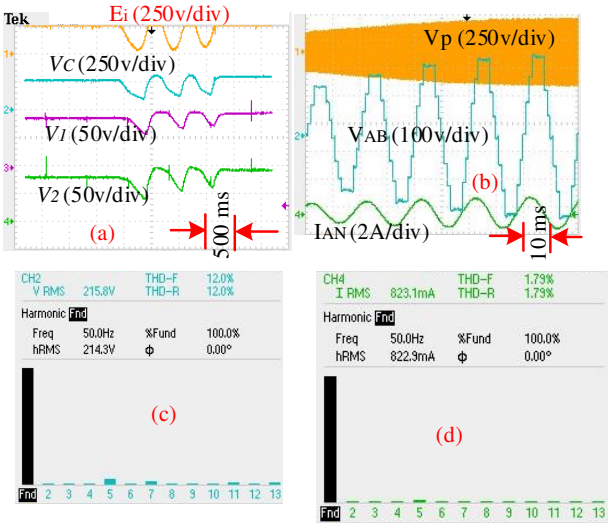


Fig. 10 Experimental performance with intermittent input dc source (a) input dc source voltage (E_i) and rectifier output voltages (V_C, V_1, V_2), (b) primary winding voltage of multi-winding transformer (V_p), line voltage (V_{AB}) and line current (I_{AN}), (c) line voltage THD and (d) line current THD

Fig. 10 shows the impact of input source voltage, E_i fluctuation on the line voltage and line current of the proposed CMLI. The MWT always keeps the same voltage ratio between primary and secondary windings. Consequently, the rectifier produces similar voltage profiles to the cascaded inverter regardless the fluctuation of E_i as shown in Fig. 10(a). While the magnitude of the cascaded inverter output line voltages and currents experience fluctuation, the number of levels in the inverter output voltage always remains unchanged as can be observed from Fig. 10(b). This constant level-generating phenomenon ensures no increment in the total harmonic distortion (THD) in the inverter output voltage and current waveforms during fluctuation events in the input dc voltage. As shown in Figs. 10(c) and (d), the line voltage waveforms exhibit 12% THD, while 1.79% THD is observed in the line current. The line voltage THD can be reduced to be less than 5% to comply with the IEEE standard [44] by increasing the number of levels. Nevertheless, the 12% THD in a 7-level inverter is quite low in comparison with other proposed cascaded MLI topologies producing the same number of levels in the output voltage waveform [31]. This key feature makes the proposed inverter topology a suitable candidate for voltage controlled motor drive applications in the machinery industry and electric vehicles.

C. *Case study 3: Performance of the proposed inverter considering load dynamics*

Inverter output voltage and current waveforms are observed during dynamic loading conditions. Fig. 11 shows the simulation results when a load of nearly unity power factor (PF) (100.31∠4.49°Ω per phase leg) changed at t=0.0325s to nearly 0.8 PF (127.13∠38.13°Ω per phase leg) that lasts for a duration of 0.0175s after which the original load is retained. Although a little distortion can be observed in the line current waveforms as shown in Fig. 11(b) during the transition period, no significant effect can be seen in the line voltage waveforms shown in Figs. 11(a).

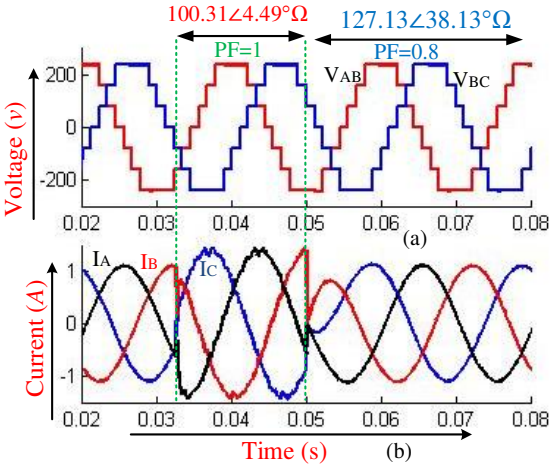


Fig.11 Simulation results for a dynamic change in the load from nearly unity PF (100.31∠4.49°Ω) to 0.8 lagging PF (127.13∠38.13°Ω): (a) line voltage waveforms, (b) line current waveforms

The performance of the proposed CMI is also observed for a change in the load magnitude with the same power factor. Fig. 12 shows the inverter line voltage and current waveforms when the magnitude of a nearly 0.8 PF lagging load (50.86∠38.15°Ω per phase leg) is doubled to 101.73∠38.15°Ω per phase leg at t=0.0325s for a duration of 0.0175s. Similar observations reported in the above case (Fig.11) can be noticed here.

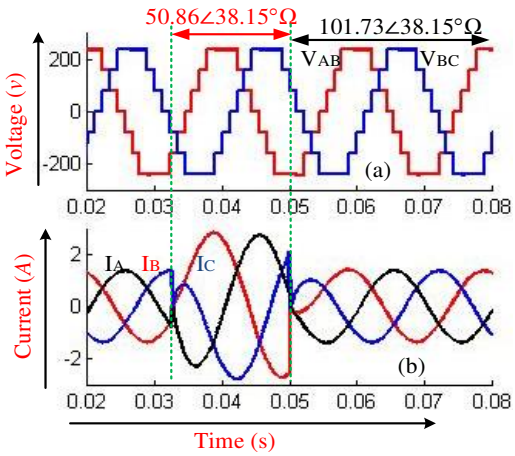


Fig. 12 Simulation results for a dynamic change in the load magnitude with the same PF: (a) line voltage waveforms, (c) line current waveforms

The above case studies reveal the feasible application of the proposed CMLI topology with renewable energy sources of intermittent characteristics and with loads of dynamic changes.

D. *Case study 4: Performance of the proposed inverter under asymmetric dc voltages*

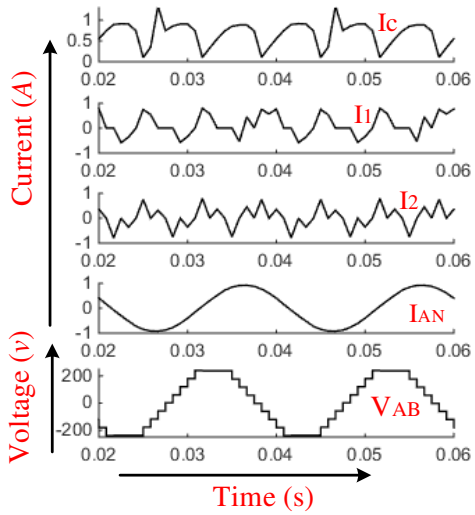


Fig. 13 Simulation results of rectifier output currents: I_C, I_1, I_2 and the MLI output voltage and current, V_{AB} and I_{AN} for asymmetric CHB input voltages

This case study is carried out to investigate the performance of the proposed CMLI under asymmetric rectifier output voltages. The asymmetric rectifier voltages are implemented by changing the transformer turns ratio from 3:3:1:1 to 4:4:2:1 in order to get asymmetric voltage magnitudes for V_1 and V_2. According to this turns ratio, the rectifiers output voltages will be: Vc= 240V, V_1=60V and V_2=120V. Fig.13 shows the rectifier output currents I_C, I_1, I_2 along with the MLI output voltage (V_{AB}) and current (I_{AN}) waveforms. As can be seen in the aforementioned figure, the number of levels in the MLI output voltage is increased to 9-levels since the H-bridge cascaded modules are now fed with binary-related input voltages (60V and 120V). This configuration achieves more levels in the output voltage waveform than symmetric CHB voltages as mentioned in the introduction section.

E. *Case study 5: Effect of unbalanced CHB input voltages*

The performance of the proposed inverter is also observed under unbalanced input voltages to the CHB cells. The imbalance may arise due to several factors including the ageing of the capacitors of the ripple filters connected to the rectifiers' terminals. In this case study, the voltage imbalance is created by adjusting the number of turns of the transformer two secondary windings connected to the CHB cells so that V_1=64V and V_2=96V. As can be seen in Fig. 14, the line voltage which comprises 7-levels and current waveforms do not exhibit observable change due to the unbalanced input dc voltages to the CHB cells. Also, no abnormal change can be seen in the rectifier output currents I_C, I_1 and I_2. This case study reveals the possible applications of the proposed CMLI topology in unbalanced dc voltage conversion systems.

It is worth noting that circulating current may arise within parallel-operation of voltage source inverters [10, 45, 46]. In the proposed topology, the inputs to the rectifier are magnetically isolated and they never operate in parallel at any switching state as shown in Fig. 2 and hence, no circulating current is expected for this configuration.

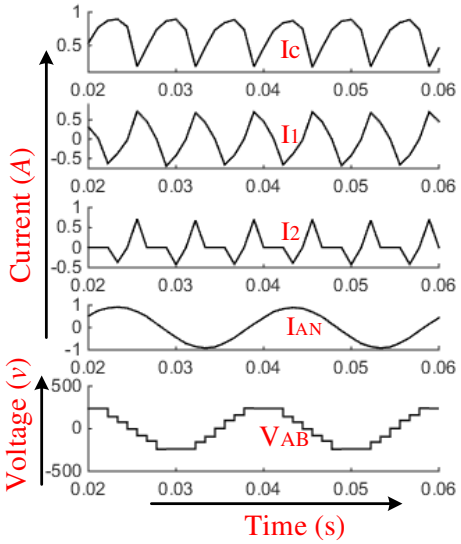


Fig. 14 Simulation results of rectifier output currents: I_C, I_1, I_2 and the MLI output voltage and current, V_{AB} and I_{AN} for unbalanced CHB input voltages

V. APPLICATIONS OF THE PROPOSED INVERTER

With the revolution in power electronic technology, high rated semiconductor switches such as IGBT-module, FZ500R65KE3 with a voltage rating up to 6.5 kV, is readily available in the market [47]. Moreover, the voltage and current ratings of switching devices can be further extended by connecting multiple switches in a suitable series-parallel combination. This will facilitate the utilization of the proposed inverter in various grid-connected applications. For example, the proposed inverter can be utilized in hybrid renewable energy conversion systems in which different renewable energy sources such as solar photovoltaic, wind and battery storage are integrated via a common DC-link as shown in the block diagram of Fig. 15 [48] in which the proposed topology facilitates the integration of such sources with the grid. Furthermore, as highlighted in case study 2 in section VI, the proposed inverter is a good candidate for motor drive and electric vehicles applications.

TABLE 2 COMPARISON OF THE PROPOSED THREE PHASE INVERTER CONCEPT WITH CONVENTIONAL THREE PHASE STRUCTURES

Three phase MLI		N_{level}	N_{Switch}	N_{Gate}	$N_{Rectifier}$
[33]	Conventional 3- phase structure	9	30	30	9
	This paper proposed structure	11	18	18	4
[25]	Conventional 3- phase structure	81	48	48	24
	This paper proposed structure	83	28	28	9
[26]	Conventional 3- phase structure	13	30	30	12
	This paper proposed structure	15	22	22	5
[49]	Conventional 3- phase structure	49	66	66	24
	This paper proposed structure	51	34	34	9

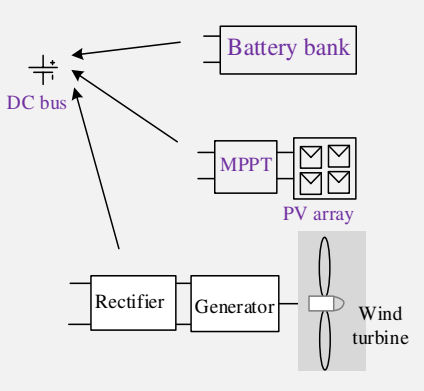


Fig. 15 Common DC-bus with hybrid renewable energy sources

VI. COMPARISON WITH OTHER THREE PHASE CMLI TOPOLOGIES

In this section, the proposed CMLI concept proposed in this paper is compared with some counterparts CMLI topologies proposed in the literatures. Several CMLI topologies are proposed in the literature with the aim of reducing the device count and maximizing the number of levels in the output voltage [25, 26, 49].

Unfortunately, the majority of these topologies are only presented as a single-phase structure. To extend these inverters to three phase structures, the number of power electronic devices required is simply three times that of the single phase inverter structure [28, 32, 33, 35]. The proposed CMLI topology in this paper allows the replacement of the cascaded stage in Fig. 1(a) with any existing single phase topology to realize a three phase structure without tripling the device count as per the current practice.

Table 2 shows a detailed device count comparison between the conventional three phase structure and the proposed three phase structure in this paper for some recently developed CMLI topologies. As it can be seen from the table, the proposed topology in this paper exhibits a significant reduction in the number of device count including number of switches N_{Switch}, number of gate driver circuits N_{Gate} and number of rectifiers $N_{Rectifier}$ while achieving higher levels N_{level} in the output voltage when compared with other conventional 3-phase CMLI structures.

On the other hand, various three-phase magnetic linked, asymmetric H-bridge modules-based CMLIs have been reported in the literature. In [17], an H-bridge module-based CMLI is implemented using high frequency magnetic link to generate 27-levels in the line voltages. An isolated dc-link H-bridge module- based CMLI could achieve 81-level in the output voltage as presented in [13]. In both cases, trinary relation is maintained among the input dc supplies to the H-bridge modules. Three H-bridge modules in the CMLI topology proposed in [17], are connected directly with the dc-power supply and hence, this arrangement does not ensure the essential galvanic isolation required for grid-connected applications. To facilitate a comparison with these two topologies, a trinary-relation has been maintained among the dc-supplies of the CHB cells in the CMLI proposed in this paper. Also, the number of CHB cells has been increased to three to achieve 29-levels in the output voltage waveform which is close to the 27-levels achieved in [17]. For comparison with the 81-level CMLI topology presented in [13], the number of CHB cells in the topology proposed in this paper is increased to 4.

TABLE 3 COMPARISON BETWEEN THE PROPOSED CMLI AND COUNTERPARTS CMLI TOPOLOGIES PROPOSED IN [13] AND [17]

Category	3-phase, 27-level CMLI proposed in [17]	Proposed CMLI with trinary-related three CHB cells	3-phase, 81-level CMLI proposed in [13]	Proposed CMLI with trinary-related four CHB cells
N_{level}	27	29	81	83
N_{Switch}	36	24	48	28
N_{Gate}	36	21	48	25
$N_{Rectifier}$	9	4	12	5
$THD_{line\ voltage}$	3%	2.97%	1%	1%

Table 3 shows a detailed comparison between the proposed CMLI in this paper and those proposed in [13] and [17], when generating close number of levels in the output voltage by adopting trinary related input dc voltages to the H-bridge modules in the cascaded stage.

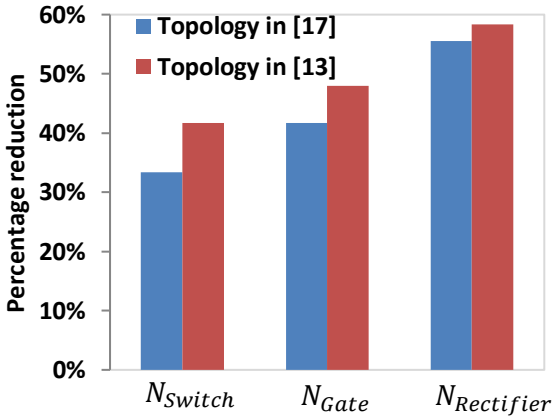


Fig. 16 Percentage reduction in device count with respect to CMLI topologies proposed in [13] and [17]

As can be seen in the table, a notable amount of device reduction is achieved while implementing the concept proposed in this paper. The percentage reduction in the power electronic components employed to implement the proposed CMLI in this paper when compared to the topologies in [13] and [17] is significant; in particular, when a higher number of levels in the output voltage waveform is required as can be seen in Fig. 16. It should be noted that the device count reduction achieved in the proposed CMLI concept in this paper does not compromise for the quality of the output waveforms as can be seen from the number of voltage levels and THD in the voltage waveform.

VII. CONCLUSION

A new high frequency magnetic linked-based cascaded multilevel inverter is presented in this paper. The proposed concept exhibits several advantageous when compared with

counterpart topologies proposed in the literatures. This includes the ability to extend the single-phase inverter to a three-phase structure without tripling the power electronic components as per the current practice in the literatures. Experimental and simulation analyses reveal the feasible applications of the proposed inverter with renewable energy sources of intermittent characteristics. Results also show the performance of the proposed inverter is not significantly impacted during load dynamic changes. The proposed concept is easy to implement as it can employ any cascaded inverter topology within a cascaded stage along with a simple conventional three-phase two-level inverter stage.

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