

A new cascaded multilevel inverter with series and parallel connection ability of DC voltage sources

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Abstract: In this paper, a new multilevel inverter is proposed based on the connection of DC voltage sources in series and parallel. The proposed topology is composed of series basic units that consist of series and parallel connections of DC voltage sources. The values of the DC voltage sources differ from one unit to another. A new algorithm to determine the magnitude of the DC voltage sources of the proposed structure is presented. All of the related equations for the proposed multilevel inverter are extracted and the optimum structure from several points of view such as the maximum blocked voltage by switches, the number of switches and that of the DC voltage sources is obtained in order to have the maximum voltage levels at the output. The proposed topology is compared with that of some of the multilevel inverters presented recently. Finally, the proposed structure and capabilities are reconfirmed using simulation and experimental results for a 53-level typical inverter.

Key words: Multilevel inverter, series-parallel connection, basic unit

1. Introduction

In recent years, multilevel inverter technology in the field of power electronics has had rapid growth and managed to become one of the most important components of DC to AC voltage conversion. Nowadays, there are 3 basic topologies for multilevel inverters: diode clamped multilevel inverters [1], flying capacitor multilevel inverters [2], and cascaded H-bridge multilevel inverters [3]. Among these inverter topologies, cascaded multilevel inverters have the capability to produce a higher number of output voltage levels. Due to their modular structure, these topologies are more reliable [4].

The multilevel inverters that are used in cascaded H-bridges [5–8] not only show the ability of producing higher voltage levels, but also reveal that more and more levels can be produced at the output by cascading different basic structures. As a result, this topology is able to provide better waveform quality at the output. The disadvantage of this kind of inverter is the necessity for a large number of isolated DC sources [5–9].

A cascaded multilevel inverter is based on several series-connected single-phase inverters. This type of structure is capable of producing medium- and high-output voltage level low-voltage components. The other advantage for the cascaded multilevel inverter is its modular structure. This topology is constructed from smaller units with the same structure and control circuit [10]. When an error occurs in one of the units, this feature makes it possible for the defective unit to be easily and quickly replaced with a fault-free unit. Moreover, with a proper control technique, bypassing the flawed unit is possible without any interruption in the load [11].

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In addition, the advantage of the modular cascaded multilevel inverter is the concept of using multiple units instead of a large number of components. This feature greatly reduces the number of additional hardware [12]. More recently, some multilevel topologies were derived from generalized topologies such as the Marx multilevel inverter [13] and zigzag multilevel inverters [14].

Some new optimum topologies with a reduced number of switches were presented in [15–20]. Among the mentioned topologies, only the multilevel inverter presented in [20] was used in series and parallel connections of DC voltage sources. This topology was derived from the Marx multilevel inverter [13] and does not have the advantages of the cascaded multilevel inverters mentioned previously.

In this paper, the proposed multilevel inverter not only has the modularity feature of cascaded topologies but also consists of the ability of series and parallel connections of DC voltage sources. Series and parallel connections of the DC voltage sources increase the output voltage levels and injected or given current to the multilevel inverter, respectively. In the proposed topology, the magnitude of the DC voltage sources differs from one unit to another. The blocked voltage by each switch in a specific unit is the same as that of the other switches used in the same unit and is equal to the magnitude of the DC voltage source used in the unit. Therefore, the number of gate-driving circuits is reduced and, as a result, the size of the multilevel inverter and its power consumption are reduced. In addition, the ability of switching at a high frequency is provided by this feature. Another feature of the proposed topology is that there is no necessity for bidirectional switches. In this paper, a new procedure is recommended to find out the magnitude of the DC voltage sources and produce all of the output voltage levels (even and odd). Finally, a method to find out the optimal number of switches and DC voltage sources so as to have the maximum output voltage levels with the minimum blocked voltage by the switches is presented. A comparison between the proposed topology with the topologies presented in [15], [16], and [20] is done. Finally, the proposed structure and capabilities are reconfirmed using simulation and experimental results for a 53-level typical inverter.

2. Proposed topology

Figure 1 shows the basic unit for the proposed multilevel inverter. This basic unit consists of 2 isolated DC voltage sources and 5 switches, S_0 , S_1 , S_{a1} , S_{b1} , and S_{c1} . The blocking voltage by the switches in Figure 1 is always positive. Therefore, the proposed topology does not need bidirectional switches from the viewpoint of voltage blocking and an insulated-gate bipolar transistor (IGBT) with an antiparallel diode can be used as the power switch. The basic unit shown in Figure 1 can generate 3 different voltage levels at the output (v_o). When switches S_0 and S_{c1} become ON, a 0 voltage level is produced at the output. By turning on the switches, S_1 , S_{b1} , and S_{c1} , the 2 DC voltage sources are paralleled and V_{dc} is produced at the output. Similarly, when

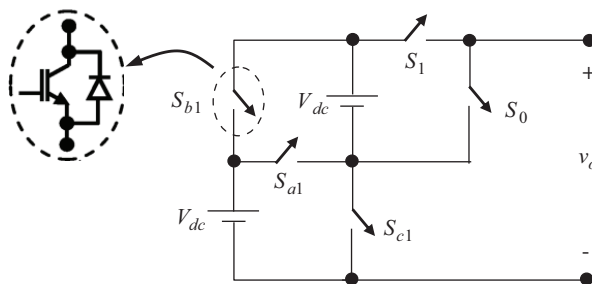


Figure 1. Proposed basic unit.

Table 1. Values of v_o for different states of the basic unit switches.

Switch states					v_o
S_{a1}	S_{b1}	S_{c1}	S_1	S_0	
0	0	0	0	1	0
0	1	1	1	0	V_{dc}
1	0	0	1	0	$2V_{dc}$

switches S_1 and S_{a1} become ON, the 2 DC voltage sources could be connected in series and $2V_{dc}$ is produced at the output. Table 1 shows the output voltage values for different states of the switches. In this Table, 0 and 1 represent the OFF and ON states of the switches, respectively. The capability of the basic unit for producing a 0 voltage level differs between this basic unit and that presented in [20]. When the units are connected in series, the mentioned capability will be useful and realizes the unit bypassing issue.

Figure 2 shows the topology of the extended unit. The extended unit is constructed of series connection of the basic units shown in Figure 1 and consists of n isolated DC voltage sources. Due to the ability of parallel connection of DC voltage sources, the magnitude of these sources is assumed as V_{dc} . The number of output voltage levels at the extended unit (N_{step}) is given as follows:

$$N_{step} = n + 1. \quad (1)$$

If the maximum output voltage and the number of used switches for the topology shown in Figure 2 are displayed with $V_{o,max}$ and N_{switch} , respectively, $V_{o,max}$ and N_{switch} are calculated by following equations:

$$V_{o,max} = \sum_{j=1}^n V_{dc} = nV_{dc}, \quad (2)$$

$$N_{switch} = 3(n - 1) + 2 = 3n - 1. \quad (3)$$

Table 2 shows the values of v_o for different states of the switches, $S_{a,1} - S_{a,n-1}$, $S_{b,1} - S_{b,n-1}$, $S_{c,1} - S_{c,n-1}$, S_0 , and S_1 , for the structure shown in Figure 2. As can be seen from Table 2, $n + 1$ different values of voltage are available across v_o . It is important to note that the structure shown in Figure 2 is capable of producing positive voltage levels at the output. The number of DC voltage sources connected in parallel ($N_{parallel}$) for each produced voltage level is shown in Table 2. The relation between the number of DC voltage sources connected in series (N_{series}) and parallel ($N_{parallel}$) can be expressed as follows:

$$N_{series} = n - N_{parallel}. \quad (4)$$

In Figure 2, the relation between the output voltage (v_o) and the number of DC voltage sources connected in series (m) can be expressed as follows:

$$v_o = (n + 1 - m)V_{dc} \quad m \neq 0, \quad (5)$$

where $m = 1$ and all of the DC voltage sources are connected in series.

In order to use the advantages of the cascaded multilevel inverter and produce more output voltage levels, k extended units are used in series, according to Figure 3. As mentioned previously, the topology shown in Figure 2 is capable of producing only positive voltage levels at the output. Therefore, to produce positive and negative voltage levels accordantly, an H-bridge ($T_1 - T_4$) is used at the output.

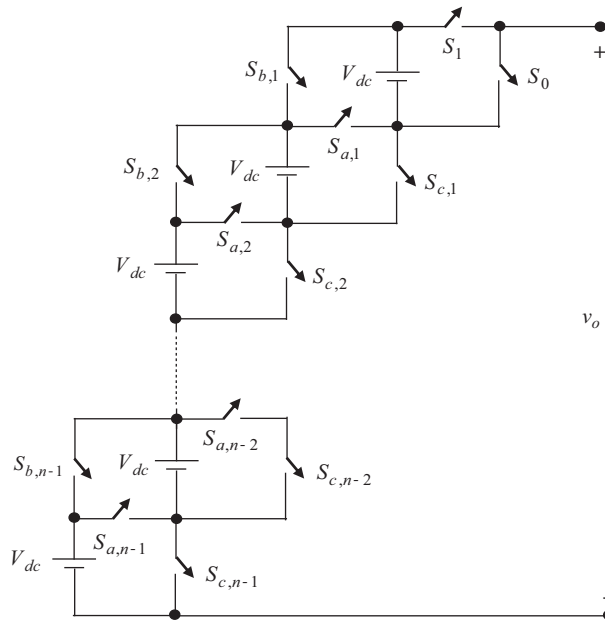


Figure 2. Proposed extended unit.

Table 2. Values of v_o for different states of the extended unit switches.

v_o	0	V_{dc}	$2V_{dc}$...	$(n-1)V_{dc}$	nV_{dc}
Switch states	$S_{a,1}$	0	0	1	...	1
	$S_{a,2}$	0	0	0	...	1
	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
	$S_{a,n-2}$	0	0	0	...	1
	$S_{a,n-1}$	0	0	0	...	0
	$S_{b,1}$	0	1	0	...	0
	$S_{b,2}$	0	1	1	...	0
	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
	$S_{b,n-2}$	0	1	1	...	0
	$S_{b,n-1}$	0	1	1	...	1
	$S_{c,1}$	1	1	0	...	0
	$S_{c,2}$	1	1	1	...	0
	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
	$S_{c,n-2}$	1	1	1	...	0
	$S_{c,n-1}$	1	1	1	...	1
	S_0	1	0	0	...	0
	S_1	0	1	1	...	1
$N_{parallel}$	0	n	$n-1$...	2	

Due to the ability of parallel connection of the DC voltage sources shown in Figure 3, the magnitude of all DC voltage sources in a unit is assumed to be equal. The 1st unit, 2nd unit, ..., and k th unit have n_1, n_2, \dots, n_k DC voltage sources with the values of V_1, V_2, \dots, V_k and nominal currents of I_1, I_2, \dots, I_k , respectively.

The nominal output current of each unit in Figure 3 can be obtained as follows:

$$I_{o,j} = bI_j. \tag{6}$$

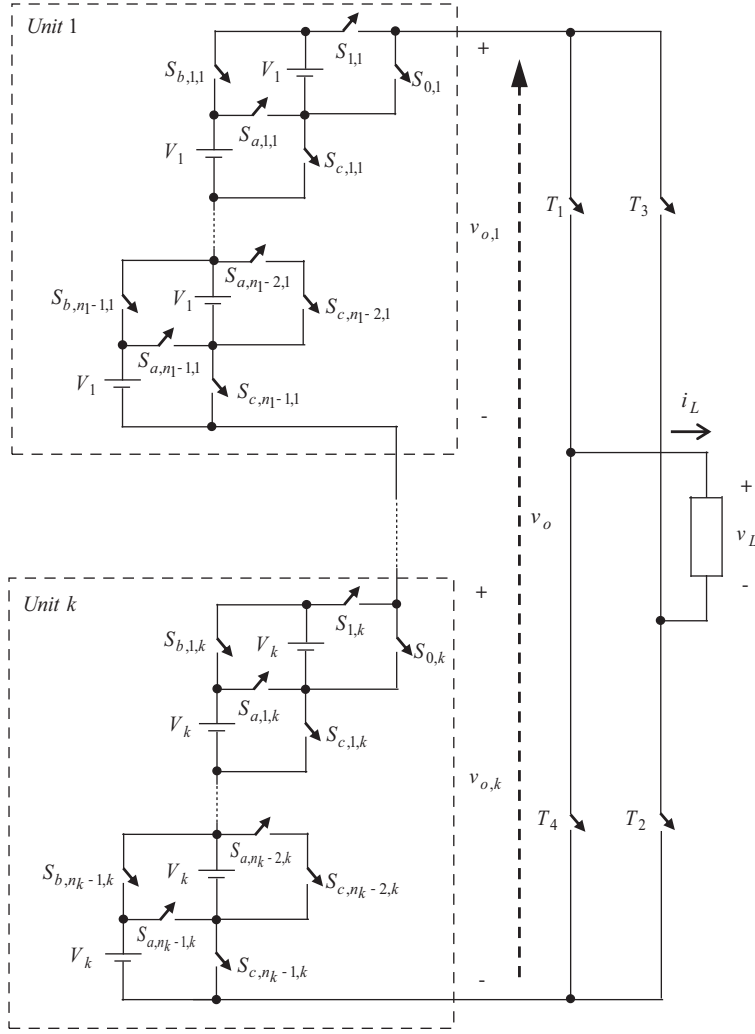


Figure 3. Proposed topology.

Here, $I_{o,j}$ and I_j show the nominal output current of the j th unit and that of the DC voltage source of V_j , respectively. The b variable is the first integer number less than the noninteger number of a . The a variable is defined as follows:

$$a = \left\lfloor \frac{V_j n_j}{V_{o,j}} \right\rfloor, \quad (7)$$

where $V_{o,j}$ and V_j are the output voltage of the j th unit and the magnitude of the DC voltage source used in the j th unit, respectively. It should be noted that if a is obtained as an integer number, the variation of b will be equal to a .

Due to the ability of series connection of the units in Figure 3, the nominal output current of the proposed topology will be equal to the nominal output current of the unit with the minor inverse current.

In Figure 3, the maximum number of the output voltage levels (v_L) can be calculated as follows:

$$N_{step} = 2 \times \left[\prod_{j=1}^k (n_j + 1) \right] - 1, \quad (8)$$

where n_j shows the number of DC voltage sources used in the j th unit.

The maximum output voltage for the proposed topology is obtained by:

$$V_{o,\max} = \sum_{j=1}^k (n_j \times V_j), \quad (9)$$

where V_j is the magnitude of the DC voltage sources used in the j th unit.

The number of required switches (N_{switch}) for the proposed topology is given by:

$$N_{switch} = 4 + \sum_{j=1}^k (3n_j - 1). \quad (10)$$

There are a lot of ways to determine the magnitude of the DC voltage sources. Some of these algorithms are not able to produce all voltage levels at the output and some of them produce repetitive voltage levels. In order to prevent the mentioned problems and produce the maximum number of voltage levels, the values of the DC voltage sources in each unit will be chosen based on the following algorithm:

Unit 1:

$$V_1 = V_{dc}. \quad (11)$$

Unit 2:

$$V_2 = n_1 V_1 + V_{dc} = (n_1 + 1)V_{dc}. \quad (12)$$

Unit 3:

$$V_3 = n_1 V_1 + n_2 V_2 + V_{dc} = (n_1 n_2 + n_1 + n_2 + 1)V_{dc}. \quad (13)$$

Unit k:

$$V_k = \left(\sum_{j=1}^k n_j V_j \right) + V_{dc}. \quad (14)$$

3. Optimal structures

In the proposed topology, to achieve a certain voltage level at the output, various positions of units, switches and that of the DC voltage sources can be used. In other words, there are diverse states for connection of the proposed topology components to produce a specified voltage level. Obtaining the best structure from the view of the number of switches, the DC voltage sources, and minimum of blocked voltage by the switches for producing the maximum number of voltage levels at the output will be worthwhile due to reducing the size and total cost of the system. In this section, the optimal structures for the proposed topology shown in Figure 3 are investigated from different aspects.

3.1. Optimization of the proposed topology for the maximum number of voltage levels with a constant number of switches

One of the most desirable goals in a multilevel inverter is to produce the maximum number of output voltage levels using the minimum number of switches. If the number of switches (N_{switch}) is constant, the maximum number of output voltage levels must be specified.

The number of switches for the proposed topology shown in Figure 3 is calculated from the following equation:

$$N_{switch} = \sum_{j=1}^k (3n_j - 1) + 4 = 3(n_1 + n_2 + \dots + n_k) - k + 4. \quad (15)$$

Considering Eq. (15), it is clear that:

$$n_1 + n_2 + \dots + n_k = \frac{N_{switch} + k - 4}{3}. \quad (16)$$

The number of voltage levels (N_{step}) at the output of the proposed topology that is stated by Eq. (8) can be rewritten as follows:

$$N_{step} = 2 \times (n_1 + 1) \times (n_2 + 1) \times \dots \times (n_k + 1) - 1. \quad (17)$$

Considering Eqs. (16) and (17), the maximum number of voltage levels in Eq. (8) will be maximized when the following condition is considered:

$$n_1 = n_2 = \dots = n_k = n. \quad (18)$$

By Eqs. (16) and (18), k can be calculated as follows:

$$k = \frac{N_{switch} - 4}{3n - 1}. \quad (19)$$

Considering Eqs. (17) and (18), the maximum number of voltage levels will be equal to:

$$N_{step} = 2 \times (n + 1)^k - 1. \quad (20)$$

Replacing k from Eqs. (19) into (20), the maximum number of voltage levels can be rewritten as follows:

$$N_{step} = 2 \times (n + 1)^{\frac{N_{switch} - 4}{3n - 1}} - 1. \quad (21)$$

Eq. (21) will maximize when $(n + 1)^{\frac{1}{3n - 1}}$ gets its maximum value. Figure 4 shows the variation of $(n + 1)^{\frac{1}{3n - 1}}$ versus n . As shown in Figure 4, N_{step} will maximize for $n = 2$. In other words, N_{step} will maximize when each unit of the proposed topology, shown in Figure 3, contains 2 isolated DC voltage sources.

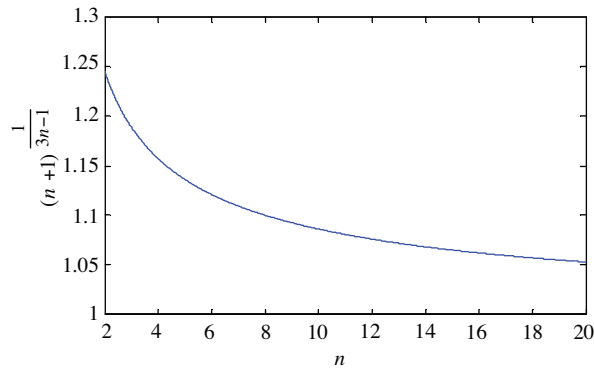


Figure 4. Variation of $(n + 1)^{\frac{1}{3n - 1}}$ versus n .

3.2. Optimization of the proposed topology for the maximum number of voltage levels with a constant number of DC voltage sources

In this subsection, the aim is to find a structure that produces the maximum number of output voltage levels using a specified number of DC voltage sources. This means that the desirable n must be obtained in order to satisfy the mentioned condition.

The number of DC voltage sources (N_{source}) for the structure shown in Figure 3 is given by:

$$N_{source} = \sum_{j=1}^k n_j = n_1 + n_2 + \dots + n_k. \quad (22)$$

Considering Eq. (18), the number of DC voltage sources can be expressed as follows:

$$N_{source} = nk. \quad (23)$$

By applying Eq. (23), k is obtained as follows:

$$k = \frac{N_{source}}{n}. \quad (24)$$

Considering Eqs. (20) and (23), N_{step} can be calculated as follows:

$$N_{step} = 2 \times (n + 1)^{\frac{N_{source}}{n}} - 1. \quad (25)$$

Eq. (25) will maximize when $(n + 1)^{\frac{1}{n}}$ gets its maximum value. Figure 5 shows the variation of $(n + 1)^{\frac{1}{n}}$ versus n . As shown in Figure 5, the maximum number of voltage levels is obtained for $n = 2$.

3.3. Optimization of the proposed topology for the minimum number of switches with a constant number of voltage levels

In this section, the desirable purpose is to find the structure that produces a specified number of voltage levels at the output of the proposed topology using the minimum number of switches.

Considering Subsection 3.1, the maximum number of voltage levels for the proposed topology shown in Figure 3 is obtained when the number of DC voltage sources in all units is equal. In other words, the condition $n_1 = n_2 = \dots = n_k = n$ in Eq. (15) must be satisfied for the proposed topology. Therefore, with the consideration of Eqs. (15), (18), and (20), the total number of switches can be calculated as follows:

$$N_{switch} = \left[\ln \left(\frac{N_{step} + 1}{2} \right) \times \frac{3n - 1}{\ln(n + 1)} \right] + 4. \quad (26)$$

Since N_{step} is assumed constant, N_{switch} will minimize when $\frac{3n-1}{\ln(n+1)}$ gets its minimum value. Figure 6 shows the variation of $\frac{3n-1}{\ln(n+1)}$ versus n . This figure illustrates that the minimum value of N_{switch} is obtained for $n = 2$.

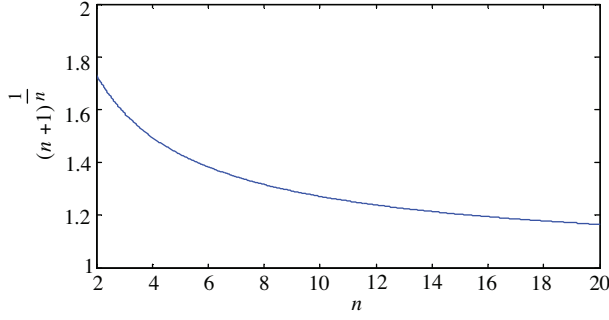


Figure 5. Variation of $(n+1)^{\frac{1}{n}}$ versus n .

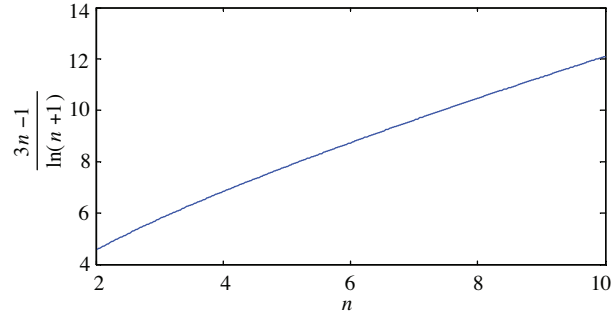


Figure 6. Variation of $\frac{3n-1}{\ln(n+1)}$ versus n .

3.4. Optimization of the proposed topology for the minimum standing voltage of switches with a constant number of voltage levels

The maximum blocked voltage by the switches in a multilevel inverter is a criterion for comparison between different topologies from a switch operation range and total cost of the system points of view [15]. In this section, with the assumption that the number of output voltage levels of the proposed topology is constant, the best structure for minimizing the maximum blocked voltage by the switches will be obtained.

The maximum blocked voltage by the switches (V_{switch}) for the topology shown in Figure 3 is equal to the sum of the blocked voltage by switches S_a , S_b , S_c , S_0 , and S_1 of all units. The value of this voltage is given by:

$$V_{switch} = \sum_{j=1}^k V_{switch,j}. \quad (27)$$

Here, $V_{switch,j}$ is the maximum blocked voltage by the switches of the j th unit. The maximum blocked voltage by the switches of the first unit ($V_{switch,1}$) can be calculated as follows:

$$V_{switch,1} = 3(n_1 - 1) \times V_1 + 2V_1 = (3n_1 - 1)V_1. \quad (28)$$

The maximum blocked voltage by switches in the second unit ($V_{switch,2}$) is given by:

$$V_{switch,2} = 3(n_2 - 1) \times V_2 + 2V_2 = (3n_2 - 1)V_2. \quad (29)$$

Finally, the maximum blocked voltage by the switches of the k th unit ($V_{switch,k}$) can be written as follows:

$$V_{switch,k} = 3(n_k - 1) \times V_k + 2V_k = (3n_k - 1)V_k. \quad (30)$$

Considering Eq. (18) and the expression of the maximum blocked voltage by the switches of each unit from Eqs. (28) to (30), the blocked voltage defined in Eq. (27) can be represented as follows:

$$V_{switch} = (3n - 1) \times \sum_{j=1}^k V_j = (3n - 1) \times (V_1 + V_2 + \dots + V_k). \quad (31)$$

Voltages V_1 to V_k in Eq. (31), show the magnitude of the DC voltage sources in the 1st, 2nd, ..., and k th unit of the proposed topology in Figure 3, respectively. Considering Eq. (18), if the magnitude of the DC voltage

sources is chosen by equations from Eqs. (11) to (14), voltages V_1 to V_k can be represented by the following equations:

$$\begin{aligned}
 V_1 &= V_{dc}, \\
 V_2 &= (n + 1)V_{dc}, \\
 V_3 &= (n^2 + 2n + 1)V_{dc}, \\
 V_4 &= (n^3 + 3n^2 + 3n + 1)V_{dc}, \\
 V_5 &= (n^4 + 4n^3 + 6n^2 + 4n + 1)V_{dc}, \\
 &\vdots \\
 V_k &= (n^{k-1} + C_{k-1}^{k-2}n^{k-2} + C_{k-1}^{k-3}n^{k-3} + \dots + 1) V_{dc}.
 \end{aligned} \tag{32}$$

The symbol C_k^m in Eq. (32) represents the number of m combinations chosen between k given numbers that is defined by:

$$C_k^m = \binom{k}{m} = \frac{k!}{m!(k-m)!}. \tag{33}$$

In order to minimize the blocked voltage by the switches of the proposed topology, each V_1 to V_k in Eq. (31) that is rewritten as Eq. (32) must get its minimum value. Owing to the fact that each voltage in Eq. (32) has a positive value, each voltage from V_1 to V_k will have its minimum value when n is chosen as minimum. As it can be seen from Figure 1, the minimum value for n is 2.

4. Comparison of the proposed topology with those recommended in [15], [16], and [17]

In this section, the proposed topology is compared with 3 topologies recommended in [15], [16], and [20]. These are shown in Figures 7a–7c, respectively. It should be noted that the topologies presented in [15] and [16] use only series connection of the DC voltage sources and the switches of these topologies are bidirectional for blocking the voltage in both directions. The topology presented in [20] uses both the series and parallel connection of the DC voltage sources.

Figure 8 shows the variation of the number of the voltage levels for v_L (N_{step}) into the number of IGBTs (N_{IGBT}) ratio versus the number of the DC voltage sources (n). It should be mentioned that Figure 8 is plotted only for one extended unit. This comparison illustrates that when one unit is used, the proposed topology has no distinction into the presented topologies in [15] and [16], except for the parallel connection of the DC voltage sources.

Figure 9 shows the number of utilized IGBTs (N_{IGBT}) for producing specified numbers of voltage levels at the output. This comparison is done for cascaded units with consideration of the optimization conditions.

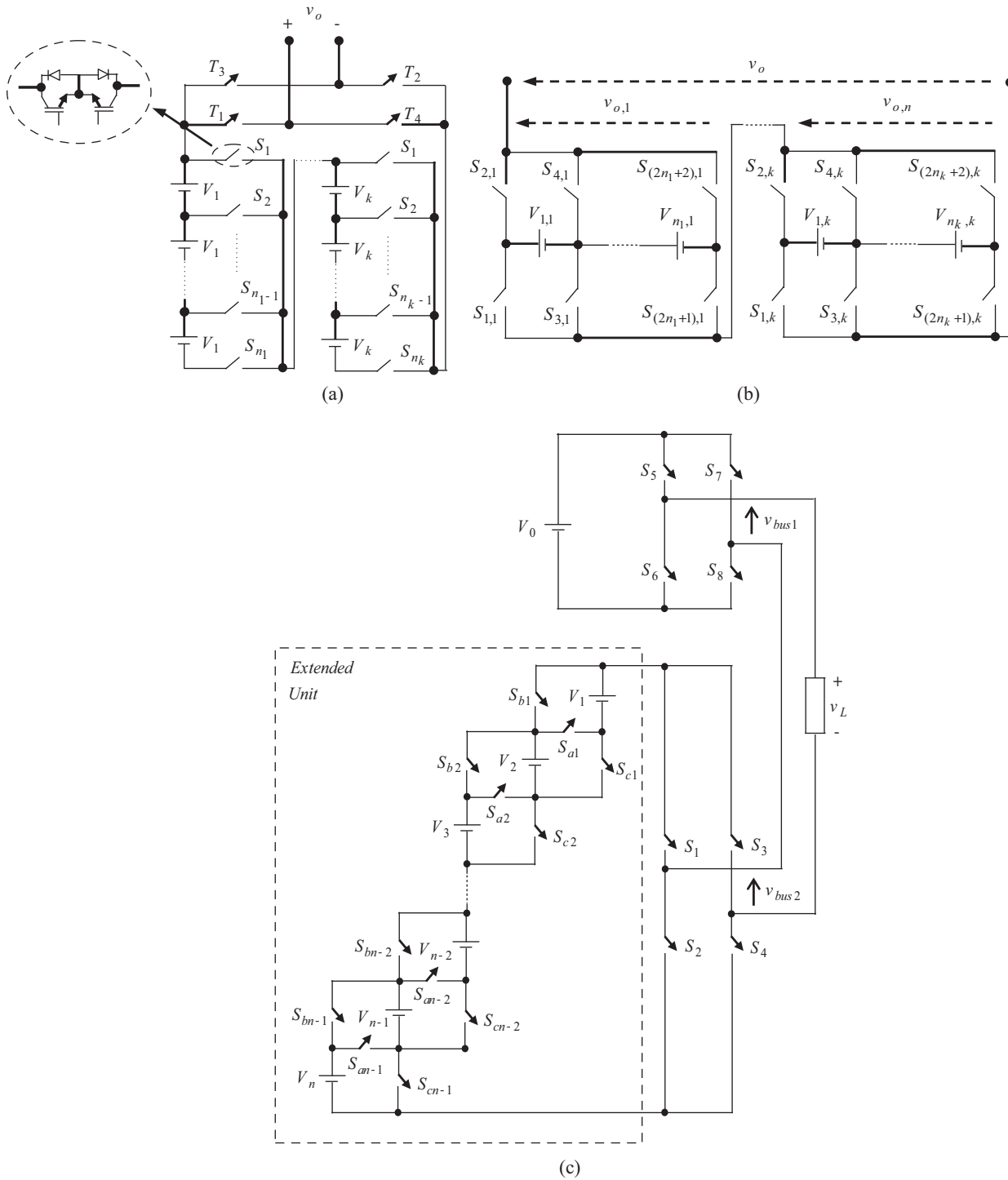


Figure 7. Recommended topology in: a) [15], b) [16], and c) [20].

The variation of the maximum blocked voltage by the switches versus the produced voltage levels at the output is shown in Figure 10. In this comparison, the proposed topology operates better than the topology presented in [16] from a maximum blocked voltage by the switches point of view for a specified voltage level at the output.

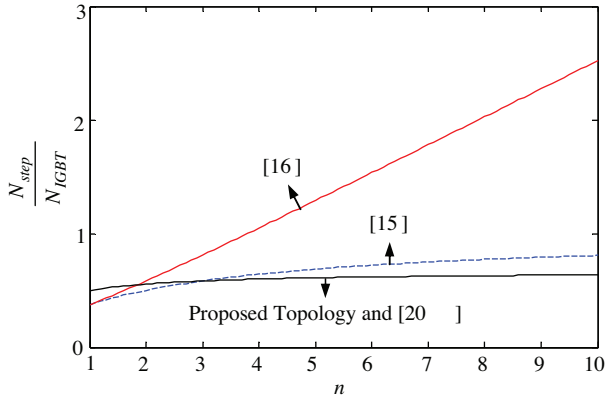


Figure 8. Comparison of $\frac{N_{step}}{N_{IGBT}}$ for the proposed topology and the presented topologies in [15], [16], and [20] for an extended unit with n DC voltage sources.

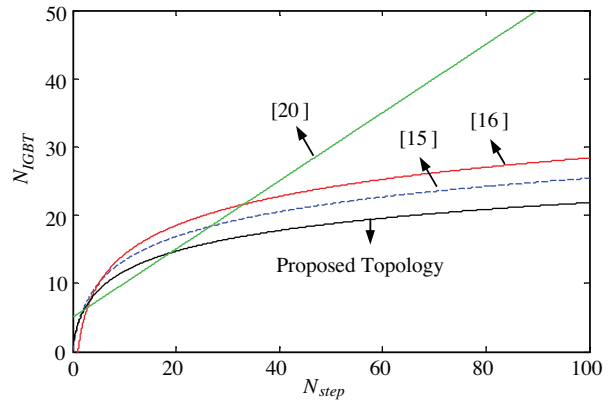


Figure 9. Comparison of the required number of IGBTs to realize N_{step} voltages in the proposed topology and the presented topologies in [15], [16], and [20].

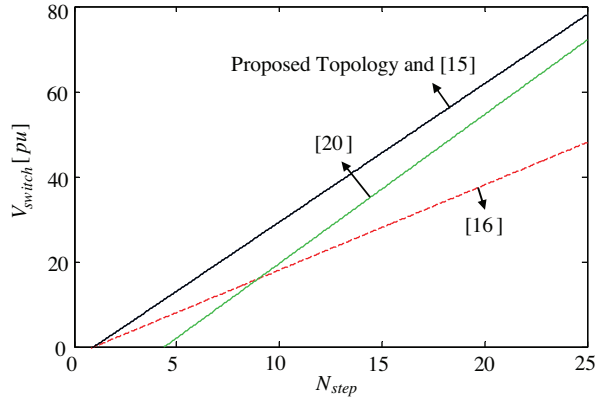


Figure 10. Standing voltages on switches to realize N_{step} voltages in the proposed topology and the presented topologies in [15], [16], and [20].

5. Simulation and experimental results

To evaluate the performance of the proposed structure, a typical single-phase 53-level inverter is simulated by PSCAD/EMTDC software. Figure 11 shows the simulated 25-level inverter circuit. The simulated multilevel inverter is set to generate a 50-Hz staircase 53-level voltage waveform with a maximum value of $110\sqrt{2}$ V. Considering Eq. (8), and according to the proposed algorithm in Eq. (11)–(14), in order to produce $110\sqrt{2}$ V as the peak value of the output voltage, the DC voltage sources' magnitudes in the 1st, 2nd, and 3rd units must be chosen as 6 V, 18 V, and 54 V, respectively. In this paper, the fundamental frequency switching scheme has been chosen for generating the favorite voltage levels at the output. This pattern can be used for minimizing the total harmonic distortion (THD) and eliminating the selective harmonics. However, these aims are not considered in this paper. Table 3 shows the look-up table of the switching states for producing distinctive voltage steps, where 0 and 1 symbolize the OFF and ON states of the switches, respectively. Due to the complementary operation between S_a with S_b and S_c , as well as S_1 with S_0 , only the states of S_a and S_1 are shown in Table 3. It should be noted that S_b and S_c operate identically.

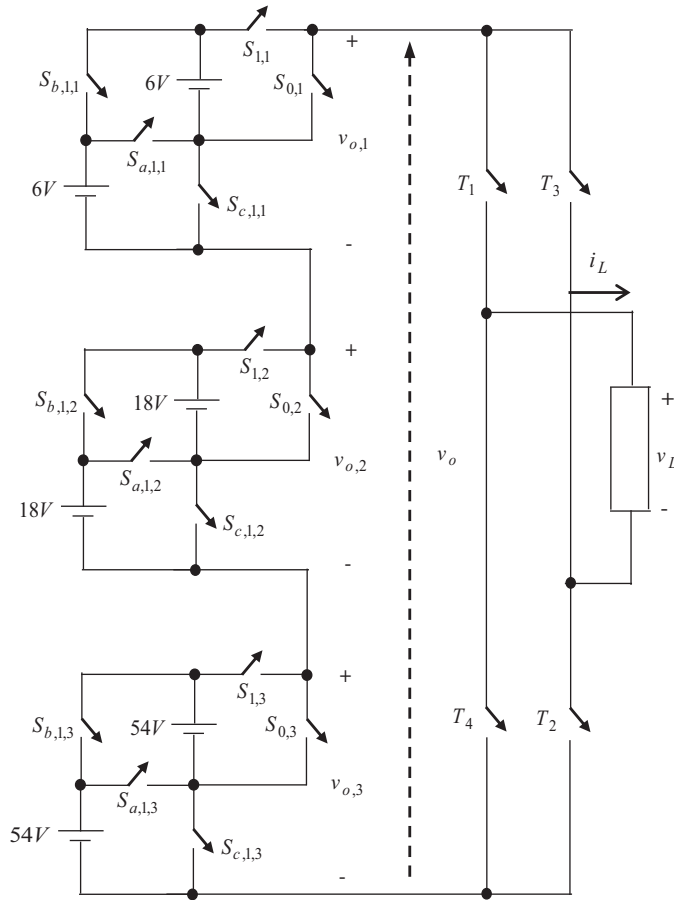


Figure 11. The 53-level proposed inverter circuit.

Table 3. Switching look-up table for the multilevel inverter shown in Figure 11.

Switch states										$v_L[pu] \ 6V = 1pu$
$S_{a,1,1}$	$S_{a,1,2}$	$S_{a,1,3}$	$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	T_1	T_2	T_3	T_4	
1	1	1	1	1	1	0	0	1	1	-26
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
0	0	0	1	0	0	0	0	1	1	-1
0	0	0	0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	1	0	0	1
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots
1	1	1	1	1	1	1	1	0	0	26

Figure 12 shows the 53-level output voltage waveform. As can be seen, the output voltage waveform is very close to the sinusoidal waveform. The THD of the simulated 53-level waveform is 1.27%. Figure 13 shows the simulated output current of the proposed 53-level inverter. The amplitude of the output current based on the simulation is 2.6 A. The R-L load ($R = 60\Omega$ and $L = 23mH$) is used for the simulation. Because of the low pass filtering feature of the R-L load used at the output, the load current shown in Figure 13 is ideally sinusoidal. Figure 14 shows the switching states and blocked voltages by the switches used in the 53-level inverter shown in Figure 11. Zero values in the blocked voltage show the ON state of the switches. As mentioned previously, the

complementary behavior of the switches can be seen in Figure 14. This behavior makes the switches' control simpler. Figure 14 also shows the blocked voltage by the switches. In the proposed topology, the switching frequency of the low-voltage switches is high and the switching frequency of the high-voltage switches is low. Figure 14 clearly shows this fact. Thus, the switching losses will be lower than the other conventional topologies. The high-frequency switching investigation is not the aim of this paper.

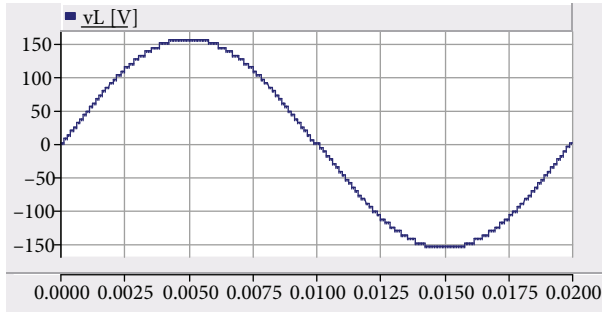


Figure 12. The 53-level output voltage.

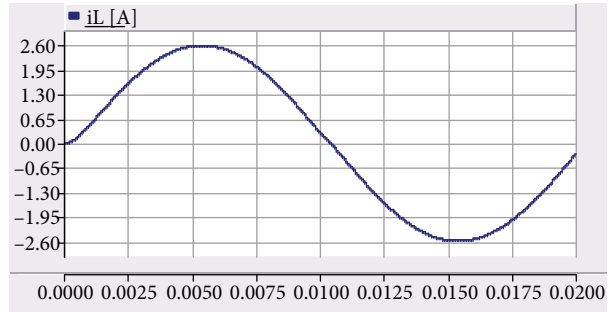


Figure 13. Output current.

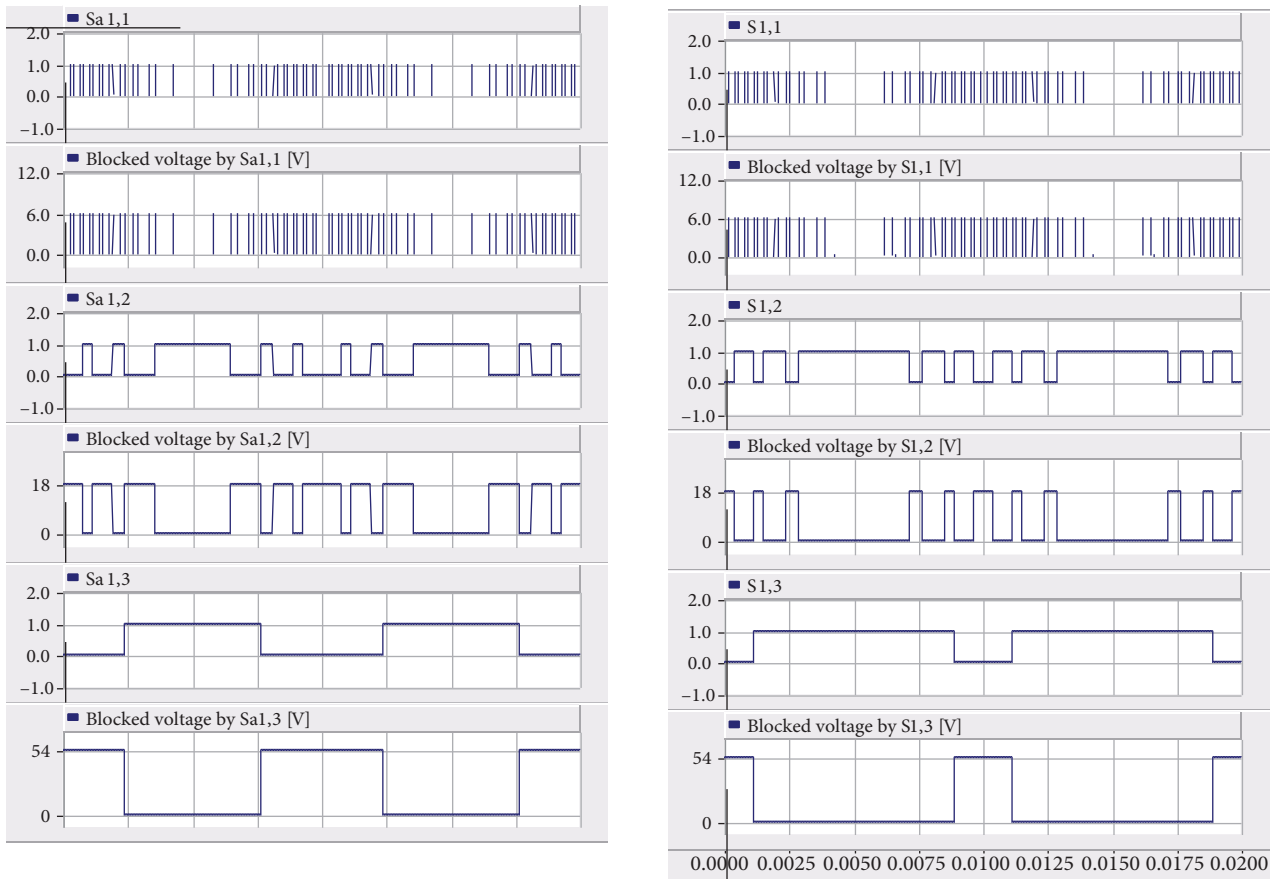


Figure 14. Switching state and blocked voltage by switches.

Figures 15a–15c show the optimal structures recommended in [15], [16], and [20] when considering the minimum number of used switches for producing the maximum voltage $110\sqrt{2}$ V at the output, respectively.

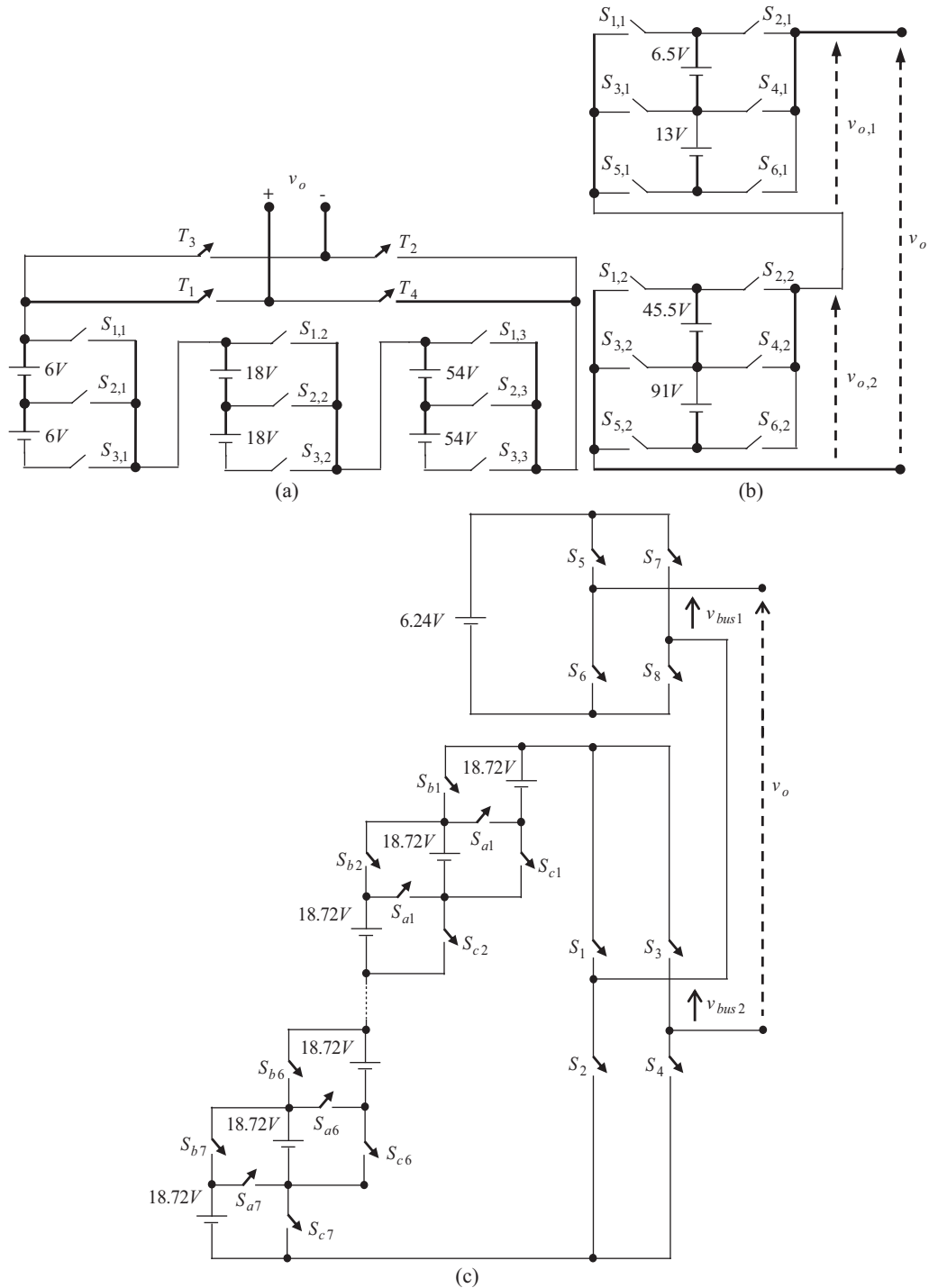


Figure 15. Optimal multilevel structure considering minimum used switches recommended in: a) [15], b) [16], and c) [20].

The structure shown in Figure 15a produces a 53-level output voltage using 22 IGBTs and 6 DC voltage sources. The standing voltage on the switches of this structure is 390 V. Figure 15b can produce a 49-level output voltage with 24 IGBTs and 4 DC voltage sources. The standing voltage on the switches of this structure is 832 V. The

structure shown in Figure 15c produces a 51-level output voltage using 29 IGBTs and 9 DC voltage sources. The standing voltage on the switches of this structure is 393.12 V without any H-bridge consideration. The proposed topology shown in Figure 11 produces a 53-level output voltage with the same maximum value ($110\sqrt{2}$ V) using 19 IGBTs and 6 DC voltage sources. The standing voltage on the switches of the proposed topology is 390 V without considering the blocked voltage by the H-bridge switches.

This experimental study is done for the proposed 53-level inverter with the R-L load ($R=60\Omega$ and $L=23mH$) mentioned in the simulation. The IGBTs of the prototype are BUP306D with internal antiparallel diodes. The 89C52 microcontroller by the ATMEL Company is used to generate the switching patterns. Figure 16 shows the experimental output voltage and current waveforms. The simulated and experimental results for output voltage of each unit ($v_{o,1}$, $v_{o,2}$, and $v_{o,3}$) and series combination of them (v_o) are shown in Figures 17a–17d, respectively. The output voltage of each unit consists of zero and positive voltage levels. As can be seen, the experimental result corresponds with the simulation.

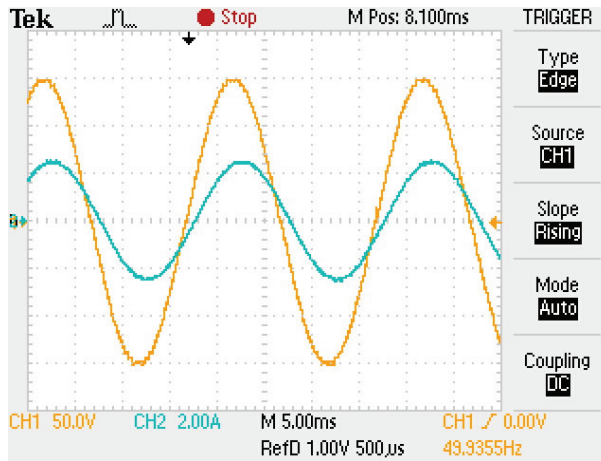


Figure 16. Experimental 53-level output voltage and current.

6. Conclusion

Cascaded multilevel inverters, in addition to acceptable reliability and simple control, provide a better voltage waveform than other types of multilevel inverters. In this paper, a new cascaded multilevel inverter topology is proposed, which is connected to the DC voltage sources in series and parallel. In order to produce all voltage levels (odd and even) at the output, an algorithm for determination the magnitude of the DC voltage sources is also proposed. All equations related to the proposed topology are extracted and the optimum structure from several points of view, such as the number of switches, the number of DC voltage sources, and maximum blocked voltage by the switches, in order to produce the maximum number of output voltage levels, is obtained. According to the optimization restrictions, the proposed topology is always in the optimal state from point of view of the number of switches, number of the DC voltage sources, maximum number of voltage levels at the output, and blocked voltage by the switches, when $n_1 = n_2 = \dots = n_k = n = 2$. The performance of all of the optimization limits by $n = 2$ is an advantage for the proposed multilevel inverter. Finally, the proposed multilevel inverter maintains the ability of series and parallel connections of the DC voltage sources while reducing the number of used IGBTs for producing a specified voltage level at the output with respect to the structures presented in [15], [16], and [20]. It is found that the proposed structure provides 53 voltage levels

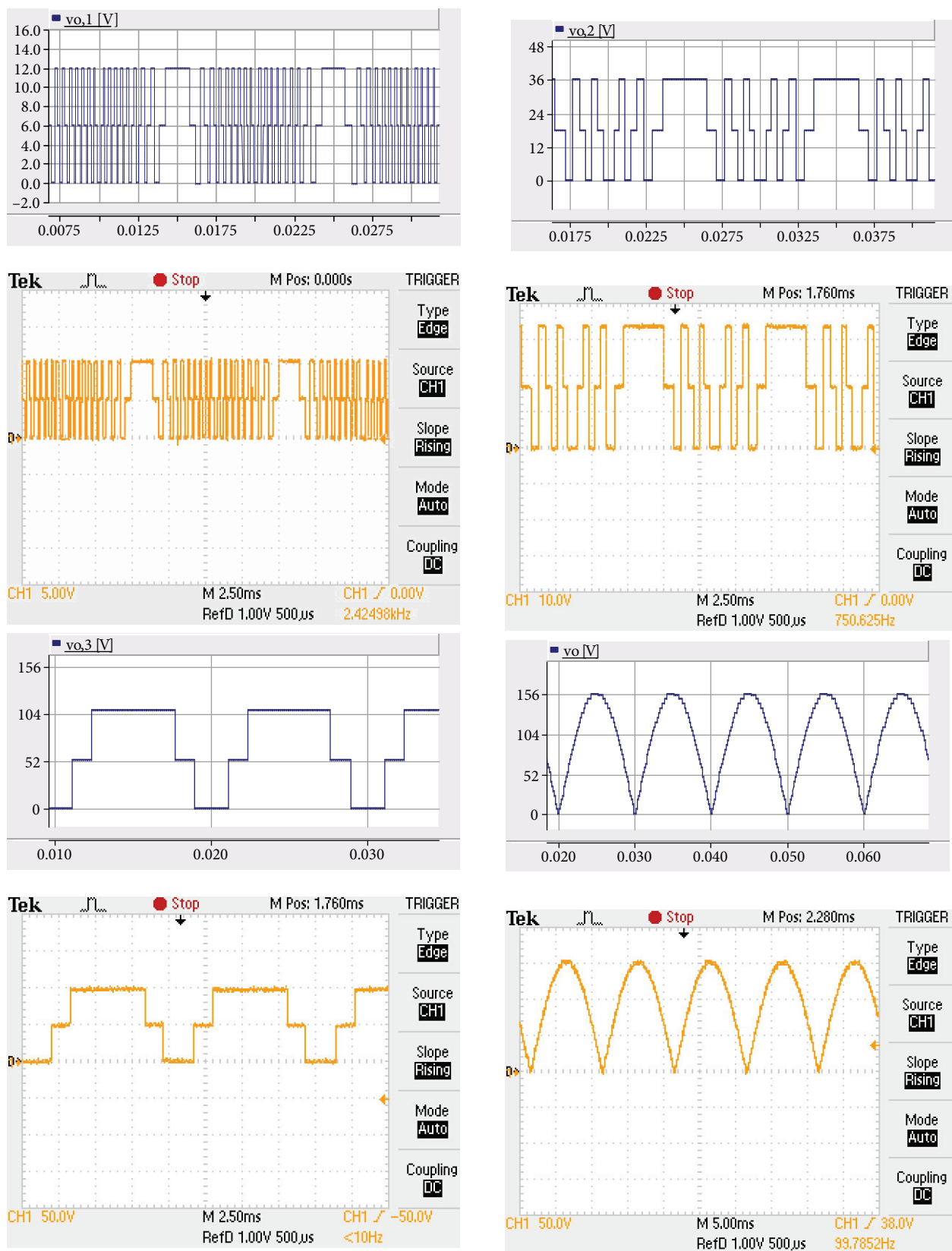


Figure 17. Simulated and experimental output voltage of the: a) 1st unit, (b) 2nd unit, c) 3rd unit, and d) series synthesis of units.

using 19 IGBTs and the structures given in [15], [16], and [20] produce 53, 49, and 51 voltage levels using 22, 24, and 29 IGBTs, respectively.

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