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Ayman M. EL-Refaie

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A New Configuration of Paralleled Modular ANPC Multilevel Converter Controlled by an Improved Modulation Method for 1 MHz, 1 MW EV Charger

Mostafa Abarzadeh

Department of Electrical and Computer Engineering, Marquette University, Milwaukee, WI, USA

Waqar A. Khan

Department of Electrical and Computer Engineering, Marquette University, Milwaukee, WI, USA

Nathan Weise

Department of Electrical and Computer Engineering, Marquette University, Milwaukee, WI, USA

Kamal Al-Haddad

Department of Electrical Engineering, Ecole de Technologie Superieure, Montreal, QC, Canada

Ayman M. El-Refaie

Abstract:

In this article, a new configuration of the modular multilevel converter (MLC) based on the parallel connection of three-level active-neutral-point-clamped (3L-ANPC) cells as well as its improved modulation method is proposed for 1 MHz, 1 MW electric vehicle (EV) megacharger. In the proposed paralleled modular ANPC-MLC, only six high-frequency silicon carbide (SiC) power switches operating at 333 kHz are required to generate 1 MHz switching frequency spectrum. Moreover, the operating voltage of all power devices is halved, the magnitude of the first switching frequency harmonic cluster is decreased by the factor of five, and the load current is equally distributed between the 3L-ANPC legs by employing the proposed improved modulation method. Hence, the modularity, efficiency, and power density of the proposed converter are notably increased, whereas the value of passive components and the overall switching loss are remarkably decreased. In addition, an optimized design of the one 3L-ANPC cell of the proposed paralleled modular ANPC-MLC for 1 MHz, 1 MW EV megacharger using Ansys SIwave, Icepak, and Q3D finite element method platforms is presented and analyzed in detail. The provided experimental results of the down-scaled setup verify the feasibility and viability of the proposed configuration as well as its improved switching pattern.

SECTION I. Introduction

Electric vehicle (EV) fast and ultrafast chargers demand a higher value of rated power, which can be increased over 1 MW for all-electric battery-powered Class 8 semitrailer trucks. Hence, the increasing trend toward utilizing high power density, lightweight, high efficiency, and high switching frequency EV megacharger necessitates employing novel converter configurations, wide bandgap (WBG) devices, improved modulation schemes, and enhanced control methods. Therefore, a project proposal-entitled high power density 1 MHz, 1 MW, three-phase ac to dc ultrafast EV charger has been suggested as a part of the creating innovative and reliable circuits using inventive topologies and semiconductors (CIRCUITS) program announced by the U.S. Department of Energy Advanced Research Projects Agency Energy. Accordingly, the major challenges of this project are achieving 1 MHz switching frequency at 1 MW power level, increasing the converter efficiency, as well as the reduction of weight and size.

Hence, attaining high efficiency and high power density power electronic converter (PEC) necessitates decreasing the size, weight, and loss of PEC, reduction of the value of the passive components as well as improving the power density, efficiency, and modularity of PEC to meet the limits mandated by the relevant stringent standards. Utilizing very high-frequency (HF) PECs by employing WBG devices can be a promising solution to increase the efficiency and power density of PECs for EV applications. However, the high switching frequency in WBG device-based PECs leads to extra electromagnetic interference (EMI) and high dv/dt . A high dv/dt results in a significant common-mode (CM) current because of exciting the capacitive paths in PECs. Accordingly, a high CM leads to damage in the passive components. Moreover, high dv/dt causes insulation and bearing damages in motor drives [1], [2].

To overcome this issue, multilevel converters (MLCs) can be considered as among the most promising solutions for various industrial applications, such as EV megachargers because of high power and medium-voltage operation capability, reduced EMI, improved total harmonic distortion (THD), lower dv/dt , reduced switching frequency and losses, improved power-grid side quality as well as a higher efficiency [3]–[4][5]. In [6], the two-level and three-level active-front-end (AFE) rectifiers have been comprehensively analyzed and compared from various aspects. As concluded in [6], because of higher power density, smaller input filter, low input current distortion, high power factor, and low dc voltage ripple, the three-level AFE rectifier is the most advantageous

configuration. An MW-scale EV charger based on the three-level neutral-point-clamped (NPC) converter has been presented in [7]. By applying the three-level (3L)-NPC converter, the input filter size of the AFE rectifier is notably decreased, which results in a higher power density AFE rectifier. However, the uneven power loss distribution between the power devices is a main drawback of the 3L-NPC AFE rectifier. The active-NPC (ANPC) converter and its hybrid configurations are widely used in various industrial applications, such as medium-voltage variable speed drive, static ground power unit for aircraft, high-efficiency drives for aircraft hybrid electric propulsion systems, and integration of renewable energy sources to the grid [8]–[9][10][11][12]. Therefore, new hybrid configurations of MLC based on the ANPC converter can be utilized to achieve high efficiency, high power density, and reliable PECs for the EV megacharger applications.

In this article, a new configuration of modular MLC based on the parallel connection of the 3L-ANPC cells as well as its improved modulation method is proposed for 1 MHz, 1 MW EV megacharger. This article is organized as follows. Section II describes the proposed paralleled modular ANPC-MLC configuration. Section III explains the proposed modulation method for the paralleled modular ANPC-MLC. The optimized design of the one 3L-ANPC cell of the proposed paralleled modular ANPC-MLC using Ansys Siwave, Icepak, and Q3D FEM platforms is presented in Section IV. The power loss calculation and efficiency evaluation of the proposed paralleled modular ANPC-MLC are discussed in Section V. The experimental results and conclusion are provided in Sections VI and VII, respectively.

SECTION II. Proposed Paralleled Modular ANPC-MLC

The main parameters of the proposed 1 MHz, 1 MW three-phase ultrafast EV megacharger are presented in Table I.

TABLE I Main Parameters of the Proposed Three-Phase-Paralleled Modular ANPC-MLC for the 1 MHz, 1 MW EV Mega Charger

Parameters	Value
Input AC grid line voltage (RMS)	$V_{L-L} = 480V$
Input AC grid frequency	$f = 60 Hz$
Input AC side nominal input current (RMS)	$I_{in} = 1200A$
Mega Charger nominal output power	$P = 1MW$
Mega Charger output voltage	$V_{dc} = 1000V$
Mega Charger output nominal current	$I_{dc} = 1000A$
Frequency of first switching harmonic cluster	$f_{1st-SW-Harmonic} = 1MHz$
Each 3L-ANPC leg inductor	$L_f = 42\mu H$

Fig. 1 presents the proposed three-phase 13-level-paralleled modular ANPC-MLC for 1 MHz, 1 MW EV megacharger. As shown in Fig. 1, the proposed three-phase-paralleled modular MLC topology consists of nine 3L-ANPC cells. All the utilized nine 3L-ANPC cells are identical, which leads to increase modularity of the proposed converter. Because of the needs for operating at the high switching frequency, all the utilized power devices in the 3L-ANPC cells are selected as SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) to decrease the total conduction and switching power losses of the proposed converter. Moreover, a novel improved modulation method is proposed for the presented three-phase 13-level-paralleled modular ANPC-MLC in Fig. 1. As depicted in Fig. 1, in each phase of the proposed three-phase 13-level-paralleled modular ANPC-MLC, 6 HF devices commutate only at 333 kHz, and the other 12 low-frequency (LF) devices operate at the line frequency (60 Hz) to achieve 1 MHz switching frequency spectrum by applying the proposed modulation method. In addition, each phase of the proposed paralleled modular ANPC-MLC generates seven voltage levels

at the output, thus, the output line–line voltage has 13 voltage levels. Hence, by employing the proposed modulation method, not only the proposed paralleled modular ANPC-MLC generates seven-level phase-neutral voltage and 13-level line–line voltage but also decreases the HF power devices switching frequency to 333 kHz to provide a 1 MHz switching frequency spectrum. The main advantages of the proposed paralleled modular ANPC-MLC for 1 MHz, 1 MW EV megacharger, and its proposed modulation method are summarized as follows.

1. The HF power devices commute only at 333 kHz to provide 1 MHz switching frequency spectrum. Hence, the switching loss is significantly decreased, thus the efficiency of the proposed paralleled modular ANPC-MLC is notably increased.
2. In each phase, only six power devices operate at the high frequency and the other 12 power devices operate at the line frequency. Hence, the efficiency of the proposed paralleled modular ANPC-MLC is high.
3. The load current is evenly distributed between all nine 3L-ANPC cells. Hence, the total conduction loss of the converter is equally distributed between all cells.
4. The proposed paralleled modular ANPC-MLC generates seven-level phase voltage and 13-level line voltage. Hence, the size of the input inductor is notably reduced, thus the power density of the EV megacharger is significantly increased.
5. The operating voltages of all power devices are $V_{dc}/2$. Hence, dv/dt of the power devices is significantly reduced. Thus, the emitted EMI of the proposed paralleled modular ANPC-MLC is reduced and the required EMI filter value is significantly decreased.
6. The proposed three-phase 13-level-paralleled modular ANPC-MLC comprises nine identical 3L-ANPC cells. Hence, the modularity of the proposed converter is considerably increased.

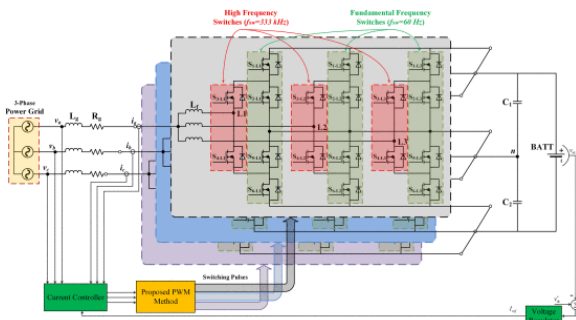


Fig. 1. Proposed three-phase 13-level (single-phase seven-level)-paralleled modular ANPC-MLC for 1 MHz, 1 MW EV megacharger.

SECTION III. Proposed Modulation Method for the Paralleled Modular ANPC Converter

A. Switching Pattern of the 3L-ANPC Cell

The switching states of each 3L-ANPC cell are illustrated in Table II, where x is the index of each leg in Fig. 1.

TABLE II Switching States of the 3L-ANPC Cell

State	S_x	S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}	V_{ph-NP}
1	+1	1	0	1	0	1	0	$V_{dc}/2$
2	0(U1)	0	1	1	0	0	1	0
3	0(L1)	1	0	0	1	1	0	0

4	-1	0	1	0	1	0	1	$-V_{dc}/2$
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As presented in Table II,

$S_{2x} = \overline{S_{1x}}$, $S_{6x} = \overline{S_{5x}}$, and $S_{4x} = \overline{S_{3x}}$. Regarding the possible switching states, two main switching patterns have been presented for the 3L-ANPC converter in the literature. In the first switching pattern, S_{1x} , S_{2x} , S_{5x} , and S_{6x} switches operate at the switching frequency, and S_{3x} and S_{4x} switches commute at the fundamental frequency [9], [13]–[14][15][16][17]. Although this method has a shorter commutation loop in comparison with the other modulation scheme, it requires four HF power switches operating at the switching frequency and two LF power switches commuting at the line frequency. In the second modulation scheme for the 3L-ANPC converter, only S_{3x} and S_{4x} switches operate at the switching frequency, whereas the remaining S_{1x} , S_{2x} , S_{5x} , and S_{6x} switches commute at the fundamental frequency [18]–[19][20]. Therefore, by utilizing the second switching pattern, only two grid-side power switches commute at the switching frequency and the remaining four dc-link-side power switches operate at the fundamental frequency. Hence, employing the second switching pattern enables utilizing a decoupled two-stage LF and HF modulation scheme in the 3L-ANPC converter by using Si insulated gate bipolar transistor (IGBT) for the dc-link side LF power switches, and SiC MOSFET for the grid-side HF power switches.

Accordingly, with respect to the very high switching frequency of the proposed 1 MHz, 1 MW EV charger, and to reduce the total switching loss and increase the efficiency of the proposed paralleled modular ANPC-MLC, the second modulation method is applied to each 3L-ANPC cell of the proposed MLC. The suggested switching pattern is presented in Fig. 2. As shown in Fig. 2, the switching pattern of each 3L-ANPC cell is the decoupled two-stage LF and HF modulation scheme. The LF (S_{1x}, S_{2x}) and (S_{5x}, S_{6x}) switching signals are generated by a zero-crossing detector as follows:

$$Z_C = \begin{cases} 1, & V_{ref} \geq 0 \\ 0, & V_{ref} < 0 \end{cases}$$

$$S_{1x} = S_{5x} = \overline{S_{2x}} = \overline{S_{6x}} = Z_C.$$

(1)(2)

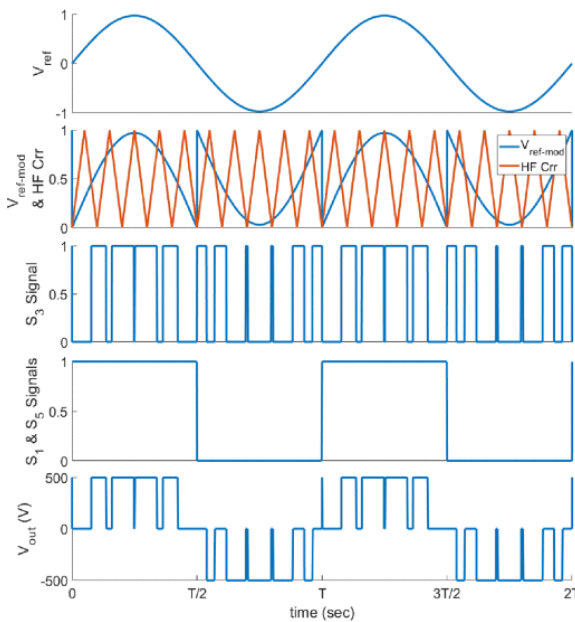


Fig. 2. Switching pattern of each 3L-ANPC cell of the proposed paralleled modular ANPC-MLC.

Hence, the LF (S_{1x}, S_{2x}) and (S_{5x}, S_{6x}) switches operate at the fundamental frequency.

To generate HF (S_{3x}, S_{4x}) switching signals, the modified reference voltage is defined as

$$V_{\text{ref-mod}} = \begin{cases} V_{\text{ref}}, & V_{\text{ref}} \geq 0 \\ 1 + V_{\text{ref}}, & V_{\text{ref}} < 0 \end{cases}$$

(3)

As presented in Fig. 2, the defined $V_{\text{ref-mod}}$ is intersected with a triangular carrier signal to generate $S_{3x} = \overline{S_{4x}}$. Hence, the HF switching function for each 3L-ANPC is defined as

$$s_{\text{Leg}x} = \begin{cases} 1, & \text{if } S_{3x} \text{ is ON} \\ -1, & \text{if } S_{3x} \text{ is OFF} \end{cases}$$

(4)

B. Proposed Modulation Method for the Paralleled Modular ANPC-MLC

The proposed modulation method for the paralleled modular ANPC-MLC for 1 MHz, 1 MW EV charger is performed to achieve the following objectives.

1. The HF power devices commutate only at 333 kHz to achieve the 1 MHz switching frequency spectrum.
2. Each phase of the proposed paralleled modular ANPC-MLC generates a 7-level output voltage. Hence, the number of voltage levels of the output line–line voltage is 13.
3. The load current is evenly distributed between each 3L-ANPC leg of the proposed paralleled modular ANPC-MLC.

The switching pattern of the proposed paralleled modular ANPC-MLC is presented in Fig. 3. As depicted in Fig. 3, the HF triangular carrier signals of one phase are phase shifted by $T_{\text{sw}}/3$ second or $2\pi/3$ radians to generate the HF switching signals of each 3L-ANPC leg. Therefore, based on the analyses in [21]–[22][23] for MLCs, the Fourier series expansion of $s_{\text{Leg}1}$, $s_{\text{Leg}2}$, and $s_{\text{Leg}3}$ HF switching function are expressed as

$$\begin{aligned}
s_{\text{Leg1}} &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty} \{A_{0n} \cos(n\omega_r t) + B_{0n} \sin(n\omega_r t)\} \\
&\quad + \sum_{m=1}^{\infty} \{A_{m0} \cos(m\omega_s t) + B_{m0} \sin(m\omega_s t)\} \\
&\quad + \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \{A_{mn} \cos(m\omega_s t + n\omega_r t) \\
&\quad + B_{mn} \sin(m\omega_s t + n\omega_r t)\} \\
s_{\text{Leg2}} &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty} \{A_{0n} \cos(n\omega_r t) + B_{0n} \sin(n\omega_r t)\} \\
&\quad + \sum_{m=1}^{\infty} \left\{ A_{m0} \cos\left(m\omega_s t - \frac{2m\pi}{3}\right) \right. \\
&\quad \left. + B_{m0} \sin\left(m\omega_s t - \frac{2m\pi}{3}\right) \right\} \\
&\quad + \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} A_{mn} \cos\left(m\omega_s t + n\omega_r t - \frac{2m\pi}{3}\right) \\
&\quad + B_{mn} \sin\left(m\omega_s t + n\omega_r t - \frac{2m\pi}{3}\right) \\
s_{\text{Leg3}} &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty} \{A_{0n} \cos(n\omega_r t) + B_{0n} \sin(n\omega_r t)\} \\
&\quad + \sum_{m=1}^{\infty} A_{m0} \cos\left(m\omega_s t - \frac{4m\pi}{3}\right) \\
&\quad + B_{m0} \sin\left(m\omega_s t - \frac{4m\pi}{3}\right) \\
&\quad + \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} A_{mn} \cos\left(m\omega_s t + n\omega_r t - \frac{4m\pi}{3}\right) \\
&\quad + B_{mn} \sin\left(m\omega_s t + n\omega_r t - \frac{4m\pi}{3}\right)
\end{aligned}$$

(5)(6)(7)

where ω_s and ω_r are the switching and the reference angular frequencies, respectively. The Fourier coefficients in (5)–(7) are determined as

$$A_{mn-Legi} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} S_{Legi}(x, y) \cos(mx + ny) dx dy$$

$$B_{mn-Legi} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} S_{Legi}(x, y) \sin(mx + ny) dx dy$$

(8)(9)

where $x = \omega_s t + \theta_{Legi}$, $y = \omega_r t$, and $i = 1, 2, 3$. θ_{Legi} is the phase shift between the carrier signal of the legi with respect to leg 1. In (5)–(7), the first term represents the dc offset, the second term represents the fundamental component and baseband harmonics, the third term represents the carrier harmonics, and the fourth term represents the sideband harmonics of the modulated reference signal. Regarding (5)–(7), the total switching function of one phase of the proposed paralleled modular ANPC-MLC is defined as

$$S_{total} = \frac{1}{3} \sum_{i=1}^3 S_{Legi} \cdot$$

(10)

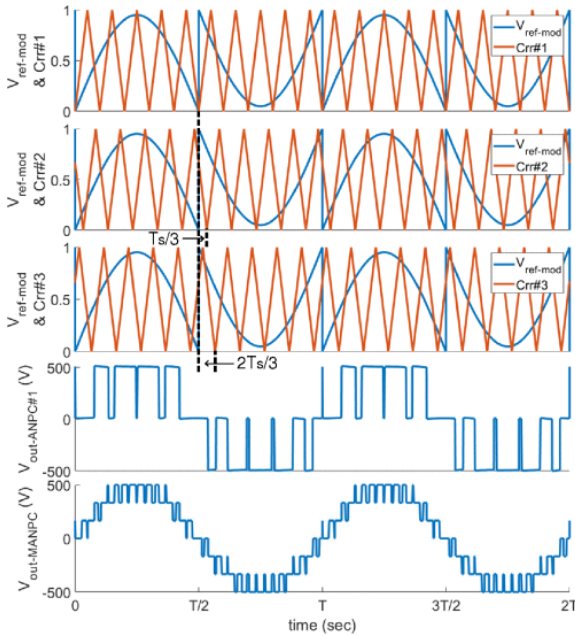


Fig. 3. Proposed switching pattern for one phase of the proposed paralleled modular ANPC-MLC.

In addition, the difference switching signal between two legs of one phase is expressed as

$$S_{diffi} = \frac{1}{2} \{ S_{Legi+1} - S_{Legi} \}, i = 1, 2.$$

(11)

With regard to the fact that the switching frequency is much higher than the fundamental frequency, the Fourier series components of s_{Leg1} , s_{Leg2} , and s_{Leg3} can be separated into different groups of harmonics. Considering (10) and (11), s_{total} presents the harmonic characteristics of one-phase output voltage and s_{diffi} expresses the current distribution between the legs of one phase. Moreover, the switching functions in the frequency domain are defined as $S_{\text{Leg1}}(\omega)$, $S_{\text{Leg2}}(\omega)$, $S_{\text{Leg3}}(\omega)$, $S_{\text{total}}(\omega)$, and $S_{\text{diffi}}(\omega)$, where $\omega = m\omega_s + n\omega_r \geq 0$.

By employing the proposed modulation method and defined switching functions, the harmonics of the switching functions are classified into two classes. The first class, which is related to the total switching function $S_{\text{total}}(\omega)$, contains the Fourier series components for $m = 3k, k = 0, 1, 2, \dots$ and the difference switching signals $S_{\text{diffi}}(\omega)$ are zero in this class. Hence, the first and second switching harmonic clusters of the 3L-ANPC legs in $S_{\text{total}}(\omega)$ are canceled out by utilizing the proposed switching pattern, and $S_{\text{total}}(\omega)$ contains the first switching harmonic clusters at $3f_{\text{SW-Leg}}$. As the very important outcome of the proposed modulation method, the 1 MHz switching frequency spectrum is obtained by commutating the HF power devices only at 333 kHz switching frequency.

The second class, which is related to the difference switching signals $S_{\text{diffi}}(\omega)$, contains the Fourier series components for $m = 3k + (l - 1), k = 0, 1, 2, \dots$ and $l = 2, 3$. In this class, the total switching function $S_{\text{total}}(\omega)$ is zero. Hence, the difference switching signals $S_{\text{diffi}}(\omega)$ contain the switching harmonic clusters at $f_{\text{SW-Leg}}, 2f_{\text{SW-Leg}}, 4f_{\text{SW-Leg}}, 5f_{\text{SW-Leg}}, \dots$. As a result, the total switching function $S_{\text{total}}(\omega)$ and the difference switching signals $S_{\text{diffi}}(\omega)$ are completely decoupled. Hence

$$|S_{\text{diffi}}(\omega)| |S_{\text{total}}(\omega)| \approx 0.$$

(12)

To avoid the circulation current between the paralleled legs, the load current should be equally distributed among the legs. The circulation current among the legs is caused by the imbalanced current distribution between the paralleled legs [24]–[25][26]. Since the switching frequency is much higher than the fundamental frequency, the average value of the inductor current in one switching period is employed to analyze the imbalanced current distribution between the legs. First, I_L^* is defined as the balanced average value of each leg current in one switching period. Hence, in the proposed paralleled modular ANPC-MLC comprising three paralleled legs per each phase, I_L^* is determined as

$$I_L^* = \frac{1}{3} \sum_{i=1}^3 I_{Li}$$

(13)

where I_{Li} is the average value of the i th leg current in one switching period. Hence, I_{Li} is determined as

$$I_{Li} = f_{\text{SW-Leg}} \int_{t_0}^{t_0+1/f_{\text{SW-Leg}}} i_{Li}(t) \cdot dt$$

(14)

where $i_{Li}(t)$ is the instantaneous value of the i th leg current. Moreover, the duty cycle for the i th leg is defined as

$$d_{Li} = d_L^* + \Delta d_{Li}$$

(15)

where d_L^* is the reference duty cycle provided by the input reference signal, which is equal for all the legs, d_{Li} is the duty cycle of the i th leg considering possible mismatch in the duty cycle calculation by the modulator, and Δd_{Li} is the difference between the reference d_L^* and the duty cycle of the i th leg d_{Li} .

In addition, the average value of the i th leg voltage V_{Li} with respect to the negative terminal of the dc link V_{DC}^- (not with respect to neutral) is defined as

$$V_{Li} = d_{Li} \cdot V_{DC}.$$

(16)

By applying a KVL to the loop between two legs, for example, leg 1 and leg 2

$$I_{L1} = \frac{1}{sL_{f1} + R_{f1}} [(V_{L2} - V_{L1}) + (sL_{f2} + R_{f2})I_{L2}]$$

(17)

where L_{fi} and R_{fi} are the i th leg inductor and its series resistance, respectively. By substituting (15) and (16) in (17), we get

$$\begin{aligned} I_{L1} - \frac{(sL_{f2} + R_{f2})}{(sL_{f1} + R_{f1})} I_{L2} \\ = \frac{1}{(sL_{f1} + R_{f1})} [(d_L^* + \Delta d_{L2} - (d_L^* + \Delta d_{L1}))V_{DC}]. \end{aligned}$$

(18)

With regard to the fact that L_{fi} and R_{fi} mismatches are normally less than 5%, it can be considered that $\frac{(sL_{f2} + R_{f2})}{(sL_{f1} + R_{f1})} \approx 1$. Hence

$$I_{L1} - I_{L2} = \frac{1}{(sL_{f1} + R_{f1})} [(\Delta d_{L2} - \Delta d_{L1})V_{DC}].$$

(19)

Regarding (19), the imbalance between the legs' currents depends on the following.

1. The leg inductor value L_f .
2. The series resistance of the leg inductor R_f .
3. Duty cycle deviation between the legs Δd_{Li} .

Accordingly, the duty cycle deviation plays a critical role in the current imbalance and circulation current between the legs. To overcome this issue, the two following conditions should be satisfied.

1. Switching harmonic clusters and sideband harmonics should be completely decoupled and separated from the current ripple and current balancing frequency of the leg inductor. As mentioned in (12), this

condition is satisfied by employing the proposed modulation method for the proposed paralleled modular ANPC-MLC.

2. The duty cycle should be calculated and updated every $1/3f_{SW-Leg}$. Unlike the traditional modulation methods in which the duty cycle is updated every $1/f_{SW-Leg}$, in the proposed modulation method for the proposed paralleled modular ANPC-MLC, the duty cycle is updated three times faster than the switching frequency. Hence, the utilized suggested oversampling method for updating the duty cycle value leads to minimizing or mitigating the duty cycle deviation between the legs.

Therefore, as another important outcome of the proposed modulation method, the equal distribution of the load current between the 3L-ANPC legs of each phase of the proposed paralleled modular ANPC-MLC is guaranteed. Moreover, the current ripple frequency in each leg inductor L_f is equal to f_{SW-Leg} .

SECTION IV. Design Considerations of the 1 MHz, 1 MW-Paralleled Modular ANPC Converter

A. Optimized 3L-ANPC Cell of the Proposed 1 MHz, 1 MW-Paralleled Modular ANPC Converter

The designed 3L-ANPC cell of the proposed 1 MHz, 1 MW-paralleled modular ANPC converter is depicted in Fig. 4. As shown in Fig. 4, the laminated busbar with decoupling film capacitors is designed to minimize the overall loop inductance of the busbar. To decrease the overall loop inductance, the total equivalent series inductance (ESL) of the film capacitors, weight, and price as well as to increase the power density of the optimized 3L-ANPC cell, distributed-paralleled film capacitors configuration has been used. Moreover, to further decrease the overall loop inductance, two adjacent decoupling capacitors are placed in the opposite direction.

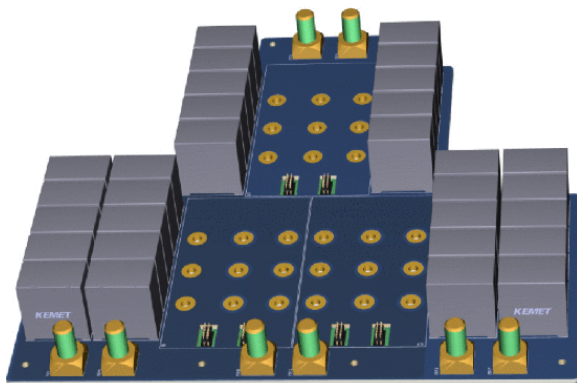


Fig. 4. Optimized 3L-ANPC cell of the proposed 1 MHz, 1 MW-paralleled modular ANPC converter.

B. Commutation Loops in One 3L-ANPC Cell of the Proposed Paralleled Modular ANPC Converter

The equivalent circuit and corresponding commutation loops of one 3L-ANPC leg of the proposed paralleled modular ANPC converter by considering the parasitic inductances of the loops are shown in Fig. 5. In Fig. 5, the LF power switches are shown in the green color, while the HF power switches are shown in the red color. Fig. 5 presents three main HF current commutation loops, including the parasitic inductances that are inherently formed as a result of the modulation scheme. Fig. 5(a) shows the current commutation loop as a result of commutation between the HF switches S_3 and S_4 during the positive and negative half cycles. Fig. 5(b) presents the commutation of current during the zero-crossing event of the fundamental

waveform. The commutation loops of the inverter include the following components: Switching devices, dc-link capacitors, and interconnecting busbars. Commutation loops 1 and 2 contain four power switches, a dc-link capacitor, and four busbar components. Commutation loop 3 contains four switches, two dc-link capacitors, and three busbar components. Since loops 1 and 2 yield identical results, the extraction will be conducted for loops 1 and 3.

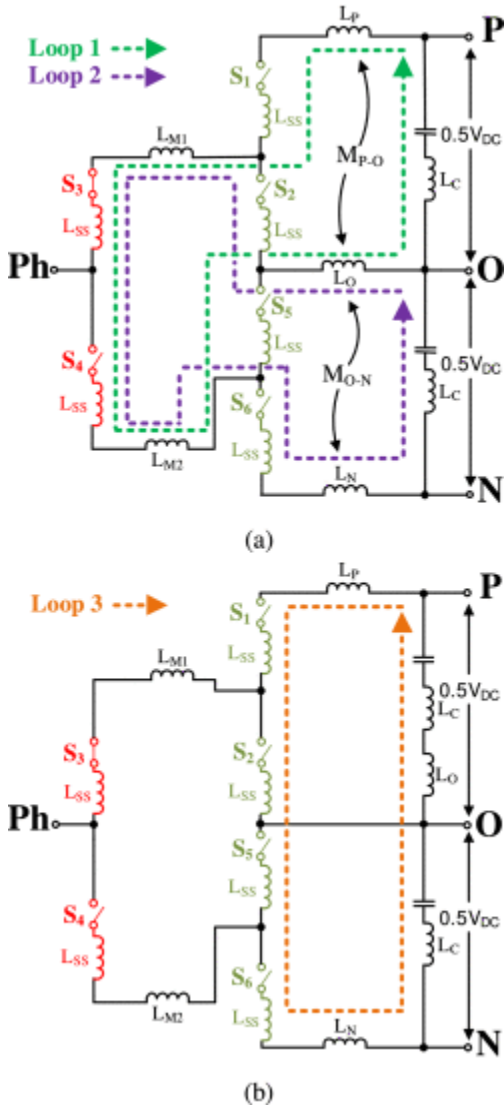


Fig. 5. Current commutation loops of the 3L-ANPC cell. (a) Current commutation loop as a result of commutation between the HF switches during the positive and negative half cycles. (b) Current commutation loop as a result of commutation between the LF switches during the zero-crossing event of the fundamental waveform.

The total loop inductance of each commutation loop is evaluated using the theory of partial inductances. Accordingly, each component of the loop can be characterized by a self-partial inductance (SPI) and mutual partial inductance (MPI). The SPI of each component is shown in Fig. 5. Moreover, as presented in Fig. 5(a), M_{P-O} is MPI between the positive busbar P and the neutral-point busbar O , and M_{O-N} is MPI between the neutral-point busbar O and negative busbar N . Furthermore, MPI between the switches and capacitors with the rest of the component is not considered since the switches and capacitors are not modeled in this study.

The loop inductance of each loop is a sum of the component's SPI and MPIs between the rest of the components. The MPI can have an additive or subtractive impact on the total loop inductance based on the direction of the current flow between the components. The MPI between the components of the loop in which the current flow is in the same direction is positive. Alternatively, the current flow in the opposite direction results in a negative MPI. A low inductance of the commutation loop is achieved by minimizing the SPI of the individual component while maximizing the subtractive MPI between the components. The SPI of the components, such as switches and capacitors, largely depends on the geometry and is hence fixed. The SPI of the busbar components can be manipulated and can be minimized through the optimized design. A compact integration of components leads to the shorter paths for the HF currents. Moreover, a straightforward solution to maximizing the subtractive MPI is through the interleaving of busbar layers [27]–[28][29].

C. Overall Stray Inductance Extraction of the 3L-ANPC Cell Busbar Using Ansys Q3D Finite Element Method (FEM) Analysis

The parasitic inductance extraction of the busbar components is achieved using the Ansys Q3D FEM analysis software. The Ansys Q3D platform efficiently performs the two-dimensional (2-D) and 3-D quasi-static electromagnetic field simulations to extract the partial inductance and resistance of the busbar. The simulation is setup through a proper connection of current sink/sources on multiple nets to direct the current flow according to the commutation loops.

As presented in Fig. 5(a), the overall loop inductance of loops 1 and 2 is equal. The simulation results show that the loop inductance of loops 1 and 2 is identical, and therefore, the calculation procedure of one can be applied to the other. Hence, the overall stray inductance of commutation loops 1, 2, and 3 are expressed as follows:

$$\begin{aligned} L_{\text{Loop},1} &= L_{\text{Loop},2} = L_{BB,1} + L_C + 4L_{SS} \\ L_{\text{Loop},3} &= L_{BB,3} + 2L_C + 4L_{SS} \end{aligned}$$

(20)(21)

where $L_{BB,1}$ and $L_{BB,3}$ are the overall stray inductances, including all SPI and MPI of the busbar, excluding the effects of SiC power switches and dc-link capacitors. The values of the $L_{BB,1}$ and $L_{BB,3}$ are obtained from the Ansys Q3D FEM analysis software. The stray inductance of the $L_{\text{Loop},1}$ is evaluated. The ac inductance estimation is conducted at the frequency f_{eval} , which is determined by the fall time t_f of the utilized CREE 1200 V/1050 A half-bridge SiC power module. For the utilized CREE 1200 V/1050 A half-bridge SiC power module, f_{eval} is 8.6 MHz. The stray inductance of the CREE 1200 V/1050 A half-bridge and dc-link capacitors are obtained from their respective datasheets and are reported in Table III. As depicted in Fig. 5(a), the commutation loop 1 consists of four busbar components ($N = 4$): positive busbar P , two middle busbars ($M1$ and $M2$), and the neutral-point busbar O . Moreover, as shown in Fig. 5(b), the commutation loop 3 consists of three busbar components ($N = 3$): positive busbar P , negative busbar N , and the neutral-point busbar O . The SPI of busbar components is listed as the diagonal elements $L_{i,i}$, while the MPI are present in off-diagonal elements $L_{i,j}$. The MPI can be positive or negative values depending on the current direction. The net inductance of each individual busbar component representing the contribution of that component to the total loop inductance is expressed as follows:

$$L_i = \sum_{j=1}^N \pm L_{i,j}.$$

(22)

TABLE III SPI of Utilized Components in One Cell of the Proposed 1 MHz, 1 MW-Paralleled Modular ANPC Converter

Component	Variable	Value (nH)
CREE 1200V/1050A Module	L_{SS}	3.75
DC-link Cap (Ten in parallel)	L_C	1.5

The total inductance $L_{BB,x}$ is the sum of the component net inductances L_i and is determined as

$$L_{BB,x} = \sum_{i=1}^N \sum_{j=1}^N \pm L_{i,j}$$

(23)

where x denotes the commutation loop. The total loop inductances are given by (20) and (21). The inductance matrices for $L_{BB,1}$ and $L_{BB,3}$ in this case are given in Tables IV and V. The results indicate that $L_{BB,1} = 9.85\text{nH}$ and $L_{BB,3} = 8.77\text{nH}$, from which the loop inductances are derived $L_{Loop,1} = 26.35\text{nH}$ and $L_{Loop,3} = 26.77\text{nH}$.

TABLE IV AC Partial Inductance Matrix for Loop 1

$L_{BB,1}$ (nH)	P	M1	M2	O
p	0.70	-0.52	0.30	-0.48
M1	-0.52	3.35	-1.86	1.93
M2	0.30	-1.86	8.89	-4.05
O	-0.48	1.93	-4.05	6.26

TABLE V AC Partial Inductance Matrix for Loop 3

$L_{BB,3}$ (nH)	P	N	O
p	0.72	-0.01	-0.25
N	-0.01	0.77	-0.25
O	-0.25	-0.25	8.34

D. Current Density Extraction and Thermal Analysis of the 3L-ANPC Cell Using Ansys SIwave and Ansys Icepak FEM Analyses

Ansys SIwave is a specialized design platform for power integrity, current distribution, and EMI analysis of HF electric circuits. The designed 3L-ANPC cell of the proposed 1 MHz, 1 MW-paralleled modular ANPC converter is simulated in Ansys SIwave platform to evaluate the current density and power integrity of the 3L-ANPC cell busbar at all possible switching states. In the proposed 1 MHz, 1 MW EV charger, the maximum dc-link current is set to the rated value for each 3L-ANPC cell. Moreover, Ansys Icepak FEM platform is used for the thermal analysis of the designed 3L-ANPC cell at the rated current for all possible switching states. It is worth mentioning that the designed busbar for the 3L-ANPC cell is considered with natural convection cooling and the ambient temperature is considered as $T_{amb} = 25^\circ\text{C}$. Figs. 6–9 present the results of the current density and thermal analyses of the designed 3L-ANPC cell for switching states 1–4, respectively. In Figs. 6–9, part (a) shows the

result of the current density analysis using Ansys Siwave FEM analysis platform and part (b) illustrates the result of the thermal analysis using Ansys Icepak FEM analysis platform.

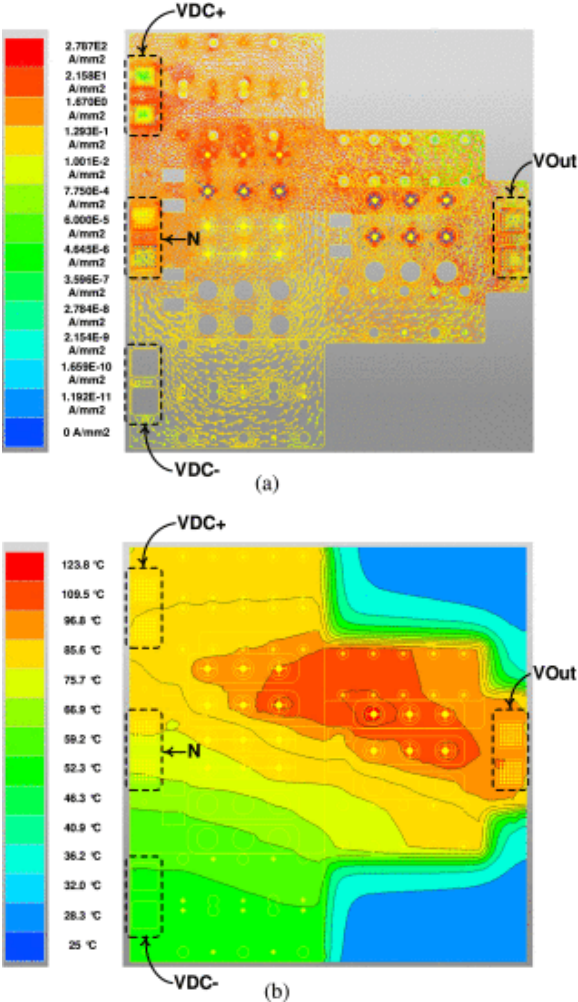


Fig. 6. Ansys Siwave and Icepak FEM analyses of the designed 3L-ANPC cell busbar for 1 MHz, 1 MW-parallel modular ANPC converter at switching state 1. (a) Current density analysis. (b) Thermal analysis.

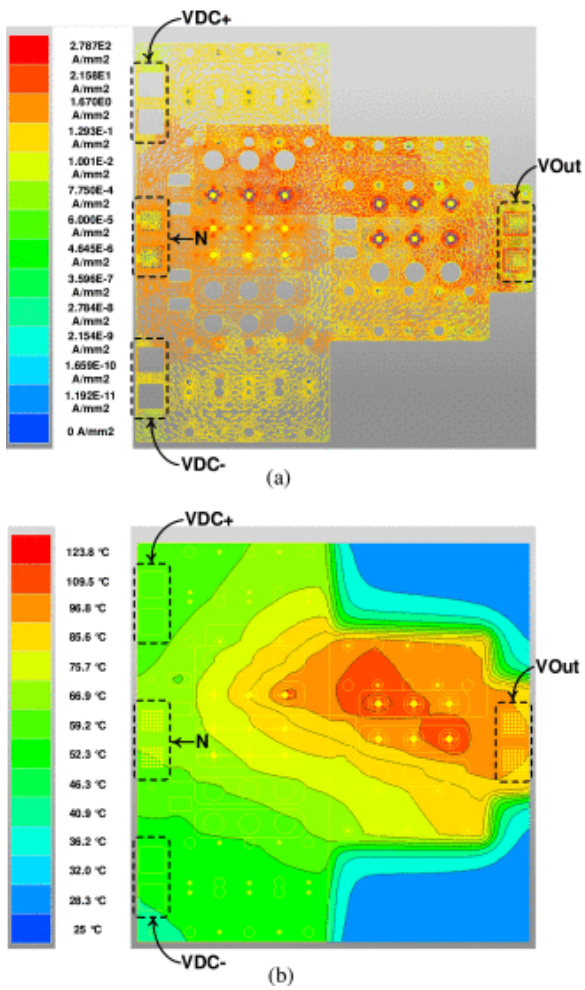


Fig. 7. Ansys Siwave and Icepak FEM analyses of the designed 3L-ANPC cell busbar for 1 MHz, 1 MW-paralleled modular ANPC converter at switching state 2. (a) Current density analysis. (b) Thermal analysis.

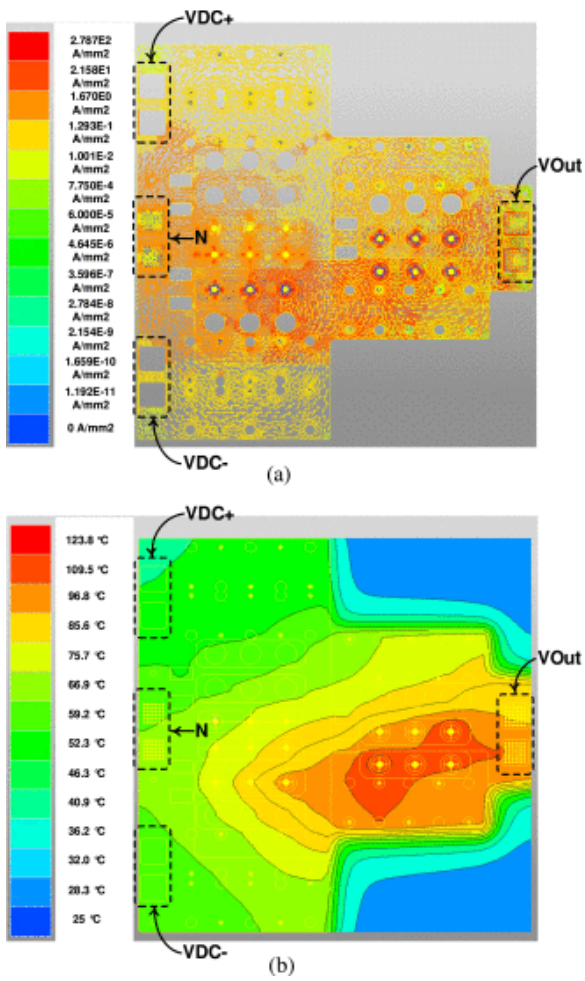


Fig. 8. Ansys SIwave and Icepak FEM analyses of the designed 3L-ANPC cell busbar for 1 MHz, 1 MW-parallel modular ANPC converter at switching state 3. (a) Current density analysis. (b) Thermal analysis.

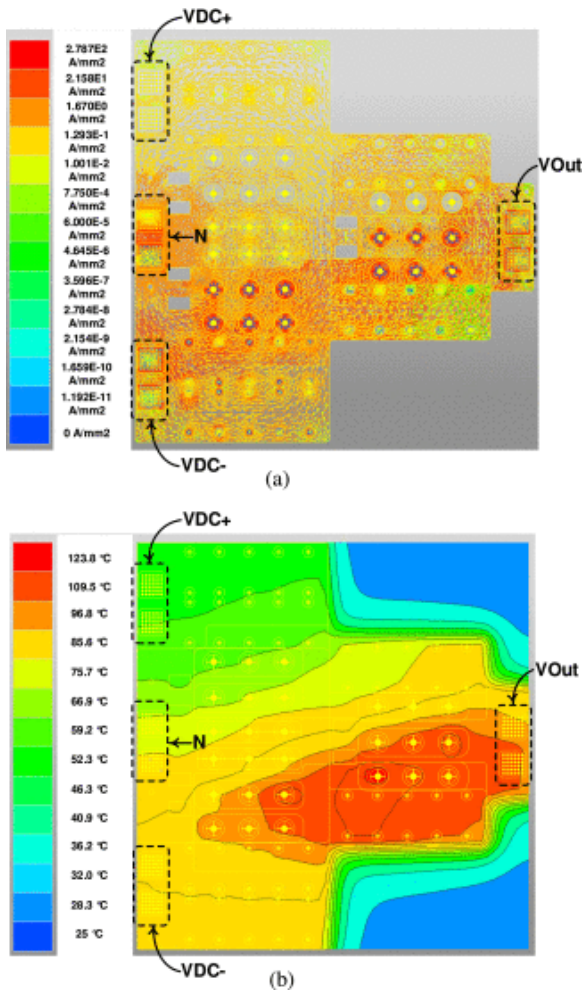


Fig. 9. Ansys SIwave and Icepak FEM analyses of the designed 3L-ANPC cell busbar for 1 MHz, 1 MW-paralleled modular ANPC converter at switching state 4. (a) Current density analysis. (b) Thermal analysis.

As shown in Figs. 6(a)–9(a), the current density is distributed in the dc-link busbar, and the maximum current density is notably decreased and is approximately equal at all the switching states. The value of the current density at all the switching states 1–4 is equal, is about $1.67\text{A}/\text{mm}^2$ for the dc-link busbar, and has a maximum value of $21.58\text{A}/\text{mm}^2$ at the input terminals and SiC power devices terminals. Moreover, as shown in Figs. 6(b)–9(b), the temperature is also distributed in the dc-link busbar and is decreased. The maximum temperature at all the switching states 1–4 is equal and is about $109.5\text{ }^\circ\text{C}$.

SECTION V. Proposed 1 MW, 1 MHz Three-Phase-Paralleled Modular ANPC-MLC Power Loss and Efficiency Evaluation, and Simulation Results

A. Power Loss Calculation and Efficiency Evaluation

To evaluate the conduction and switching loss of the proposed three-phase-paralleled modular ANPC-MLC controlled by the suggested improved modulation method, the conduction and switching loss model of CREE 1200 V/1050 A SiC MOSFET has been generated in MATLAB/Simulink. To characterize the switching losses of semiconductor devices, typically double pulse tests need to be conducted on the devices. The double pulse test hardware prototype has been built to extract the turn-on and turn-off switching losses of CREE 1200 V/1050 A SiC MOSFET. The voltage of the double pulse setup was swept from 100 to 1000 V in steps of 100 V. Similarly,

the current in the double pulse test was stepped from 100 to 1000 A in steps of 100 A. Figs. 10 and 11 present the 3-D turn-on and turn-off switching losses at different voltage and current operating points, respectively. The switching losses are increased as the voltage or current is increased.

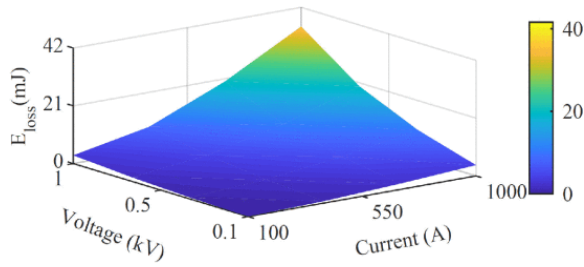


Fig. 10. Measured turn-on switching loss of CREE 1200 V/1050 A SiC MOSFET at different voltage and current operating points.

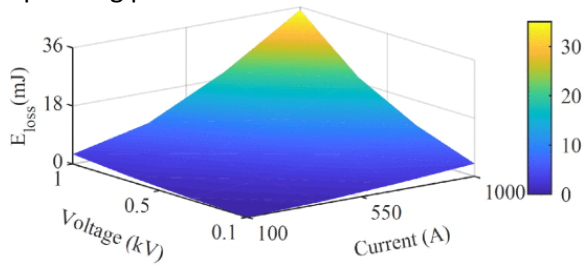
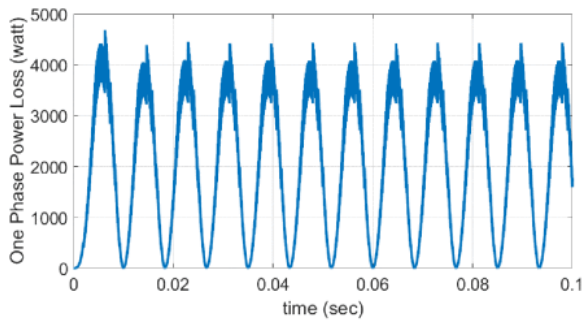
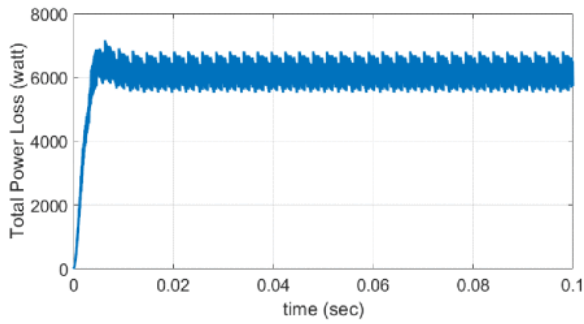


Fig. 11. Measured turn-off switching loss of CREE 1200 V/1050 A SiC MOSFET at different voltage and current operating points.

Moreover, on-state resistance R_{DS-ON} of CREE 1200 V/1050 A SiC MOSFET is 1.33 m Ω to calculate the conduction power loss. In the proposed paralleled modular ANPC-MLC, all the power devices are selected as CREE 1200 V/1050 A SiC MOSFET. The total power loss of the proposed paralleled modular ANPC-MLC operating at 1 kV, 1 MVA, and 1 MHz is presented in Fig. 12. Fig. 12(a) presents the total power loss of one phase of the proposed paralleled modular ANPC-MLC and Fig. 12(b) shows the total power loss of the proposed three-phase-paralleled modular ANPC-MLC. Based on the presented simulation results in Fig. 12, the total power loss of the proposed three-phase-paralleled modular ANPC-MLC by utilizing the CREE 1200 V/1050 A SiC MOSFETs operating at 1 kV, 1 MVA, and 1 MHz is 7000 W. Therefore, the efficiency of the proposed three-phase-paralleled modular ANPC-MLC is 99.3%.



(a)

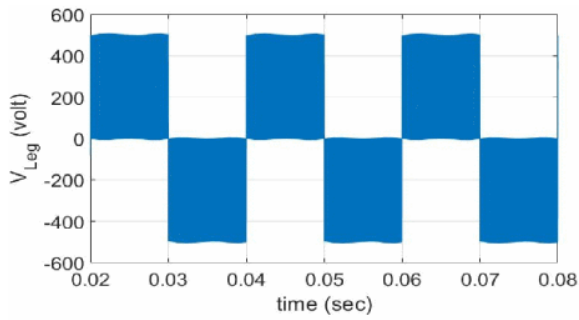


(b)

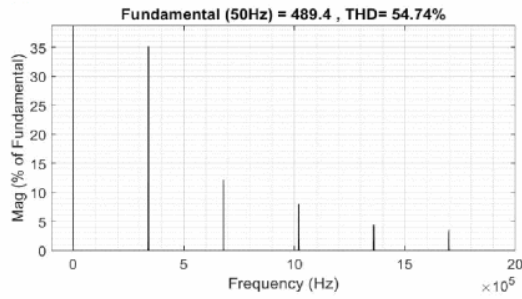
Fig. 12. Total power semiconductor loss of the proposed paralleled modular ANPC-MLC operating at 1 kV, 1 MVA, and 1 MHz by utilizing CREE 1200 V/1050 A SiC MOSFET. (a) Power loss of one phase of the paralleled modular ANPC-MLC. (b) Total power loss of three-phase-paralleled modular ANPC-MLC.

B. Simulation Results of the Proposed 1 MHz, 1 MW Three-Phase-Paralleled Modular ANPC-MLC

The simulation results of the proposed three-phase-paralleled modular ANPC-MLC operating at 1 kV dc-link voltage, 1 MVA, and 1 MHz are presented in this part. The output voltage and its fast Fourier transform (FFT) analysis of one 3L-ANPC cell, the phase-neutral voltage and its FFT analysis, and the line–line voltage and its FFT analysis of the proposed three-phase-paralleled modular ANPC-MLC operating at $f_{SW} = 340\text{kHz}$ by employing the proposed phase-shifted switching pattern are shown in Figs. 13–15.

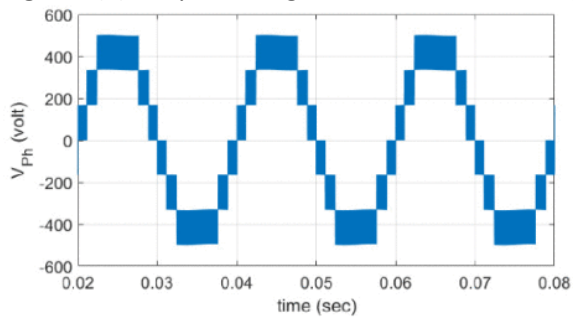


(a)

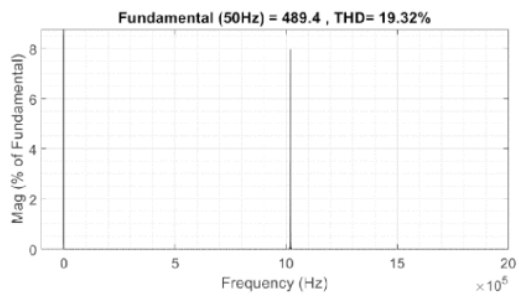


(b)

Fig. 13. (a) Output voltage of one 3L-ANPC cell. (b) Its FFT analysis.



(a)



(b)

Fig. 14. (a) Output phase-neutral voltage of one phase of the proposed three-phase-paralleled modular ANPC MLC. (b) Its FFT analysis.

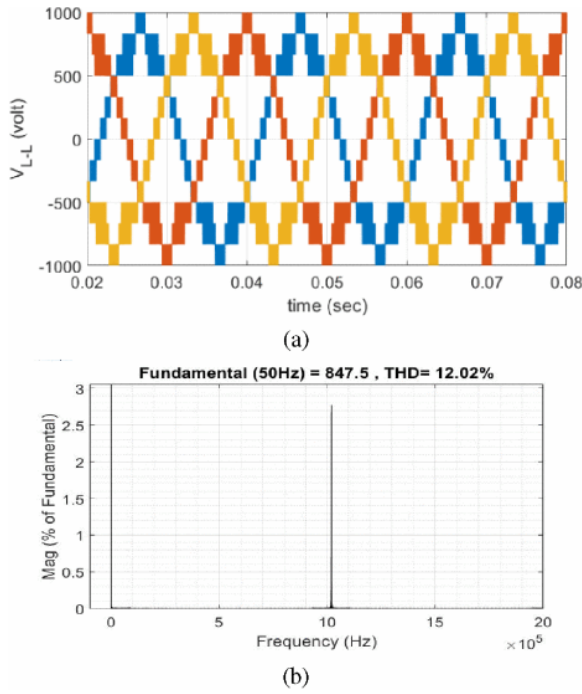


Fig. 15. (a) Output line–line voltage of the proposed three-phase-paralleled modular ANPC-MLC. (b) Its FFT analysis.

As presented in Figs. 13–15, by applying the proposed phase-shifted switching pattern, not only the first and second switching harmonic clusters are canceled out but also the number of output voltage levels are seven for phase neutral, and thirteen for line–line output voltages. Moreover, the amplitude of the first switching harmonic cluster is decreased from 35% of the fundamental amplitude to 8% of the fundamental amplitude for the phase-neutral voltage and to only 2.75% of the fundamental amplitude for the line–line voltage. Hence, the amplitude of the first switching harmonic cluster is remarkably decreased by applying the proposed switching pattern and thus the emitted EMI from the proposed paralleled modular ANPC-MLC is significantly reduced.

SECTION VI. Experimental Results

A. Single-Phase Seven-Level-Downscaled 50 kW Setup of the Proposed Paralleled Modular ANPC-MLC

The 50-kW downscaled experimental setup of the one phase of the proposed paralleled modular ANPC-MLC using SiC MOSFETs has been implemented to verify the feasibility and viability of the proposed configuration as well as the suggested modulation method. The implemented single-phase seven-level-downscaled setup of the proposed paralleled modular ANPC-MLC is shown in Fig. 16. The dc-link voltage is set to 1 kV dc, and the experimental results of the downscaled setup operating at first switching harmonic cluster frequencies of 450 kHz and 1 MHz at 1 kV dc-link voltage and 30 kW for the single-phase configuration are presented. Figs. 17 and 18 present the experimental results of the single-phase configuration of the proposed paralleled modular ANPC-MLC at 1 kV dc-link voltage and 30 kW, operating at first switching harmonic cluster frequencies of 450 kHz and 1 MHz, respectively. The leg voltages (Ch1, Ch2, and Ch3), phase voltage (Ch4), leg currents (Ch5, Ch6, and Ch7), load current (Ch8), one leg voltage FFT analysis (Math1), and output voltage FFT analysis (Math2) are presented in Figs. 17 and 18 for first switching harmonic cluster frequencies of 450 kHz and 1 MHz, respectively.

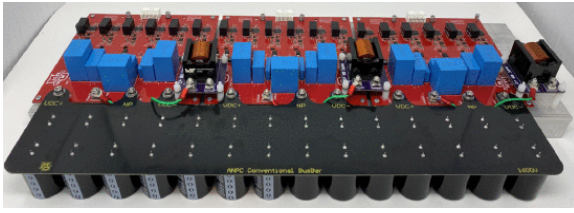


Fig. 16. Single-phase seven-level-downscaled 50 kW setup of the proposed paralleled modular ANPC-MLC.

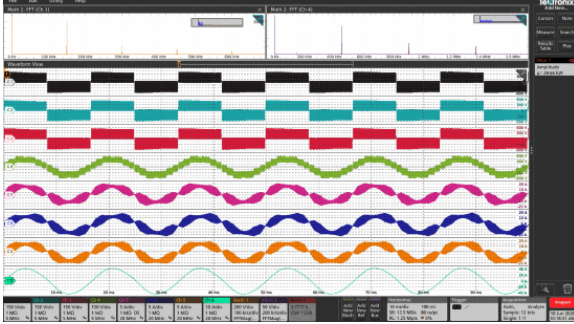


Fig. 17. Experimental results of the proposed paralleled modular ANPC-MLC for first switching harmonic cluster frequency of 450 kHz. Leg voltages (Ch1, Ch2, Ch3: 150 V/div), phase voltage (Ch4: 150 V/div), leg currents (Ch5, Ch6, Ch7: 5 A/div), load current (Ch8: 10 A/div), Math1: one leg voltage FFT analysis (Vertical: 200 V/div; Horizontal: 100 kHz/div), and Math2: output voltage FFT analysis (Vertical: 50 V/div; Horizontal: 200 kHz/div).

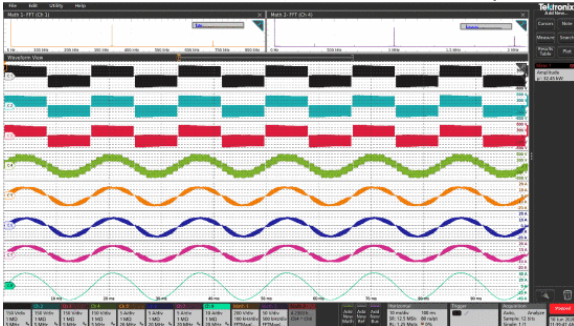


Fig. 18. Experimental results of the proposed paralleled modular ANPC-MLC for first switching harmonic cluster frequency of 1 MHz. Leg voltages (Ch1, Ch2, Ch3: 150 V/div), phase voltage (Ch4: 150 V/div), leg currents (Ch5, Ch6, Ch7: 5 A/div), load current (Ch8: 10 A/div), Math1: one leg voltage FFT analysis (Vertical: 200 V/div; Horizontal: 100 kHz/div), and Math2: output voltage FFT analysis (Vertical: 50 volt/div; Horizontal: 500 kHz/div).

As shown in Fig. 17, although the switching frequency is set to 150 kHz and considering the one leg voltage FFT analysis (Math1) in which the first switching harmonic cluster is around 150 kHz, as presented in Math2, the phase voltage has the first switching harmonic cluster around 450 kHz. Moreover, the output voltage has seven levels and the magnitude of the first switching frequency harmonic cluster is decreased by the factor of six. In addition, as shown in Ch5, Ch6, and Ch7 in Fig. 17, all three 3L-ANPC legs' currents are equal. Hence, the load current in Ch8 is equally distributed between all three 3L-ANPC legs.

In addition, as depicted in Fig. 18, although the switching frequency is set to 333 kHz and considering the one leg voltage FFT analysis (Math1) in which the first switching harmonic cluster is around 333 kHz, as illustrated in Math2, the phase voltage has the first switching harmonic cluster around 1 MHz. Moreover, the output voltage has seven levels and the magnitude of the first switching frequency harmonic cluster is decreased by the factor of six. Moreover, as presented in Ch5, Ch6, and Ch7 in Fig. 18, all three 3L-ANPC legs' currents are equal. Hence, the load current in Ch8 is equally distributed between all three 3L-ANPC legs.

As shown in Math1 of Figs. 17 and 18, the amplitude of the first switching harmonic cluster of each 3L-ANPC leg voltage is 200 V, whereas as presented in Math2 of Figs. 17 and 18, the amplitude of the first switching

harmonic cluster of the phase-neutral voltage of the proposed paralleled modular ANPC converter is only about 35 V. Hence, the amplitude of the first switching harmonic cluster is decreased by the factor of six and thus the emitted EMI is remarkably decreased in the proposed paralleled modular ANPC-MLC. The voltage of one leg of the proposed paralleled modular ANPC-MLC has the first switching harmonic cluster around 333 kHz, the voltage THD is 54.74%, and the magnitude of the first switching harmonic cluster is 40% of the fundamental output voltage. The one phase of the proposed paralleled modular ANPC converter has seven levels at the output voltage, the phase-voltage THD is 19.32%, and the magnitude of the first switching harmonic cluster is only 7% of the fundamental output voltage. Moreover, the first and second harmonic clusters are canceled out by employing the proposed switching pattern, and the first switching harmonic cluster is shifted to 1 MHz.

With respect to the leg currents in Figs. 17 and 18, the load current is equally distributed between the legs by employing the proposed switching method. Furthermore, the load current is pure sinusoidal in both case studies. Only the current ripples of the legs vary by changing the switching frequency.

Considering Figs. 17 and 18, the current ripples of the leg currents are notably reduced by increasing the switching frequency, which means that it is possible to decrease the value of inductors to obtain a higher power density.

Therefore, considering the presented experimental results, by utilizing the proposed paralleled modular ANPC-MLC and the suggested enhanced switching pattern, by employing only 6 HF power switches operating at 333 kHz and $V_{dc}/2$, the expected 1 MHz switching frequency spectrum is achieved. Moreover, the magnitude of the first switching harmonic cluster is decreased from 40% to only 7% in each phase, which means the emitted EMI and the size of the required EMI filter are notably decreased. Therefore, the power density of the proposed converter is remarkably increased.

B. Optimized 3L-ANPC Cell of the Proposed 1 MHz, 1 MW-Paralleled Modular ANPC-MLC

The designed optimized 3L-ANPC cell of the proposed 1 MHz, 1 MW-paralleled modular ANPC-MLC in Section IV has been implemented. The proposed three-phase 1 MHz, 1 MW-paralleled modular ANPC-MLC is comprised of nine optimized 3L-ANPC cells. Hence, the experimental results of one optimized 3L-ANPC cell operating at 1 kV, 190 A, 200 kHz, and 200 kW are presented. The experimental results of the switching cycles and switching transient of the implemented optimized 3L-ANPC cell operating at 1 kV, 190 A, 200 kHz, and 200 kW are shown in Fig. 19. As presented in Fig. 19, the voltage overshoot across the drain-source of HF switch S4 during the switching transient is only 10% and the voltage overshoot at the output of the 3L-ANPC converter during the switching transient is only about 20%.

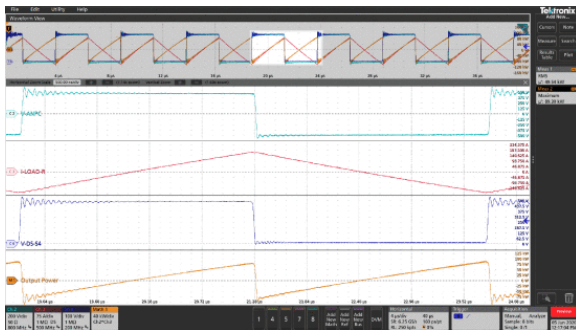


Fig. 19. Experimental results of the switching cycles and switching transient of the new optimized 3L-ANPC cell operating at 1 kV, 190 A, 200 kHz, and 200 kW. The 3L-ANPC cell output (Ch2: 200 V/div), load current (Ch3: 75 A/div), voltage across the drain and source of S4 (Ch6: 100 V/div), and output power (Math1: 40 kW/div).

Accordingly, provided experimental results for both the single-phase seven-level-downscaled setup of the proposed paralleled modular ANPC-MLC and the designed optimized 3L-ANPC cell verify the performance,

feasibility, and viability of the proposed configuration, its improved modulation method, and the optimized designed high-power 3L-ANPC cell.

SECTION VII. Conclusion

The paralleled modular ANPC-MLC as well as its improved modulation method was proposed for the three-phase 1 MHz, 1 MW EV megacharger. The 1 MHz frequency spectrum is achieved by utilizing only six HF SiC MOSFETs operating at 333 kHz in each phase. Each phase generates seven-level output voltage and the magnitude of the first switching frequency harmonic cluster is decreased by the factor of five. Moreover, the load current is equally distributed between all the 3L-ANPC legs by employing the proposed improved modulation method. Hence, the modularity, efficiency, and power density of the proposed converter were notably increased, whereas the value of passive components and the overall switching loss were remarkably decreased. The optimized design of the one 3L-ANPC cell of the proposed paralleled modular ANPC-MLC for 1 MHz, 1 MW EV megacharger using Ansys Siwave, Icepak, and Q3D FEM platforms was performed and described. The presented experimental results verified the feasibility of the proposed configuration and the performance of the suggested improved switching pattern.

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