A New Current Mirror Layout Technique for Improved Matching Characteristics

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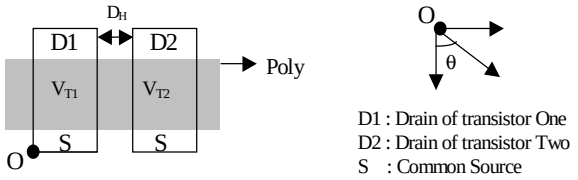
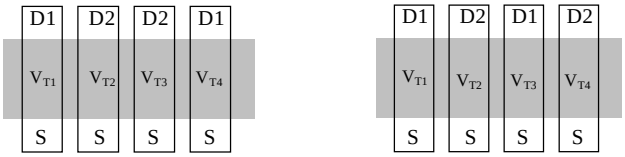
***Abstract*-This paper proposes a new current mirror layout technique to improve matching characteristics in the presence of parameter gradient. Effects of threshold gradients across a mirror on the matching characteristics of current mirrors are discussed. New and the existing layouts are compared with computer simulations for threshold voltage gradients at all angles across the active area. Results show a significant improvement in matching characteristics of the proposed structures over what is achievable with existing layout techniques.**

I. INTRODUCTION

The performance characteristics of many linear and mixed-signal integrated circuits are dominated by the matching characteristics of current mirrors and differential amplifiers. The matching characteristics of these two essential circuit elements can be attributed to systematic and random variations in both geometric parameters and process parameters. The random variations are easy to model and tradeoffs can be made between area and performance to compensate for random variations in these parameters. It is often more difficult to compensate for the systematic parameter variations and some of these are often mistakenly assumed to be random (an assumption that can cause significant errors in a statistical analysis because of the inherent correlation of these parameters). Some recent work by Felt et. al, [1] shows that the magnitude of the matching errors associated with the systematic parameter variations are comparable to that of the random parameter variations even with good layout strategies. We believe that the impact of not correctly handling the systematic parameter variations is even more significant than suggested by Felt et. al, in the design of high-end linear circuits. Systematic variations include mobility (μ), C_{OX}, threshold voltage (V_T) and γ variations. In this paper, only V_T variations have been considered for various layouts to compare matching characteristics but the reduced sensitivity to gradients in other parameters parallel that observed for V_T gradients in the proposed structure. Five different existing layout techniques for current mirrors are shown in Fig. 1. Fig. 1a shows the simple layout technique. Although parameter gradients that occur in the direction from drain to source (designated as "vertical" in Fig. 1) cause no device matching problem with this structure, the matching performance degrades substantially if there are substantial "horizontal" components (relative to Fig. 1) of the gradient. The interdigitized layout structures of Fig. 1b and Fig. 1c have a reduced sensitivity to horizontal components of the gradient but the gradient effects are still substantial. The common centroid layouts of Fig. 1d and Fig. 1e generally offer better matching performance than the other structures presented in the figure. The common centroid layout technique is currently being widely used since it reduces systematic gradients when compared to the simple and interdigitized techniques. The proposed technique improves matching characteristics over what is achievable with the common centroid technique.

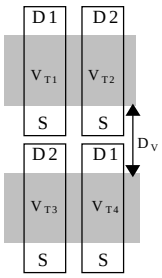


(a) Simple Technique

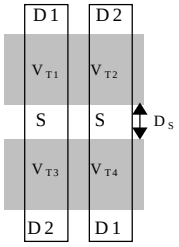


(b) Interdigitized Type I

(c) Interdigitized Type II



(d) Common Centroid Type I



(e) Common Centroid Type II

Figure 1. Existing Current Mirror Layout Techniques

II. GRADIENT MODELING

In this section, the effects of threshold voltage gradients on the matching performance of current mirrors are investigated. In particular, the effects of threshold voltage gradients at any angle across a wafer for interdigitized and common-centroid geometries are compared with the matching characteristics of a simple mirror layout. The parameter gradients are modeled in a distributed way through the active devices themselves. The simulation results show that the matching characteristics are strongly a function of the angle of the threshold voltage gradient across a die and that, for any angle, the effects of the threshold gradient for the common centroid layout is small. The results also show, in contrast to the well-accepted premise that the effects of linear gradients can be readily modeled [2] and are inherently canceled in common centroid structure [1], that the threshold gradients through the devices themselves create an angle-dependent gradient even in common centroid structures that assumes a maximum at a 45° angle through a simple common centroid layout comprised of square unit transistors.

The widely used approach for predicting the effects of the threshold gradient is based upon deriving an equivalent threshold voltage [3] for the devices as given by the following equation.

$$V_{Teq} = \frac{\int_{active\ \ area} V_T(x,y)\ \ dxdy}{Active\ \ \ \ Area} \qquad (1)$$

If the threshold gradient amplitude is α and the gradient direction is θ as indicated in Fig. 1, it follows that for a simple current mirror structure (Fig. 1a):

$$V_{T1} = V_{TN} + \frac{\alpha W}{2}\sin\theta - \frac{\alpha L}{2}\cos\theta \qquad (2)$$

$$V_{T2} = V_{TN} + \alpha(\frac{3W}{2} + D_H)\sin\theta - \frac{\alpha L}{2}\cos\theta$$

where D_H is the minimum separation, usually 4 lambda, between the two drain diffusions, D1 and D2, V_{T1} and V_{T2} are the threshold voltages of the two transistors of equal sizes W/L and V_{TN} is the threshold voltage at the base point O in Fig. 1a. If the equivalent V_T equation (1) is applied to Type I interdigitized layout (Fig. 1b), the transistors One and Two have the same threshold voltage given by the following equation.

$$V_{TD1} = V_{TD2} = V_{TN} + \alpha(W + \frac{3D_H}{2})\sin\theta - \frac{\alpha L}{2}\cos\theta \qquad (3)$$

This indicates that perfect matching can be achieved using this structure. However, experimental results in the past have not been in accordance with the above conclusion. If a segmented integral approach is used instead of equation (1), we see that there exists an angle (θ) dependent mismatch which is consistent with experimental results and hence this would be a better approach to approximate the true behavior of current mirrors. In the segmented integral model, the V_T's of all individual unit transistors are calculated separately and resultant lumped devices are then placed in parallel. Using this approach, the threshold voltages for the simple structure remain the same as before, while those of the four unit transistors for the Type I interdigitized structure are given by,

$$V_{T1} = V_{TN} + \frac{\alpha W}{4}\sin\theta - \frac{\alpha L}{2}\cos\theta \qquad (4)$$

$$V_{T2} = V_{TN} + \alpha(D_H + \frac{3W}{4})\sin\theta - \frac{\alpha L}{2}\cos\theta$$

$$V_{T3} = V_{TN} + \alpha(2D_H + \frac{5W}{4})\sin\theta - \frac{\alpha L}{2}\cos\theta$$

$$V_{T4} = V_{TN} + \alpha(3D_H + \frac{7W}{4})\sin\theta - \frac{\alpha L}{2}\cos\theta$$

where V_{T1} and V_{T4} correspond to the two unit transistors of "Transistor One" and V_{T2} and V_{T3} correspond to the two unit transistors of "Transistor Two". The four expressions also hold for Type II interdigitized layout (Fig. 1c) where V_{T1} and V_{T3} correspond to the two unit transistors of "Transistor One" and V_{T2} and V_{T4} correspond to the two unit transistors of "Transistor Two". Similarly, threshold voltages for the four unit transistors were determined for the common centroid Type I (Fig. 1d) and Type II (Fig. 1e) and are given by,

$$V_{T1} = V_{TN} + \frac{\alpha W}{4}\sin\theta - \alpha(D_{V/S} + \frac{3L}{2})\cos\theta \qquad (5)$$

$$V_{T2} = V_{TN} + \alpha(D_H + \frac{3W}{4})\sin\theta - \alpha(D_{V/S} + \frac{3L}{2})\cos\theta$$

$$V_{T3} = V_{TN} + \frac{\alpha W}{4}\sin\theta - \frac{\alpha L}{2}\cos\theta$$

$$V_{T4} = V_{TN} + \alpha(D_H + \frac{3W}{4})\sin\theta - \frac{\alpha L}{2}\cos\theta$$

where D_V and D_S are the minimum required distances between the two channels as shown in Fig. 1d and Fig.1e respectively. The above equations were used to plot the mismatch for the five mirror layouts and for $0 \le \theta \le 360°$, V_{TN}=0.8V, α=0.5mV/um, W=40um, L=40um, and D_H=4um as shown in Fig. 2. For a fair comparison, mismatch for all the structures were measured with the same active area, W/L and D_H. Mismatch is defined by,

$$Mismatch = \frac{I_{D2} - I_{D1}}{I_{D1}} x100\ \ \% \qquad (6)$$

From Fig. 2 it can be seen that interdigitized Type I, common centroid Type I and Type II have very good matching characteristics relative to the other two structures. An expanded view of the latter three results is shown Fig. 3. It is evident that the interdigitzed Type I layout has mismatch characteristics with maximum values at θ = 90° and 270°. Common centroid I and II have better and similar matching performance with maximum mismatch values at θ = 45°, 135°, 225° and 315°.

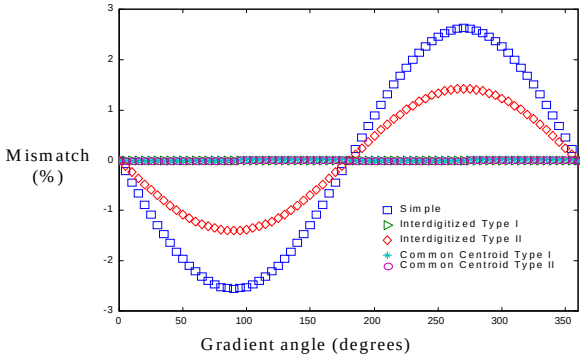


Figure 2. Comparison of Simple, Interdigitized and Common Centroid techniques

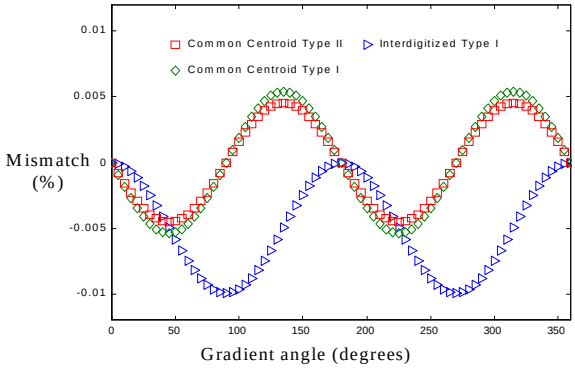


Figure 3. Comparison of Interdigitized and Common Centroid techniques in closer detail

III. PROPOSED TECHNIQUE

A new structure that offers improvement over what is achievable with the common centroid technique is shown in Fig. 4a. The proposed technique attempts to minimize the mismatch at 45°, 135°, 225° and 315° angles, at which common centroid structures exhibit maximum mismatch. In the common centroid technique, the layout is the same when we rotate it by 180°, thus canceling the mismatch at 90° while having a maximum at 45°. In the proposed technique, the layout is the same when we rotate it by 90°, thus canceling the mismatch at 45°. In the proposed structure, each transistor is divided into 4 unit transistors and since the source and the gate are common for the current mirror, we share the source and gate for all the eight unit transistors.

The segmented integral approach was used to evaluate the matching characteristics of the proposed technique similar to the analysis done for the existing layout techniques in the previous section. The V_T's of eight unit transistors in Fig. 4a are given by:

$$V_{T1} = V_{TN} + \alpha(L + D_H + \frac{W}{8})\sin\theta - \alpha(3D_H + \frac{W}{2} + \frac{3L}{2})\cos\theta \quad (7)$$

$$V_{T2} = V_{TN} + \alpha(L + 2D_H + \frac{3W}{8})\sin\theta - \alpha(3D_H + \frac{W}{2} + \frac{3L}{2})\cos\theta$$

$$V_{T3} = V_{TN} + \alpha(3D_H + \frac{W}{2} + \frac{3L}{2})\sin\theta - \alpha(L + 2D_H + \frac{3W}{8})\cos\theta$$

$$V_{T4} = V_{TN} + \alpha(3D_H + \frac{W}{2} + \frac{3L}{2})\sin\theta - \alpha(L + D_H + \frac{W}{8})\cos\theta$$

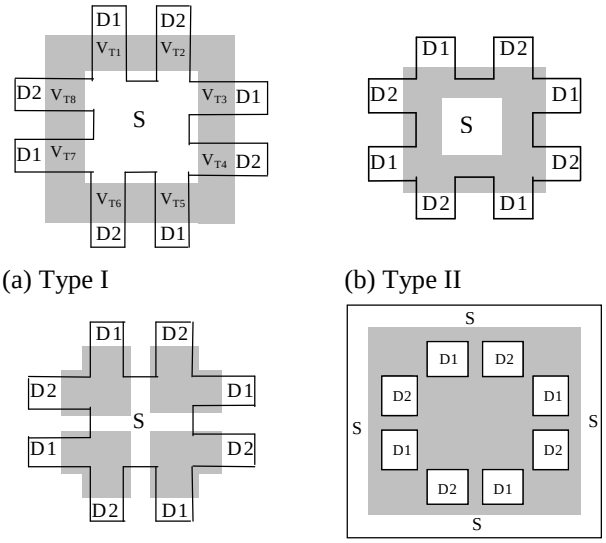
$$V_{T5} = V_{TN} + \alpha(L + 2D_H + \frac{3W}{8})\sin\theta - \frac{\alpha L}{2}\cos\theta$$

$$V_{T6} = V_{TN} + \alpha(L + D_H + \frac{W}{8})\sin\theta - \frac{\alpha L}{2}\cos\theta$$

$$V_{T7} = V_{TN} + \frac{\alpha L}{2}\sin\theta - \alpha(L + D_H + \frac{W}{8})\cos\theta$$

$$V_{T8} = V_{TN} + \frac{\alpha L}{2}\sin\theta - \alpha(L + 2D_H + \frac{3W}{8})\cos\theta$$

Using the above it was found that the mismatch for the proposed technique was zero at 45°, 90°, 135°, 180° and so on, giving a big improvement in matching characteristics over that of common centroid technique. The disadvantage of the proposed technique is the requirement of more silicon-area. Three other layouts based on the proposed technique with better area budgets are shown in Fig. 4b, 4c and 4d. Each layout-configuration has different area requirements with similar matching characteristics to that of Fig. 4a. It is tedious to fairly compare the four matching-enhanced layouts, since it is not difficult to maintain the same active area and drain currents in all layouts. Further investigation is ongoing to compare the four layouts and the trade-off between area and performance.



(a) Type I (b) Type II

(c) Type III (d) Type IV

Figure 4. Matching-Enhanced Current Mirror Layout Techniques

IV. SIMULATION RESULTS

For the same reason the segmented integral approach gives incorrect results with segmented transistors, even the errors caused by the segmented integral model become significant when close matching is expected. A simulator [4] was developed for predicting matching characteristics in the presence of either linear or non-linear gradients through the active area of the devices. It uses a finite lumped-element model approach more accurately than is attained with the segmented approach. The simulator can be used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in threshold voltage or any other process parameters.

The proposed structure (Fig. 4a), interdigitized Type I, common centroid Type I and Type II were simulated using the simulator and the mismatch characteristics are shown in Fig. 5. In this simulation, the same parameters as that mentioned in the section II are used. It can be seen that the proposed technique improves the matching performance by at least two orders of magnitude over what is achievable with the common centroid layouts. Table 1 summarizes the worst case mismatch in the structures simulated. The maximum achievable resolution is calculated from the results of the simulator such that the worst case mismatch is less than ½ LSB for a relative full-scale (for the N-bit resolution ½ LSB = $1/2^{N+1}$). It can be seen that common centroid structure can achieve only about 13-bit resolution while the proposed structure can achieve 25-bit resolution showing a big improvement in matching with the new layout. The above results are valid only for a linear gradient of 0.5mV/µm and resolution would be lower if the gradient is non-linear.

V. CONCLUSION

A new current mirror layout technique has been proposed that offers improvement in matching characteristics over the simple, interdigitized and common centroid structures. Simulation results showed an improvement in matching by at least two orders of magnitude in the presence of linear gradient for the test structures. A comparison of the performance of several layout structures shows substantial differences in the sensitivity of the mirror gain due to parameter gradients.

ACKNOWLEDGEMENTS

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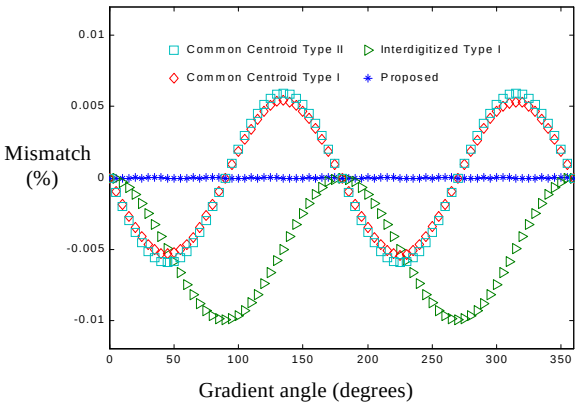

Figure 5. Comparison of Interdigitized, Common Centroid and Proposed techniques

Table 1. Comparison of various structures with a linear gradient of 0.5mV/um

Structure	Worst Mismatch (%)			
	Simple integral model	Segmented integral model	Distributed simulator	Resolution
Simple	2.6221	2.6221	2.6190	4-bit
Interdigitized Type I	0	9.9643e-3	9.9416e-3	5-bit
Interdigitized Type II	1.4218	1.4217	1.4201	12-bit
Common centroid Type I	0	5.3979e-3	5.4560e-3	13-bit
Common centroid Type II	0	4.5675e-3	5.9501e-3	13-bit
Proposed Structure (Fig. 4a)	0	2.2631e-14	1.2677e-6	25-bit

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