A New Design Flow and Testability Measure for the Generation of a Structural Test and BIST for Analogue and Mixed-Signal Circuits

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Abstract

For the generation of defect-oriented tests a system is developed that includes the synthesis of self-test structures. With the objective to generate a highly efficient analogue test, the fault simulation methods are greatly enhanced: (1) A new testability measure, (2)the possibility to distinguish between not-to-detect and hard-to-detect faults with respect to the tolerances of the respective measurement system. By presenting a new design flow and using the fault simulation in a very early design stage a tool-suite is developed. It allows to control the defect-robust layout and to eliminate those faults that limit the efficiency of a measurement system. This allows for economic self-test applications! It is demonstrated that the system finds the most efficient and less expense test for a given fault set. With the presented results it is possible to include the defect-oriented approach from the fault simulation to the automatic generation of layout rules and the test synthesis in an industrial design flow.

1. Introduction

Growing chip sizes and very large scale integration enabled the design of highly complex mixed-signal circuits and complete systems on silicon (SOC). Testing these circuits is more and more limited by severe restrictions on observability and controllability. Thus, structural (defect-oriented) approaches together with self-test implementations (DFT, BIST) to test the *digital* parts already help to solve these problems and belong to the state of the art. However, since ever smaller structure sizes and larger die areas are used, the test of the analogue circuit parts emerges as a dominant test problem to maintain low test costs and a high test quality. To guarantee and test the related analogue circuit specifications the application of analogue test stimuli as well as the observation of the analogue test answer becomes costly and sometimes impossible. As a result, also in the analogue domain the structural approaches emerge as an important complement to develop tests and test structures for those most challenging mixed-signal systems. Moreover, the implementation of DFT and BIST structures is mandatory for tomorrow‘s analogue circuit design.

The approaches which implement specific DFT structures in the analogue part of the mixed-signal design are various. In [90Wey] and [95ShieW] analogue register chains, similar to scan paths in the digital domain, are used to enhance the controll- and observability. More in the area of test pattern generation are those approaches that propose test circuits in conjunction with certain test stimuli to control the respective analogue DUT [96ChatKN], [97RenoAB]. A review can be found in [98Milo].

In recent years researchers spent much work on BIST techniques for analogue and mixed-signal circuits. In [91Ohle] for the first time a self test structure using the digital test components (e.g. BILBOs) to test the analogue parts was proposed and refined in [94NagiC], [95DammA]. For converter testing efficient solutions were proposed by [97SuntN] and [96ToneR]. Also the usage of an on-chip available DSP-core can be exploited [93TeraKY]. More recently, methods to make on-chip measurements of the analogue part have been proposed with the O-BIST by [97ArabKb], a method that has been used successfully in digital circuits [82BuehS], and with the T-BIST by [93SlamK]. For all these efforts it has to be mentioned that only the latter two approaches are capable of testing specifications of large analogue circuits without a principle limitation to certain circuit classes.

The structural approach, that is to test against defects, is used in a number of the investigations mentioned above. With the goal to prove a certain fault coverage it can be observed that the analogue defect-oriented testing gains an increasing industrial relevance. But, although the underlying concepts and investigations on tools for fault modelling ([85FantM], [91Ohle]), fault listing ([85ShenMF], [96Ohle], [99HoffSM]) and fault simulation ([00StraMV], [98HoffB], [99BartB]) are highly developed these approaches are seldom used for more than the calculation of an additional test quality measure *after* the traditional tests have been determined. Unlike in the digital domain, so far neither the test stimuli generation nor the design and layout of analogue circuits is based on defect-oriented investigations or automated defect-oriented tools.

To enable the further automation of the structural test approach for analogue circuits and to develop an algorithm to calculate and synthesize a highly efficient structural test and self-test, two problems are solved in this paper, based on the data of a fault simulation.

- Determination of a test and self-test with the highest possible fault coverage based on the electrical tolerances of the circuit and of the measurement

system.(pattern grading and test answer evaluation)

S Inclusion and control of the application of a defect-robust layout to increase the test quality (fault coverage) and to decrease the necessary precision of the measurement system.

The test answer evaluation method used in this paper to reach the above goals is based on transient response measurements. In [98Hoff] and [99RayaVN] the use of detection windows was proposed. Within this paper the detection window approach will be extended by new algorithms to enable the efficient automatic test generation and the hardware synthesis of a BIST! The approach is defect-oriented and the analogue fault simulator AnaFAULT [98HoffB] will be applied. The fault simulation results will be used by the new developed tool BistFAULT to analyse the test answers and to generate the self-test measurements and hardware. Similar approaches to basically exploit DC measurements for fault detection are known ([79HochB], [88MarlA], [94DevaS], [95IhsD]) but have not been used for the generation and optimisation of the related test and self-test. The problem especially for self-testing is that not every single measured test response can be compared with its respective known good response. The necessary memory effort and time consumption would be too large. Moreover, test response compaction like signature generation (MISR) for digital signals is not applicable due to the nature of analogue signals. To the knowledge of the author so far no structure has been developed to enable the automatic generation *and* hardware synthesis of a test and built-in self-test for mixed-signal circuits. Additionally, the method to automatically control a defect-robust layout to generate an area and cost efficient self-test is proposed for the first time [01Hoff].

This paper is organized as follows: In chapter 2 the new approach to generate and analyse the analogue fault simulation data including the new testability measure and detection criterion is introduced. Chapter 3 describes the application of the classification of hard-to-detect faults and the proposed design flow using the automatic determination of the *necessary* defect-robust design rules. In a case study a VCO is used in chapter 4 to prove the applicability of the methods and to describe the developed CAD tools (xFAULT-Tools) to be used for the automatic analogue test, BIST-hardware and layout rules generation.

2. Analogue fault simulation approach

The process of the defect-oriented analogue fault simulation can be divided into the tasks fault list generation, fault injection, fault simulation and calculation of the fault coverage. The latter is typically defined as the number of detectable faults over the number of all considered faults. So far this concept has hardly been used for more than test evaluation instead for test generation. To enable the automatic test generation the known methods have to be modified and investigated for their applicability and new measures and analyses have to be developed.

2.1. Fault list generation

Obviously the quality of the fault simulation results highly depends on the set of considered faults and, thus, on the method to ensure that only physically likely (layout-realistic) faults are analysed. This is true as far as the circuit, layout and test system has been already developed and a structural test measure was required, afterwards eventually resulting in certain redesign activities. But with this flow the potential of the structural test generation is not exploited, that would be to use the derived fault detectability information already in parallel to the circuit design and prior to the layout! The advantage would be to include the design of optimal (100% FC) and highly effective (small overhead, simple measurement functions) self-test structures in the circuit design and the possibility to control a defect-robust layout of specific critical elements. In this early design phase we propose to make use of the ‚local hard fault model' [89Ohle] with a fixed number of faults per element to enable the comparison of the fault coverages of different measurement and structural test systems.

A resistor model will be used for all shorts between two nodes at a time and opens at every node. The values for the ‚shorts' and ‚opens' have been chosen to be 20 Ohm and 1 Megohm. It is very important to note, that these values as well as the fault model itself are variable parameters of the fault simulation process and can be changed or extended locally per element on the basis of new technology or process data. But its intention is similar to the approaches in the digital domain to define a fault set, modelling the vast majority of all electrical failure mechanisms, to enable the reasonable usage of a fault coverage measure and thus to build the basis for test generation methods.

2.2. A new testability measure for test generation

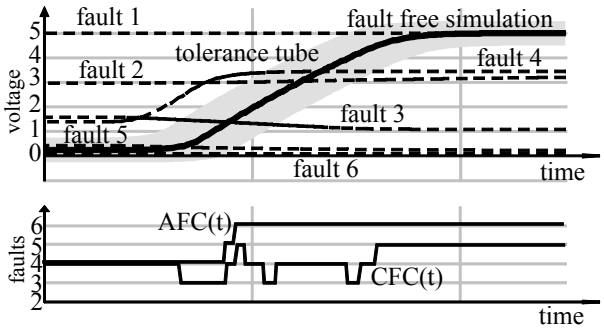

Fig. 1 Fault coverages and tolerance tube

The defect-oriented testability for transient analyses of an analogue circuit is usually specified by the fault coverage in its accumulated (AFC(t)) and concurrent (CFC(t)) form. These are defined by the number of detected faults *until* and *at* the current time step. For an example with six faults and a tolerance tube around the fault free test answer the FCs with the absolute number of detected faults can be seen in fig.1. Faults are detected when their related test answer runs out of the tube.

From the discussion of the FCs follows that the AFC describes the overall efficiency of the test and the necessary test length to detect a certain number of faults. The CFC results in the test points or periods with the respective highest temporary FC, thus, possibly controling the best test time for measurements. But as will be shown in the following these analyses are only one part and are not sufficient to guide an optimal selection and generation process for efficient structural tests, since the information about the necessary measurement precision to detect the detectable faults is missing. The need to complement the testability measure can be seen by thinking about two circuits or two stimuli for one circuit that have nearly the same CFCs. They can differ heavily in the distances of the detectable faults to the fault free simulation, and thus in their testability. The question where to test can not be answered effectively so far. The connection with the possible decrease of the necessary measurement accuracy is obvious.

$$NUFD(t) = min\{F_1(t), F_2(t), \ldots, F_n(t)\}, \quad \forall\ F_i(t) - G(t) > T_{upper}(t) \tag{1}$$

$$NLFD(t) = max\{F_1(t), F_2(t), \ldots, F_n(t)\}, \quad \forall\ G(t) - F_i(t) < T_{lower}(t) \tag{2}$$

$$MFD(t) = min\{NUFD(t) - G(t), G(t) - NLFD(t)\} \tag{3}$$

$$CFC_{norm}(t) = \frac{CFC(t)}{CFC_{max}},\ MFD_{norm}(t) = \frac{MFD(t)}{MFD_{max}}$$
$$DFC(t) = \frac{1}{2}(CFC_{norm}(t) + MFD_{norm}(t)) \tag{4}$$

To solve this, we propose to investigate the distances of the nearest fault detection Fi(t) to the fault free test response G(t) at every test time and combine these information with the traditional CFC(t), resulting in a ‚distance weighted fault coverage' DFC(t). The first step is the determination of the nearest upper and lower fault detections at each time step (NUFD(t), NLFD(t)). The lowest value of both is selected to build the ‚minimal fault detection' MFD(t) and the related weighted form $MFD_{norm}(t)$. In the last step the normalized $CFC_{norm}(t)$ is weighted with the $MFD_{nom}(t)$ to build the DFC(t). The calculation can be seen in the equations 1 to 4.

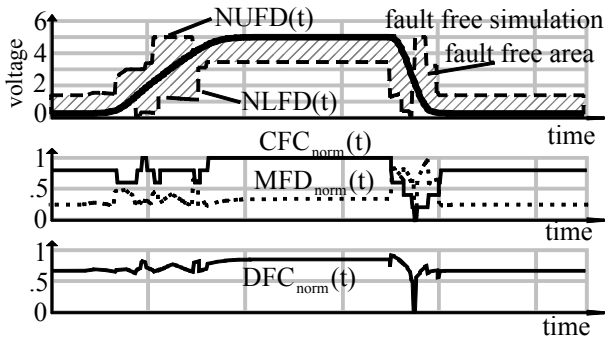

Fig. 2 Distance weighted fault coverage DFC(t)

For the given example the results are drawn in fig.2. We propose to use this DFC(t) as the concurrent testability measure for analogue circuits rather than the simple CFC(t). The advantages will be proved in the next chapters.

2.3. The window criterion

The application of the tolerance tube as the detection criterion is a direct transformation of the process and measurement tolerances to the test answer. For the application in a real test with the objective to *simply* find all faults it can be greatly simplified by choosing a small number of necessary test times. This process can be identified as a compression of the redundant information that is included in the tolerance tube. For a self-test this is mandatory.

The developed procedure to select the appropriate test times is based on the new test measures of the last chapter and on a fault dropping algorithm that has already been used in [98Hoff]. A maximum-search in the DFC(t) identifies a highly efficient test time with a high concurrent fault coverage *and* a large distance of the faulty to the fault free test answer. Since usually not all faults are detectable at one time the so far detected faults are dropped, the DFC(t) is recalculated with the remaining faults and the maximum search is repeated until no faults are left. This loop results in the necessary number of test times to detect all principally detectable faults.

Since the main contribution of this paper is the automatic generation of an applicable test, it becomes obvious that ‚real' measurement systems will seldom be capable of measuring precisely a value at a predetermined single test time. Therefor the concept has to be extended to a window criterion ([98Hoff]). By using the window criterion it will be observed whether the respective output signal lies during a certain time interval within a predetermined voltage or current range (fault free) or not (faulty). In fig.3 a possible detection window is drawn together with the fault free response, the related tolerance tube and one possible faulty

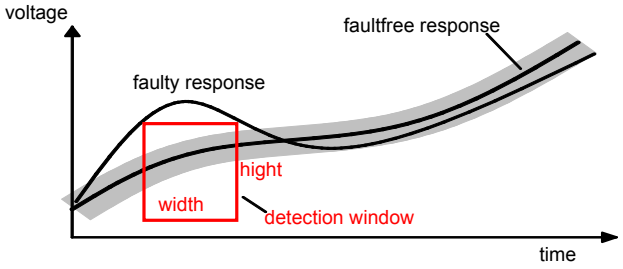

Fig. 3 Application of the window criterion

response. It can be seen that the application of the drawn detection window would lead to the detection of the fault causing the faulty response. Even a wider window would detect the fault as the response lies out of the window over a certain time.

By using a window criterion it is now possible to include the tolerances of a - so far virtual - measurement system in form of the time tolerance around the left and right window border and the level tolerance around the upper and lower window border respectively. This can be seen in fig. 4 for one window, where the measurement system would be programmed to the respective middle values (measurement window). Using this window the faults that lie during the inner window period out of the outer upper or lower border are detected (detection window). The related windows to detect all faults are found by following the procedure of DFT-maximum-search and fault dropping as above with one difference. The time points are understood as start values for the following widening of the windows such that the window is at least as wide as the time tolerance of the measurement system imposes.

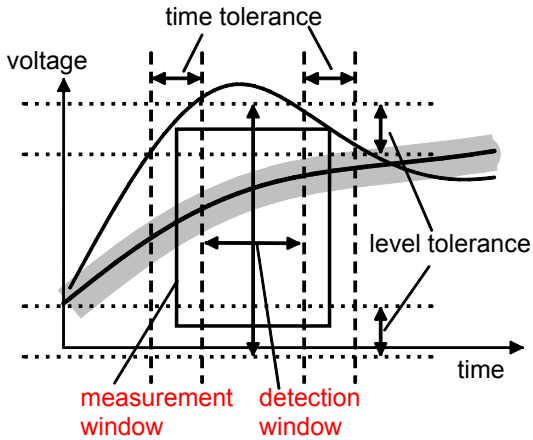

Fig. 4 Measurement tolerances

2.5. Hard-to-detect faults

The above procedure of window maximisation is working well besides the problem that certain faults may remain undetectable due to the new inserted measurement tolerances. Thus, the concept of the tolerance tube in the analogue fault simulation has to be refined by splitting the influence of measurement and technology tolerances into two different tubes around the fault free test answer: The inner technology tube and the outer measurement tube. This approach is extremely important for the consideration of measurement tolerances and can be identified as the major drawback of the traditional analogue test data evaluation approach, since so far it was not possible to distinguish between hard-to-detect and not-to-detect faults. This is all the more important because of the connection to the test costs: The harder to test the higher the necessary test costs. We propose to define them as follows according to their test answers: Not-to-detect faults lie within the inner tube (TG: dark grey), hard-to-detect faults lie within the outer tube (TF: light grey) but outside the inner tube. In fig. 5 both tubes are drawn around the fault free test answer together with one window criterion.

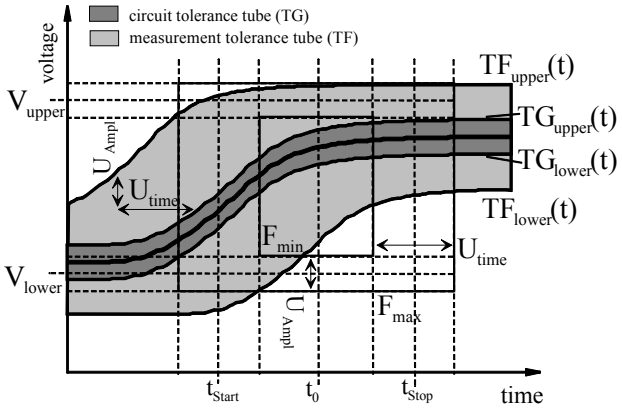

Fig. 5 Window criterion and tolerances

The measurement tube has been constructed according to the former explained measurement tolerances, being applied to the window criterion. When using these window measurements with time and amplitude tolerances the borders of the inner tube have to be shifted by U_{ampl} *and* U_{time}. By doing this it can be assured that all faulty test answers that lie out of the outer tube can be detected with the related measurement system! Besides the construction of the outer tube to clearly define the hard- and not-to-detect faults, the major advantage is the application to the design flow of the analogue fault simulation. It is now possible to determine the set of faulty test answers by the fault simulation and apply the technology tube. The not-to-detect faults (presuming well defined test stimuli) remain undetectable and are removed from the following analyses. From this step on it is possible to analyse the effect of high measurement tolerances (e.g. cheap test equipment) on the fault coverage *before* the concrete detection windows are calculated. Moreover, it is possible to precisely identify those faults

that remain undetected with certain measurement tolerances. A compromise between test cost and test quality is enabled to be done.

3. A local testability enhanced design

A defect robust design can greatly enhance the testability of analogue circuits, by preparing the layout in a way that certain faults that are caused by defects are highly unlikely. From yield investigations the knowledge about these connections between layout geometries and defect impacts is well established in the layout process. Nevertheless, a general maximal defect-robust design is economically not feasible. But, with the investigation from the last chapter regarding the hard-to-detect faults in conjunction with the possibly decrease of measurement precision it is possible to identify those faults that have to be defect-robust layouted. In fact, from the experience with the analogue fault simulations and the application of possibly low-cost test equipment follows, that there is always a number of not- and hard- (or better costly-) to-detect faults that limit the structural approaches greatly.

3.1. A new defect-oriented design flow

To overcome this problem we propose to use the L²RFM [96Ohle] approach to enable the layout-realistic fault listing in an early design phase before the layout is started. Thus, the CPU-time-intensive fault simulation can be done in parallel to the design process and results can already be used in the circuit design. Basically this approach uses well known defect related information about the future (!) layout of certain element sets (e.g. basic building blocks) to build a layout-realistic fault list by netlist analyses. The new developed program GenFAULT [99HoffSM] detects the element sets and links the layout information. The program together with the fault simulator aFSIM [00StraMV] have currently passed an industrial certification process and were integrated in the design flow.

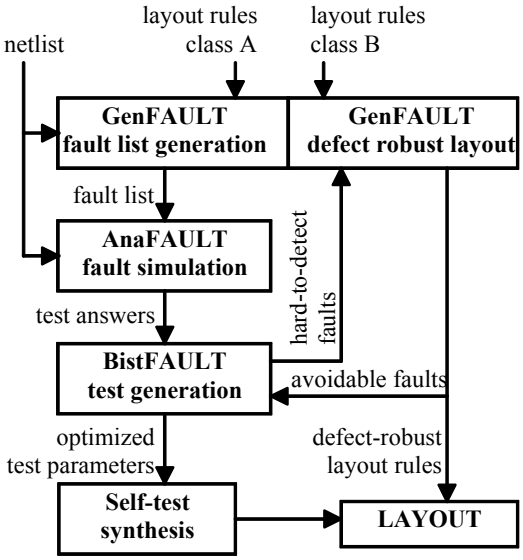

Fig. 6 New design flow

As explained, rule-like layout methods that can be certainly assumed (sometimes demanded similar to the known technology dependent layout rules) and which can be linked to topological detectable element sets are collected and applied to the fault listing process. The problem with this approach is that many possible defect-robust layout rules exist but only a few can be certainly assumed. To overcome this problem the concept and the program GenFAULT have been extended from the layout rules that must be used (class A) to the layout rules that could be used (class B). Again these rules are related to certain topological element sets or element properties that can be determined by netlist analyses. Together with the methods from chapter 2 that have been collected in the tool BistFAULT and the fault simulator AnaFAULT the new design flow from fig. 6 is proposed here for the first time.

The result is a system to automatically search for the existence of layout methods to avoid those faults that are hard- or not-to-detect and thus to enhance the testability of the circuit. But moreover, the main advantage is the possibility to decrease the accuracy of the measurement system, find those faults that are then hard-to-detect and automatically search for a possible layout measure to avoid these faults. Thus, the test costs can be decreased until no layout measures are found.

3.2. Controling a local design for robustness

To elaborate this concept the process of the automatic determination of layout measures will be explained in two examples that have been derived from an industrial CMOS circuit. A very typical problem is the detectability of gate open faults in the bias stage of differential amplifiers. In this case the fault simulations results in the two hard-to-detect faults in the load transistors M4 and M9 that can be seen in fig. 7.

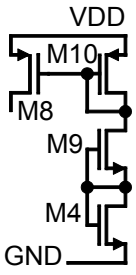

Fig. 7 Bias

The topological analysis of GenFAULT detects the current mirror as well as the load transistors. Since the gate open but not the drain open of the load transistors are hard-to-detect it is easily possible to derive the necessary layout topology: Routing from M9 to M10, first connect the drain then connect the gate and use enough contacts. In this way the single gate-open is highly unlikely. The remaining combined gate/drain-open is still likely but is known to be detectable. There is a large number of such layout measures that can be applied without any

problems to a limited number of transistors controlling the order of connecting elements and the number of contacts that have to be used.

For shorts it is much more difficult to avoid these faults by layout measures since a separate routing can decrease the probability of occurrence drastically but a short between the terminals of an element is always possible. Nevertheless, to guide the separate routing of specific signal lines is a very important layout measure. Also these information can be derived from the above system.

4. Case study: BIST generation

To show the applicability of the test generation algorithm, of the window criterion and the advantages of the proposed design flow, a voltage controlled oscillator (VCO) as a part of a mixed-signal system is investigated in a case study. It is envisaged to generate a self-test for this circuit in a mixed-signal environment. Similar to the approach in [91Ohle] mixed-signal systems are supposed to have at least one AD converter on-chip or, in this case, can be directly analysed in the digital domain. Thus, to keep the need for extra analogue test circuits as low as possible and to

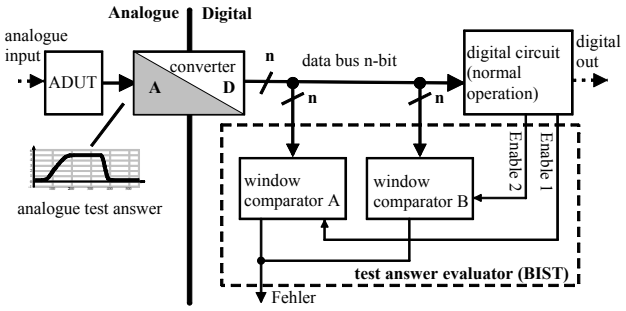

Fig. 8 Target system and BIST implementation

exploit the advantages of low area consumption, the test response evaluation is realized in the digital domain. The resulting structure is shown in fig.8 with the analogue device under test (ADUT), the ADC, the digital part of the design and the test answer evaluator of the BIST that consists of a set of comparators (detections windows). One major advantage of the proposed methodology is that the digital BIST hardware can be generated *automatically*. The calculated parameters of the windows can be directly trans lated into a gate description (VHDL) of the window comparator network and synthesized.

The VCO (ADUT) consists of 26 transistors and 104 fault simulations have been carried out with AnaFAULT performing a transient analysis. The input voltage V_{in} and the output voltage V_{out} can be seen in fig. 9. In this case study all hard faults using the local hard fault model have been considered. The used fault simulation model consisted

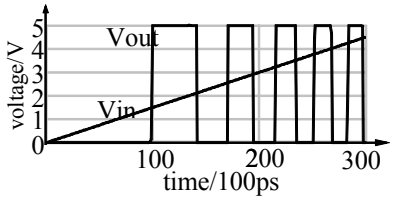

Fig. 9 Fault free operation of the VCO

of a resistor with 20 Ohm for shorts and 1 MOhm for opens. Before BistFAULT can be used, the standard testability analysis has to be applied by AnaFAULT by using a tolerance tube (here ±0.2V, ±0.8ns) around the gold simulation to model the tolerances of the circuit. By doing this 13 faults turned out to be not detectable (12 gate open, 1 drain/source short). The analysis with GenFAULT results in the automatic determination of 12 possible layout rules to avoid the single gate opens. The drain/source short remains possible but should be avoided by separate routing. The remaining 91 faulty responses are analysed by BistFAULT whether they are detectable by a window criterion BIST or not. In fig. 10 the fault free response with the used tolerance tube according to the measurement tolerances (0.1V, 1ns) and the NFDG are drawn. The analysis for hard-to-detect faults results in 2 gate open faults. Again these opens could be automatically translated into layout rules by GenFAULT. It has to be mentioned that, although not pictured here, the resulting MFD(t) is recalculated after every fault dropping. Applying the above described window determination algorithm the derived window positions and dimensions can be seen in fig. 10. 4 windows are enough to detect all faults using the measurement system with the

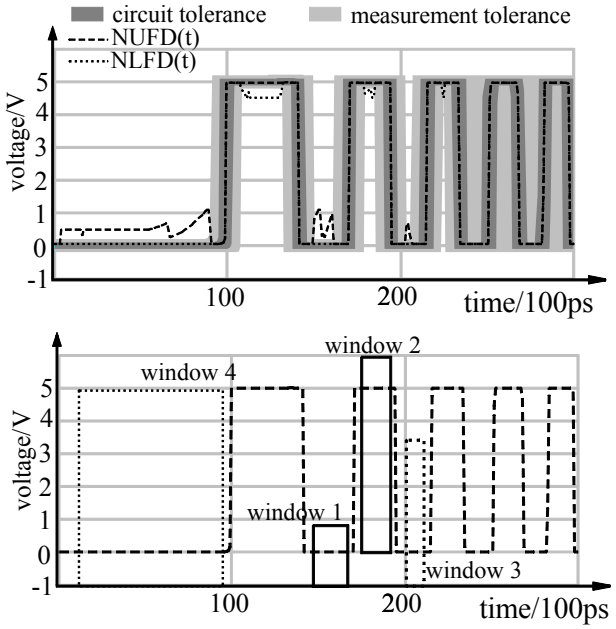

Fig. 10 Window calculation for the VCO

above tolerance.

The fault coverage of the above test is calculated under the assumption that the derived layout rules are used, and consequently 104-14=90 faults have to be detected. 1 remains undetectable although being very unlikely, thus the FC is 99%. Finally, the derived windows were automatically translated by BistFAULT to a VHDL representation and were transferred to the circuit synthesis (Synergy, Cadence). The circuit was mapped to a 0.8µ CMOS technology and could be synthesised resulting in a digital circuit of 32 gate equivalents. The total area including wiring for this BIST circuits amounts to 0,019 mm².

5. Conclusion

The defect-oriented (structural) test approach has been successfully used to enable the automatic and software based generation of a highly efficient test for analogue circuits. With this objective the existing methods of the analogue fault simulation were greatly enhanced and the distance weighted fault coverage DFC(t) has been introduced as a new testability measure to include the distances between the faulty and fault free test answers. Thus, it is possible to determine the most effective test times with respect to the number of fault detections *and* the necessary accuracy of the measurements. The approach finds the necessary number of test times to detect all theoretically detectable faults.

With the introduced new distinction between production and measurement tolerances it is possible to define not-to-detect and hard-to-detect faults. Since the latter mostly can be defined as costly-to-detect and now can be identified with the presented test systems, it is possible to clearly decide whether the respective fault should be detected by a more complex test or not. Moreover, a system was presented that allows to analyse the effects of the measurement tolerances on the fault coverage.

With the development of the new tool GenFAULT it is possible to automatically search for the existence of defect-robust layout measures to avoid certain faults by controlling the layout process. Since this is possible in an early design phase, the defect robust layout can be used as a variable to optimize the test system and the necessary measurement accuracy.

The developed procedures have been implemented in the analogue fault simulation tools GenFAULT, AnaFAULT and BistFAULT to enable the EDA-tool-based automatic generation of self-test structures that use a window criterion for fault detection. The applicability could be demonstrated in a case study, resulting in a self-test system with an extremely small area overhead and a very high fault coverage

Acknowledgement

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