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A New Family of Step-Up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies With Dual Input Voltage Sources

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ABSTRACT In the low voltage based renewable systems like PV and Fuel cell applications, the step-up of the output voltage to drive the loads is essential. For this, the integration of switched-capacitor (SC) units with the dc-ac converters will have the potential advantages like improved efficiency, optimal switching devices, small size of passive elements (L and C) as compared with traditional two-stage conversion system (dc/dc converter and dc/ac converter). This paper focuses on a new family of step-up multilevel inverter topologies with switched capacitor integration with dual input voltage sources. With the flexibility of 2 dc sources and switching capacitor circuits, four different topologies have been suggested in this paper with features of high voltage gain, reduced component count, reduced voltage stress and self-voltage balancing of the capacitor while achieving a higher number of levels. A detailed analysis of proposed multilevel inverters has been analyzed with the symmetrical and asymmetrical mode of operations and the associated gain, the number of levels, and other performance indices are presented. An in-depth study of all the topologies has been accomplished in this paper with several comparative studies in terms of components count, voltage gain and cost. The effectiveness and practicability of the suggested topology with 13 level output voltage has been explained by the experimental results obtained from a scale down prototype.

INDEX TERMS Hybrid reduced switch bidirectional cascaded H-bridge multilevel inverter, pulse width modulation (PWM), total harmonics distortion (THD).

I. INTRODUCTION

With the rising demand for renewable energy sources, the importance of multilevel inverters (MLI) has been at its peak for the dc-ac power conversion. The growing application of MLIs in the renewable energy system is due to the advantages of connecting several dc-link formed by dc voltage sources. The string of dc voltage sources can comprise multiple solar photovoltaic (PV) units, ultra-capacitors, or batteries to get different voltage levels. The MLI can integrate these dc power sources to achieve an efficient dc/ac power conversion for high voltage applications. Multilevel inverters also demonstrations the properties like improved output parameters (like reduced harmonic distortion, improved fundamental voltage), reduced the size of the required filter, reduced voltage rating of individual switches, and improved efficiency. The traditional MLI configurations have been categorized as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) with their different evolved structures. Conversely, with traditional topologies, the component count is high for a higher level count of output voltage, Further, they also suffer from capacitor voltage balancing issue [1]–[3]. The research related to MLIs has been done from the last four to five decades and still, there is a research scope on MLI topologies and their control with the advanced features like simple in realization, higher fault tolerance, hybrid single state for low voltage dc to high voltage dc and many more. The current research related to MLI has been the reduced component count topologies with modularity, reduced voltage stresses, higher efficiency, etc., [4]–[7].

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Based on the reduced switch count, numerous topologies have been proposed [3], [8]. The optimal design of several topologies has also been considered to reduce the number of switches and dc voltage source count [9]–[11]. However, the main issue with these topologies has been the requirement of a higher number of isolated dc voltage sources, which makes them not suitable for practical applications. Another drawback of these topologies has been the lacking of boosting the input voltage.

The integration of capacitors in the multilevel inverter topology is not a new concept as capacitors have been used in NPC and FC based MLIs. However, the capacitor used in these topologies does not provide any boosting feature. In recent years, the switched-capacitor based multilevel inverter (SCMLI) topologies based on series/parallel combination of capacitors have gained much popularity for high voltage applications [12]–[16]. This is due to the boosting feature possess by the SCMLI. The self-voltage balancing of the capacitors is the additional important feature of the SC-based topology which reduces the control complexity of the system. The step-up or boosting feature enables the low voltage sources such as PV systems to be used for the high voltage applications. These step-up converters eliminate the need for intermittent boost dc/dc converter topology, results in lower size and cost with improved efficiency of the overall system. However, the higher number of components and their extension for a higher number of levels have been the major challenges nowadays. A seven-level topology has been proposed in [17], which uses 16 switches with two capacitors. Similarly, nine-level topologies have been proposed in [18], [19], which uses 11 and 12 switches respectively. However, for a higher number of levels, the only option is the cascade connection of several modules which increases the components count.

Apart from a large number of components required for a higher number of levels, another problem associated with the SC-MLI topologies has been the lower power ranges due to the high current rating of some of the switches [20]. The problem of lower power rating can be solved by having multiple dc voltage sources with SC modules. The use of multiple dc voltage sources splits the amount of current among the available dc voltage sources and switches. Several topologies with multiple sources based on SC-MLI have been reported in the literature. A topology with a higher number of levels has been recommended in [20], however, due to the higher number of components, reliability has been one of the major issues. Another topology with 13 level output voltage has been proposed in [21], which uses 14 switches with two capacitors of different voltage ratings. Furthermore, in the topology of [21], the charging time for both capacitors is very less compared to their discharging time, which leads to a higher voltage ripple of the capacitor voltages. A nine-level dual input topology has been proposed in [2], however, it lacks the boosting feature along with higher total standing voltage (TSV) due to the use of backend H-bridge for the purpose of polarity change across the load. Similarly, some more topologies with multiple dc voltage sources have been proposed in [2], [21]–[31].

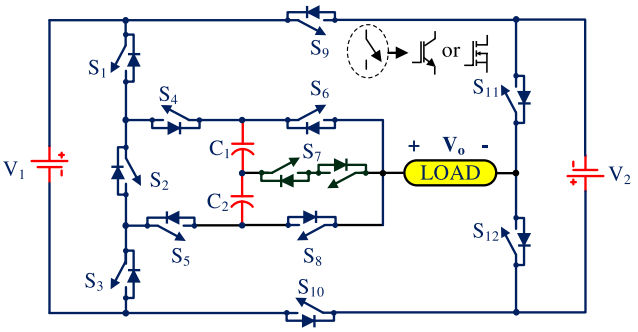

FIGURE 1. First proposed topology (PT-I).

In this paper, a new family of dual input SC- MLI has been proposed to achieve a higher number of voltage levels ensuring the lower number of components and TSV. The proposed topologies provide the boosting of the input voltage. The paper has been organized as follows: Section II gives a detailed explanation of the suggested topology in both symmetrical and asymmetrical configurations. In Section III, a comparison of different topologies has been provided and Section IV gives the experimental results. The conclusion of the paper is given in Section V.

II. PROPOSED DUAL SOURCE TOPOLOGIES

A. PROPOSED TOPOLOGY-I (PT-I)

The assembly of the 1st proposed topology is shown in Fig. 1. It consist of two dc voltage source V_1 and V_2 and 12 switches. The two capacitors C_1 and C_2 are integrated with the dc voltage source V_1 and give the boosting feature to the proposed topology. Both capacitors are charged by connecting them in parallel to the dc voltage source V_1. However, 19 different combinations are available from the topology shown in Fig. 1. The switching table for different switching states is given in Table 1 with the charging and discharging state of both capacitors. Based on Table 1, the different positive voltage states of the proposed topology I are illustrated in Fig. 2 (a)-(j).

Another important aspect of the proposed topology has been reduced voltage stress. The maximum peak voltage of different switches are given as

$$\left.\begin{aligned} &V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{S6} = V_{S8} = V_1 \\ &V_{S7} = 0.5V_1 \\ &V_{S9} = V_{S10} = V_1 + V_2 \\ &V_{S11} = V_{S12} = V_2 \end{aligned}\right\} \quad (1)$$

Therefore the TSV of the PT-I can be calculated as

$$TSV = \sum_{x=1}^{12} V_{sx} = 10V_1 + 4V_2 \quad (2)$$

As it is clear from Table 1, the PT-I can produce a maximum of 19 levels of the output voltage. The magnitude of both dc voltage sources V_1 and V_2 of the PT-I can be selected in two different modes of operation, i.e., symmetrical and asymmetrical.

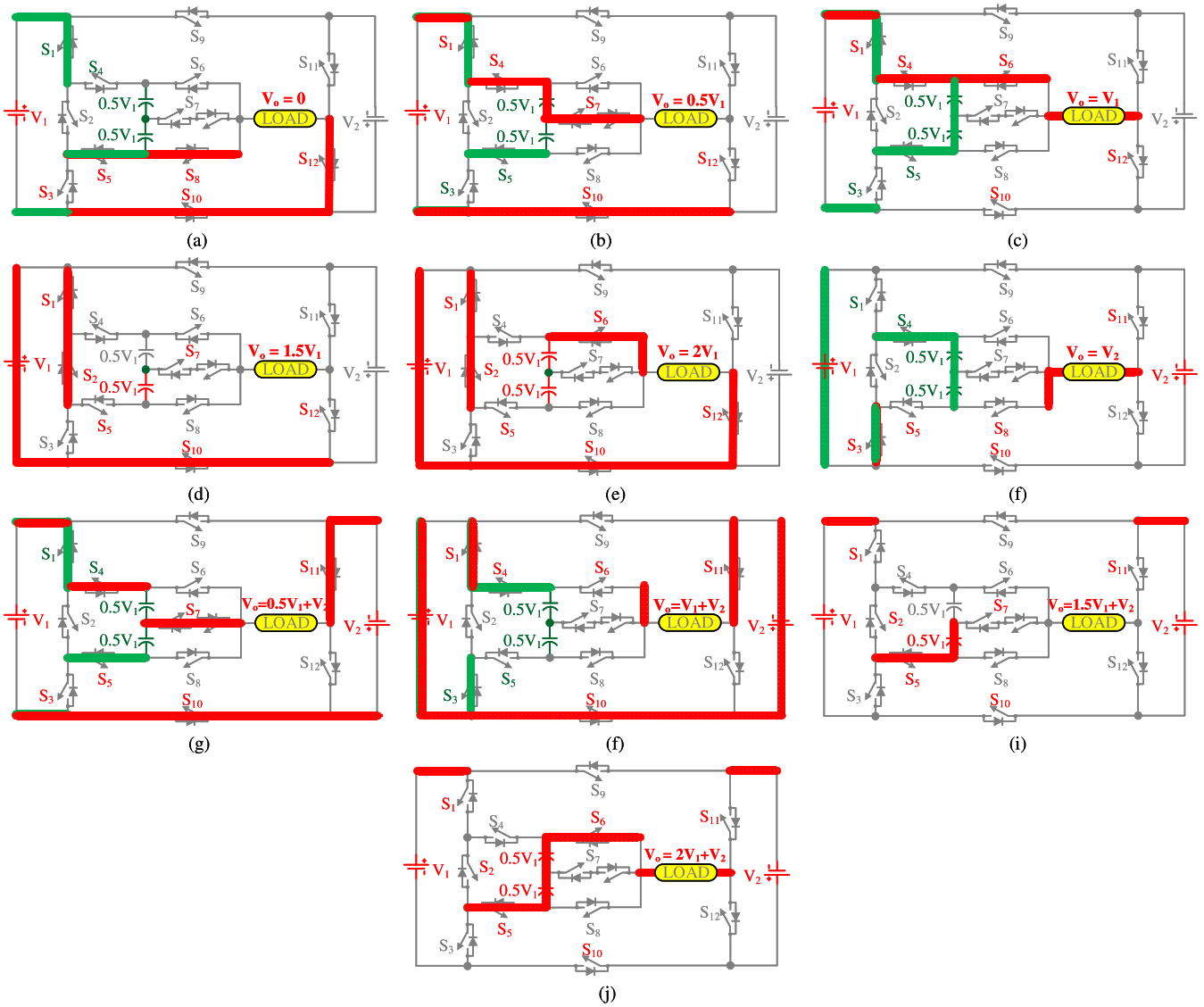

FIGURE 2. All possible voltage states of the proposed topology I with (a) $V_0 = 0$, (b) $V_0 = 0.5V_1$, (c) $V_0 = V_1$, (d) $V_0 = 1.5V_1$, (e) $V_0 = 2V_1$, (f) $V_0 = V_2$, (g) $V_0 = 0.5V_1 + V_2$, (h) $V_0 = V_1 + V_2$, (i) $V_0 = 1.5V_1 + V_2$, (j) $V_0 = 2V_1 + V_2$.

1) SYMMETRICAL MODE

In this mode, the magnitude of both dc voltage sources is selected as V_{dc}, i.e. $V_1 = V_2 = V_{dc}$. With this selection, the capacitor voltages are changed up to half of V_1, i.e., $0.5V_{dc}$. Therefore, in this mode, the total number of voltage levels which can be generated becomes 13 with peak output voltage, $V_{o,peak} = 3V_{dc}$. With $V_1 = V_2 = V_{dc}$, the TSV of the proposed topology I become $14V_{dc}$, the per-unit TSV (TSV_{pu}) can be calculated as

$$TSV_{pu} = \frac{TSV}{V_{o,peak}} = \frac{14V_{dc}}{3V_{dc}} = 4.67 \tag{3}$$

The voltage gain (VG) can be calculated as

$$VG = \frac{V_{o,peak}}{V_1 + V_2} = \frac{3V_{dc}}{2V_{dc}} = 1.5 \tag{4}$$

2) ASYMMETRICAL MODE

In this mode, the magnitude of both dc voltage sources has a different magnitude. For generating the maximum number of levels with a maximum voltage gain, the magnitude of V_1 is kept higher than the magnitude of V_2. With these criteria, the magnitude of both voltage sources i.e., V_1 and V_2 are selected as $4V_{dc}$ and V_{dc} respectively. With this magnitude selection, both capacitor voltages attend a maximum of $2V_{dc}$. The TSV and $V_{o,peak}$ becomes $44V_{dc}$ and $9V_{dc}$ respectively. the TSV_{pu} and VG are calculated from (3) and (4) as

$$\left.\begin{aligned} TSV_{pu} &= \tfrac{44V_{dc}}{9V_{dc}} = 4.89 \\ VG &= \tfrac{9V_{dc}}{5V_{dc}} = 1.8 \end{aligned}\right\} \tag{5}$$

Therefore, with asymmetrical mode, the number of levels is increased to 19 with a higher voltage gain of 1.8.

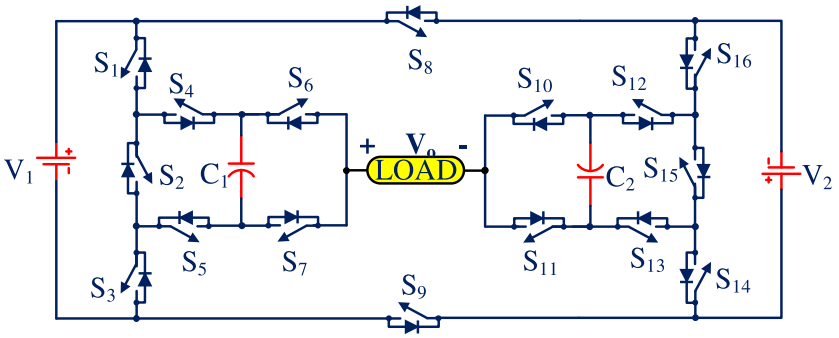

FIGURE 3. Circuit configuration of PT-II.

TABLE 1. Switching state of the proposed topology-I.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	V_0	V_{C1}	V_{C2}
1	0	1	1	1	0	0	1	0	1	0	1	0	C	C
1	0	1	1	1	0	1	0	0	1	0	1	$0.5V_1$	C	C
1	0	1	1	1	1	0	0	0	1	0	1	V_1	C	C
1	1	0	0	1	0	1	0	0	1	0	1	$1.5V_1$	-	D
1	1	0	0	1	1	0	0	0	1	0	1	$2V_1$	D	D
1	0	1	1	1	0	0	1	0	1	1	0	V_2	C	C
1	0	1	1	1	0	1	0	0	1	1	0	$0.5V_1+V_2$	C	C
1	0	1	1	1	1	0	0	0	1	1	0	V_1+V_2	C	C
1	1	0	0	1	0	1	0	0	1	1	0	$1.5V_1+V_2$	D	-
1	1	0	0	1	1	0	0	0	1	1	0	$2V_1+V_2$	D	D
1	0	1	1	1	1	0	0	1	0	1	0	0	C	C
1	0	1	1	1	0	1	0	1	0	1	0	$-0.5V_1$	C	C
1	0	1	1	1	0	0	1	1	0	1	0	$-V_1$	C	C
0	1	1	1	0	0	1	0	1	0	1	0	$-1.5V_1$	D	-
0	1	1	1	0	0	0	1	1	0	1	0	$-2V_1$	D	D
1	0	1	1	1	1	0	0	1	0	0	1	$-V_2$	C	C
1	0	1	1	1	0	1	0	1	0	0	1	$-(0.5V_1+V_2)$	C	C
1	0	1	1	1	0	0	1	1	0	0	1	$-(V_1+V_2)$	C	C
0	1	1	1	0	0	1	0	1	0	0	1	$-(1.5V_1+V_2)$	-	D
0	1	1	1	0	0	0	1	1	0	0	1	$-(2V_1+V_2)$	D	D

B. PROPOSED TOPOLOGY II (PT-II)

In PT-I, the switched capacitor units are connected to the dc voltage source V_1 which results in the lower voltage gain and is limited to 1.8. To increase the VG, PT-I is modified by integrating two switched capacitor unit with both dc voltage sources and is depicted in Fig. 3. By adding two SC units, the switching Table for PT-II is given in Table 2. Similar to PT-I, the expression for TSV and $V_{o,peak}$ comes out to be

$$\left.\begin{aligned} TSV &= 9V_1 + 9V_2 \\ V_{o,peak} &= 2\,(V_1 + V_2) \end{aligned}\right\} \tag{6}$$

Similar to PT-I, the PT-II can be operated in two modes as the symmetrical and asymmetrical modes. In symmetrical mode, $V_1 = V_2 = V_{dc}$. This results in the charging of both capacitors up to a voltage level of V_{dc}. A maximum of nine levels can be generated with the symmetrical mode of operation of PT-II. With a similar expression of PT-I, the different parameters for PT-II are given as

$$\left.\begin{aligned} TSV_{pu} &= \frac{18V_{dc}}{4V_{dc}} = 4.5 \\ VG &= \frac{4V_{dc}}{2V_{dc}} = 2 \end{aligned}\right\} \tag{7}$$

Furthermore, for the asymmetrical mode, considering a higher number of levels, the magnitude of V_1 and V_2 can be selected as $3V_{dc}$ and V_{dc} respectively. With this selection of magnitudes, 17 levels can be achieved across the load. The different parameters for the PT-II with the symmetrical mode of operation are given as

$$\left.\begin{aligned} TSV_{pu} &= \frac{36V_{dc}}{8V_{dc}} = 4.5 \\ VG &= \frac{8V_{dc}}{4V_{dc}} = 2 \end{aligned}\right\} \tag{8}$$

Based on PT-I and PT-II, two more hybrid topologies have been proposed in this paper which is depicted in Fig. 4 and termed as proposed topology-III (PT-III) and proposed topology-IV (PT-IV). Table 3 gives the summarized overview of all the proposed topology by considering both modes of operation.

III. COMPARATIVE ANALYSIS

In Table 4, a comparison of the proposed converter with recently existing converters is presented. The comparison has been done based on the number of components, voltage stress, voltage gain, and cost function. Based on this table, it can be noted that with asymmetrical configuration, the boosting factor of the proposed topology is higher than the topologies presented in [2] and [26]. It can be noted that the topologies presented in [2], and [26] generated 11 and 13 levels of output voltage using two dc voltage source with asymmetrical configuration, whereas for the proposed topology, 19 levels can be achieved. Further, the topology of [26] higher per unit TSV as compared to the proposed structure.

In addition to the component comparison, a cost function (CF) has been defined which has been used to evaluate different topologies of Table 4. The cost function and normalized CF (NCF) has been defined as [32]

$$\begin{aligned} CF &= \left(N_{sw} + N_{gd} + N_d + N_C + \alpha \times TSV_{pu}\right) \times N_{dc} \\ NCF &= \frac{CF}{N_L} \end{aligned} \tag{9}$$

TABLE 2. Switching state of the proposed topology II.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	V_o	V_{C1}	V_{C2}
1	0	1	1	1	0	1	0	1	0	1	1	1	1	0	1	0	C	C
1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	1	V_1	C	C
1	1	0	0	1	1	0	0	1	0	1	1	1	1	0	1	$2V_1$	D	C
1	0	1	1	1	0	1	0	1	1	0	1	1	1	0	1	V_2	C	C
1	0	1	1	1	0	1	0	1	1	0	0	1	0	1	1	$2V_2$	C	D
1	0	1	1	1	1	0	0	1	1	0	1	1	1	0	1	V_1+V_2	C	C
1	1	0	0	1	1	0	0	1	1	0	1	1	1	0	1	$2V_1+V_2$	D	C
1	0	1	1	1	1	0	0	1	1	0	0	1	0	1	1	V_1+2V_2	C	D
1	1	0	0	1	1	0	0	1	1	0	0	1	0	1	1	$2V_1+2V_2$	D	D
1	0	1	1	1	1	0	1	0	1	0	1	1	1	0	1	0	C	C
1	0	1	1	1	0	1	1	0	1	0	1	1	1	0	1	$-V_1$	C	C
0	1	1	1	0	0	1	1	0	1	0	1	1	1	0	1	$-2V_1$	D	C
1	0	1	1	1	1	0	1	0	0	1	1	1	1	0	1	$-V_2$	C	C
1	0	1	1	1	1	0	1	0	0	1	1	0	1	1	0	$-2V_2$	C	D
1	0	1	1	1	0	1	1	0	0	1	1	1	1	0	1	$-(V_1+V_2)$	C	C
0	1	1	1	0	0	1	1	0	0	1	1	1	1	0	1	$-(2V_1+V_2)$	D	C
1	0	1	1	1	0	1	1	0	0	1	1	0	1	1	0	$-(V_1+2V_2)$	C	D
0	1	1	1	0	0	1	1	0	0	1	1	0	1	1	0	$-(2V_1+2V_2)$	D	D

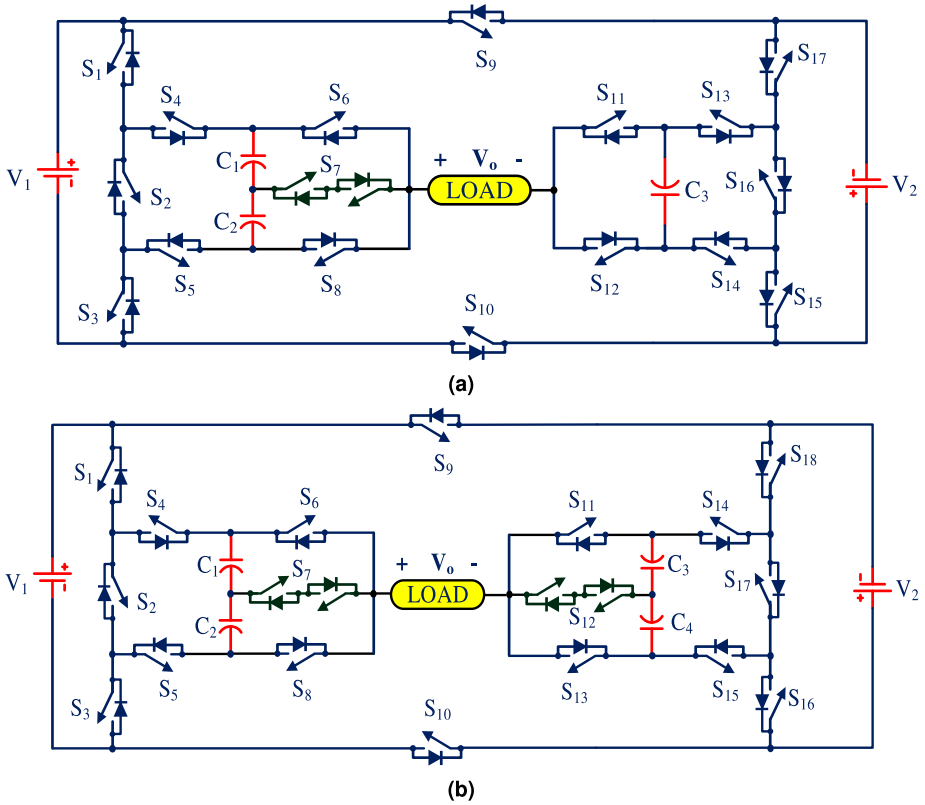

FIGURE 4. Schematic diagram of (a) PT-III and (b) PT-IV.

where α is constant which is associated with the voltage stress of the topologies. From Table 4, it can be observed that the proposed structure with asymmetrical configurations provides the lowest NCF for all values of α. This signifies that the suggested arrangement is more cost-effective as compared to other suggested topologies. The proposed converter

TABLE 3. Different parameters of the proposed topologies.

PT	N_{sw}	N_{gd}	N_C	Mode of operation	Magnitude of		N_L	TSV_{pu}	VG
					V_1	V_2			
I	13	12	2	Symmetrical	V_{DC}	V_{DC}	13	4.67	1.5
				Asymmetrical	$4V_{DC}$	V_{DC}	19	4.89	1.8
II	16	16	2	Symmetrical	V_{DC}	V_{DC}	9	4.5	2
				Asymmetrical	$3V_{DC}$	V_{DC}	17	4.5	2
III	18	17	3	Symmetrical	V_{DC}	V_{DC}	17	4.75	2
				Asymmetrical	V_{DC}	$2.5V_{DC}$	29	4.64	2
IV	20	18	4	Symmetrical	V_{DC}	V_{DC}	17	5	2
				Asymmetrical	$5V_{DC}$	V_{DC}	49	5	2

$N_{sw}/N_{gd}/N_c/N_L$= Number of switches / gate driver circuits/ capacitors / levels

TABLE 4. Comparison of PT-I with the other SCMLI topologies.

Topology	N_L	N_{dc}	N_{sw}	N_{gd}	N_d	N_C	TSV_{pu}	VG	α=0.5		α=1.0		α=1.5	
									CF	NCF	CF	NCF	CF	NCF
[2]	11	2	11	11	0	1	4.4	1.67	50.4	4.58	54.8	4.98	59.2	5.38
[21]	13	2	14	11	0	2	5.33	2	59.3	4.56	64.66	4.97	69.99	5.38
[23]	17	2	10	10	2	2	5.5	2	53.5	3.15	59	3.47	64.5	3.79
[25]	17	2	10	10	2	2	5.5	2	53.5	3.15	59	3.47	64.5	3.79
[26]	13	2	11	10	1	1	6.3	1.5	52.3	4.75	58.6	5.33	64.9	5.9
[29]	13	2	18	15	0	2	5	2	75	5.77	80.0	6.15	85	6.54
[30]	17	2	18	14	2	4	6	2	82	4.82	88.0	5.17	94	5.53
[31]	19	2	12	12	6	4	5.8	2.25	73.8	3.88	79.6	4.19	85.4	4.50
[PT-I] Symmetrical	13	2	13	12	0	2	4.67	1.5	58.67	4.51	63.34	4.87	68.01	5.23
[PT-I] Asymmetrical	19						4.89	1.8	58.89	3.10	63.78	3.36	68.67	3.61

provides a viable solution to achieve a high number of levels compared to other existing topologies with low voltage stress across the switches.

IV. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

The symmetrical operation of the proposed topology, i.e., with $V_1 = V_2 = 60V$ has been simulated using MATLAB software. A sinusoidal level-shifted carrier-based PWM with 12 carriers of 5kHz and one sinusoidal reference is implemented to attain the 13-level output voltage. The modulation index is the ratio of reference magnitude (V_{ref}) to carrier reference ($V_{carrier}$) and the output voltage of a proposed MLI is, $V_0 = MI \times (2V_1 + V_2)$. The peak magnitude of the output voltage with MI = 1.0 is 180V with the symmetrical configuration of the source. Fig. 5 (a) depicts the output waveforms of the load voltage, current and both capacitor voltage with a change of load parameter. At the time, t = 0.1s, the load is changed from 90Ω to 80mH + 90Ω, the nature of load current changes, however, both capacitor voltage remains balanced. Similarly, Fig. 5 (b) illustrates the different waveforms with the change of MI from 0.80 to 0.90 to 1.0. With lower MI, the magnitude of the output voltage reduces. However, the capacitor voltages remain balanced with the change of MI. Furthermore, Fig. 6 (a) and (b) illustrate the voltage and current stress of all 12 switches with a load parameter of 80mH + 90Ω. Out of 13 switches, S_1-S_6, S_8, S_{11}, and S_{12} need to be of a voltage rating of 100V, switches S_9 and S_{10} need to of voltage rating of 200V and the remaining two switches of the bidirectional switch S_7 need to block the voltage of 30V. In the charging loop of both capacitors, four switches are present, i.e., S_1, S_3, S_4 and S_5 need to of the current rating which is equal to the sum of changing and load current. The remaining switches of the topology have a current rating equal to the load current.

B. EXPERIMENTAL RESULTS

The experimental prototype of the proposed switched-capacitor multilevel inverter as shown in Fig. 7, has built-in the laboratory with the following: G60N100 IGBT switches, TDK Lambda GEN300-11 DC regulated power supplies, RL load Banks, PG6DI (450V and 2200μF) capacitors, FPGA Vertix-5 (XC5VLX50T) controller and GDA-2A4S1 Gate Drivers. The proposed MLI configuration is tested at 50Hz/5kHz modulating/switching fre-

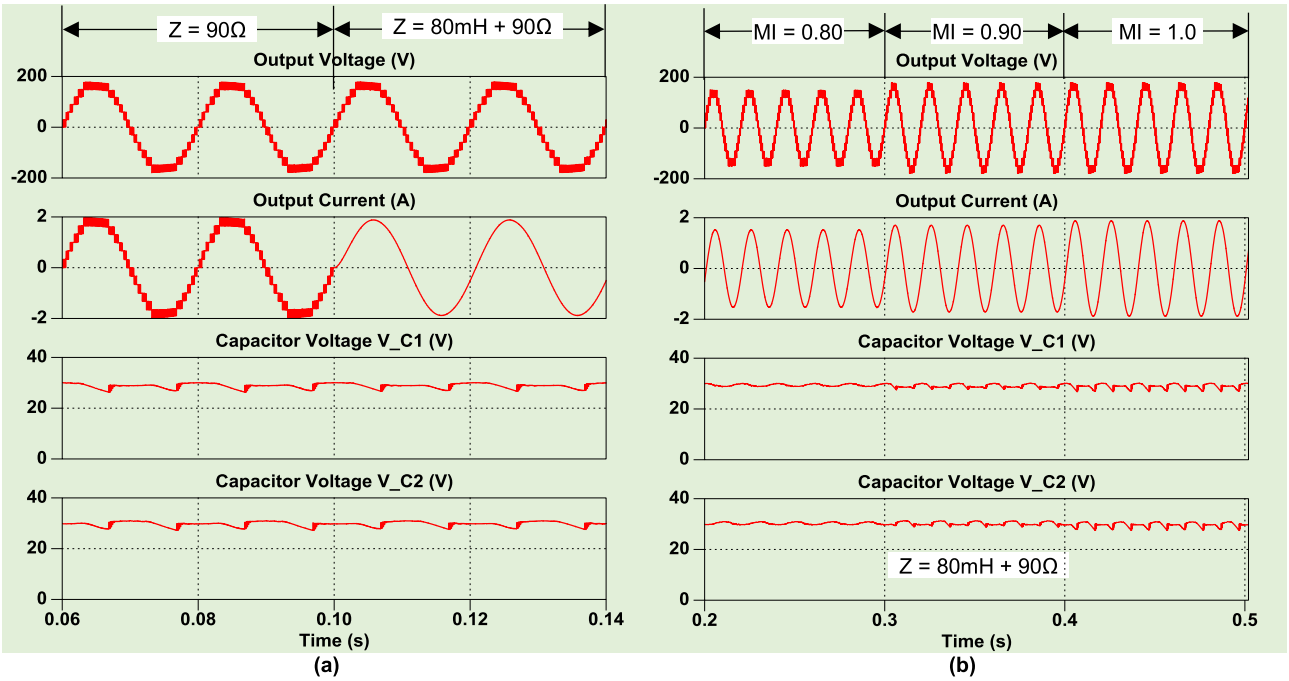

FIGURE 5. Simulation results with change of (a) load and (b) MI.

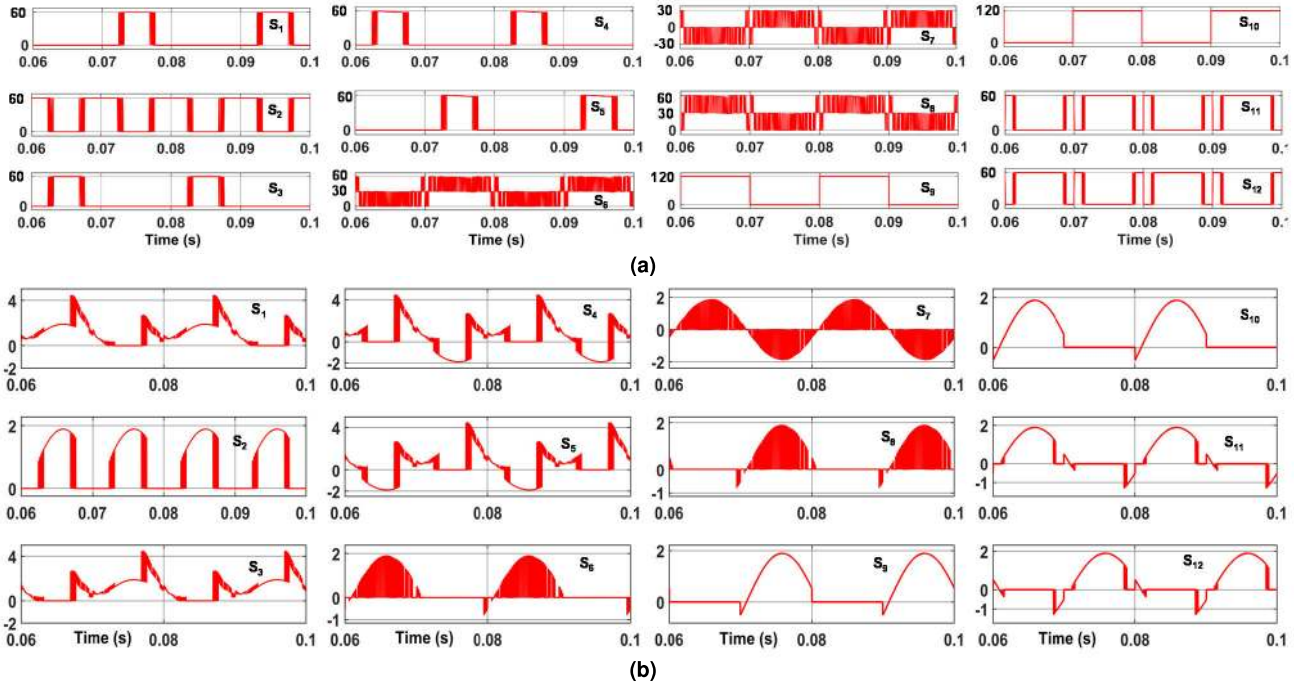

FIGURE 6. Simulation results of (a) voltage stress and (b) current stress of switches with symmetrical configuration.

quency, two 60V power supplies, two 90Ω load resistors and two 80mH load inductors. From the switching logic given in Table. 1, the complementary switch pair gate pulses are controlled with a 2μs delay to avoids the short circuit of source/load/capacitors. The control logic for symmetrical DC source driven proposed MLI is implemented in FPGA Vertix-5 board, where the programming has done in VHDL language. The proposed multilevel inverter is tested at various operating conditions, i.e., R load, RL load, a Step change in R/RL loads, Change of load type i.e., R to RL type, Change

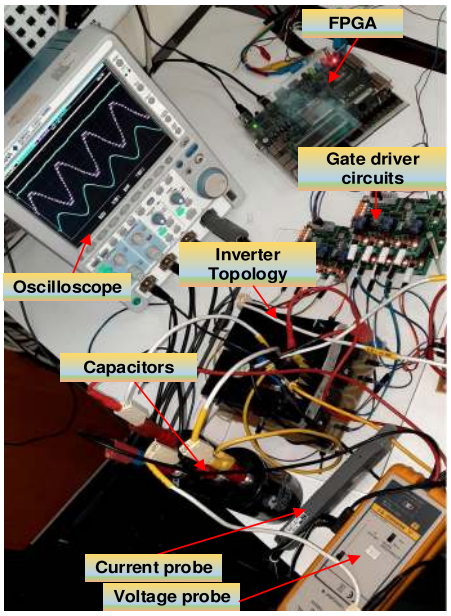

FIGURE 7. Experimental Setup.

of modulation index (MI) values, and Change of frequency of output voltage. These test results are evident for an effective operation of the proposed symmetrical source driven 13-level step-up boost inverter.

Fig. 8 shows the waveforms of 13 level output voltage, and voltage stress of switches (S_1, S_5) and (S_3, S_4). With the magnitude of $V_1 = V_2 = 60$V, the peak of the output voltage is 180V. The voltage stress of switches (S_1, S_5) and (S_3, S_4) have a peak magnitude of 60V, which is equal to the dc source magnitude. Similarly, Fig. 9 (a) illustrates the voltage stress of switches S_9, S_{10}, and S_{12}. The switches S_9 and S_{10} have maximum voltage stress which is equal to the sum of the input voltage, i.e., 120V. The maximum voltage stress for switches S_{12} is 60V.

The proposed MLI with Resistive (R) load (90 Ω) is tested in a laboratory for a MI = 1.0, and the associated test results are given in Fig. 9 (b). In this waveform, capacitor voltages, output voltage, and output current have been shown. Here the capacitors are charged symmetrically with half the voltage of DC-link voltage, i.e., $V_{C1} = V_{C2} = 30$V. Since the load is a Resistive type, the output voltage and current are in phase and having the same wave shape (13 level voltage). The peak output voltage and current of symmetrical DC source driven proposed MLI are 180V and 2A respectively. From these voltage/current waveforms, it is observed that the levels symmetrical and each voltage level is a step of 30V. The experimental analysis of proposed MLI is also carried out for Resistive-Inductive (RL) load at MI = 1, the results are shown in Fig. 9 (c). In this figure, it is observed that the current is sinusoidal and it is lagging behind the phase voltage since the load is inductive in nature. The peak voltage and current magnitudes are 180V/2A and the capacitor voltages are balanced (30V). Fig. 9 (d) demonstrates the harmonic spectrum of the 13 level output voltage waveform. The THD content of the output voltage is 8.9%. The lower order harmonics are almost zero due to the switching frequency of 5kHz which reduces the filter requirement.

The proposed MLI is tested under step change in Resistive load and the respective results are presented in Fig. 10. To show the effectiveness of a proposed MLI, a step-change in RL load is done and the associated results are presented in Fig. 10. In this figure, the enlarged version of experimental results for a step change of RL load, i.e., no-load to 180Ω-180mH and 180Ω-180mH to 90Ω-90mH are presented. The step-change in R load has been demonstrated

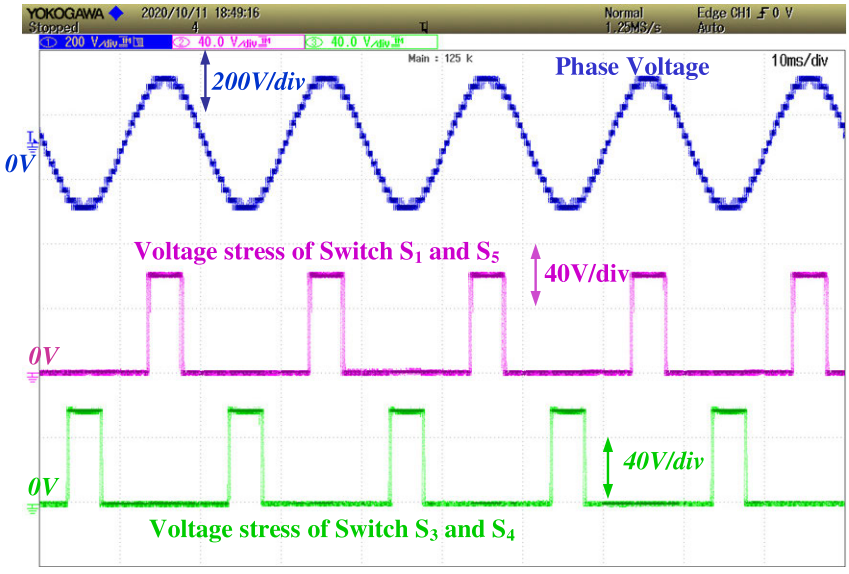

FIGURE 8. Experimental result of output voltage and voltage stress of switches (S_1, S_5) and (S_3, S_4).

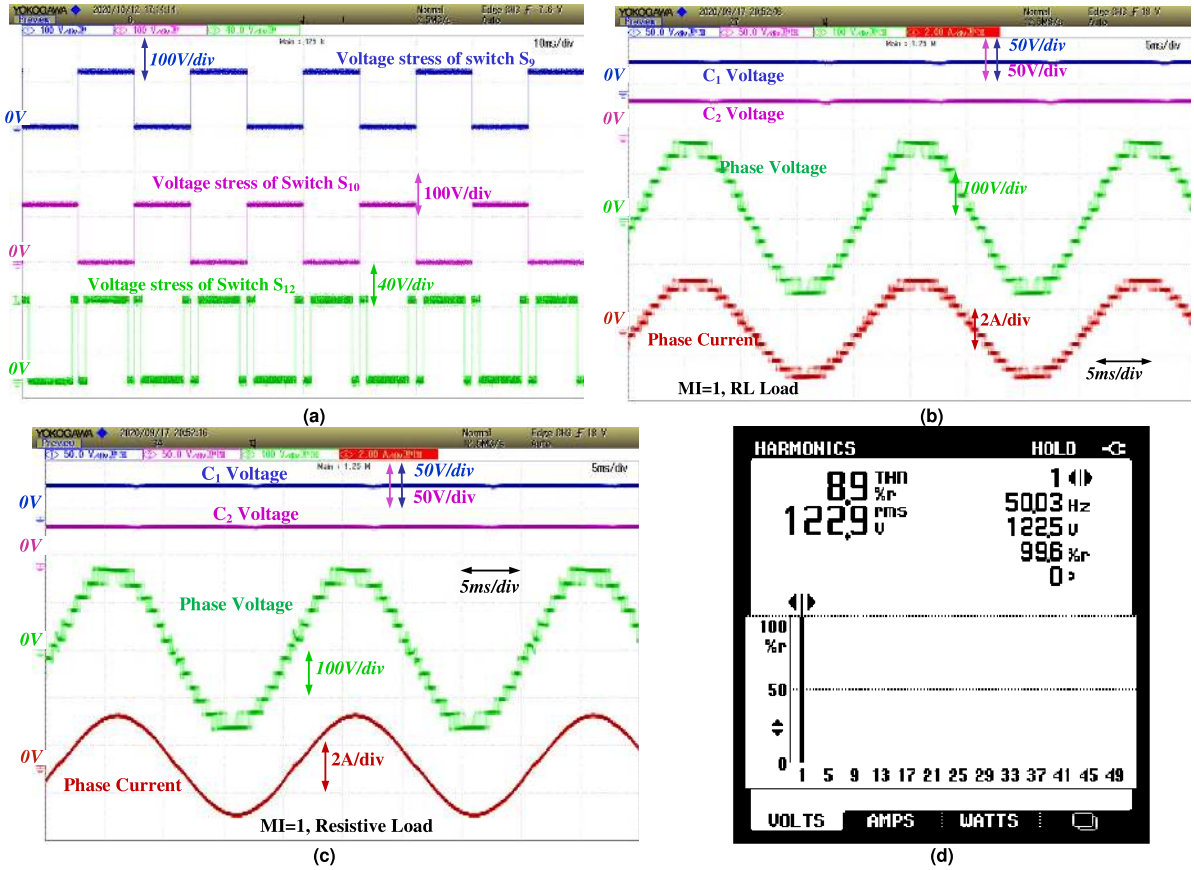

FIGURE 9. Experimental results with (a) voltage stress of switches, S_9, S_{10}, S_{12}, (b) R-load, (c) RL load, and (d) harmonic spectrum of output voltage.

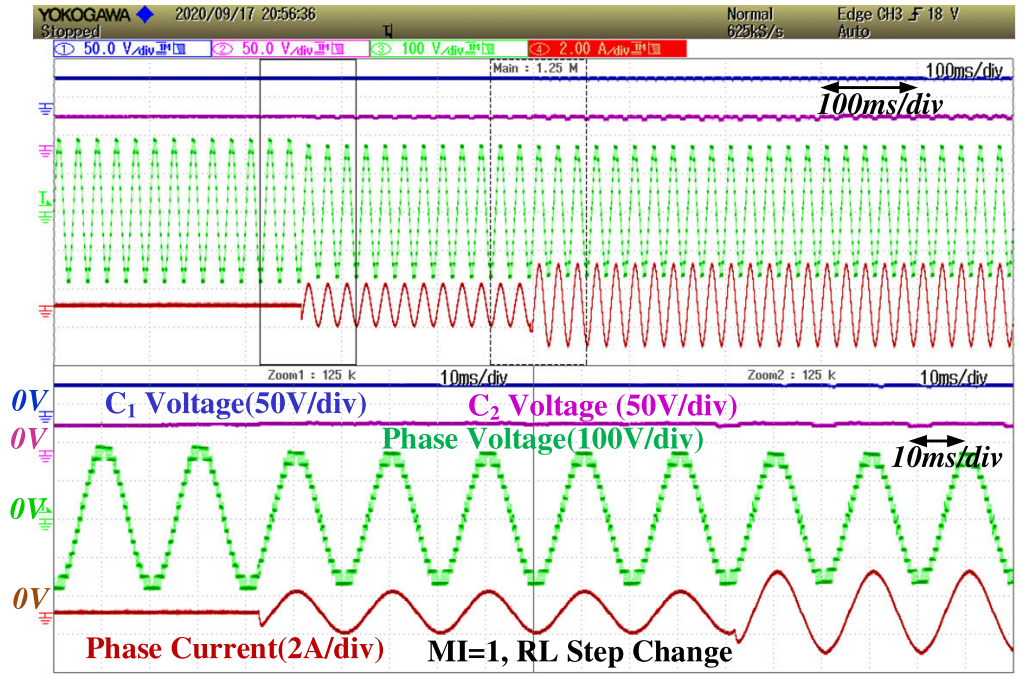

FIGURE 10. Experimental results with change in Rl load.

in Fig. 11 (a). In the bottom side of this figure, a zoomed version of experimental results for the step change of R load from no-load to 180 Ω (series of two 90 Ω resistors) and 180 Ω to 90 Ω are shown, i.e., left and right respectively. The peak current magnitude is 0, 1A, and 2A for no-load, 180 Ω and 90 Ω respectively.

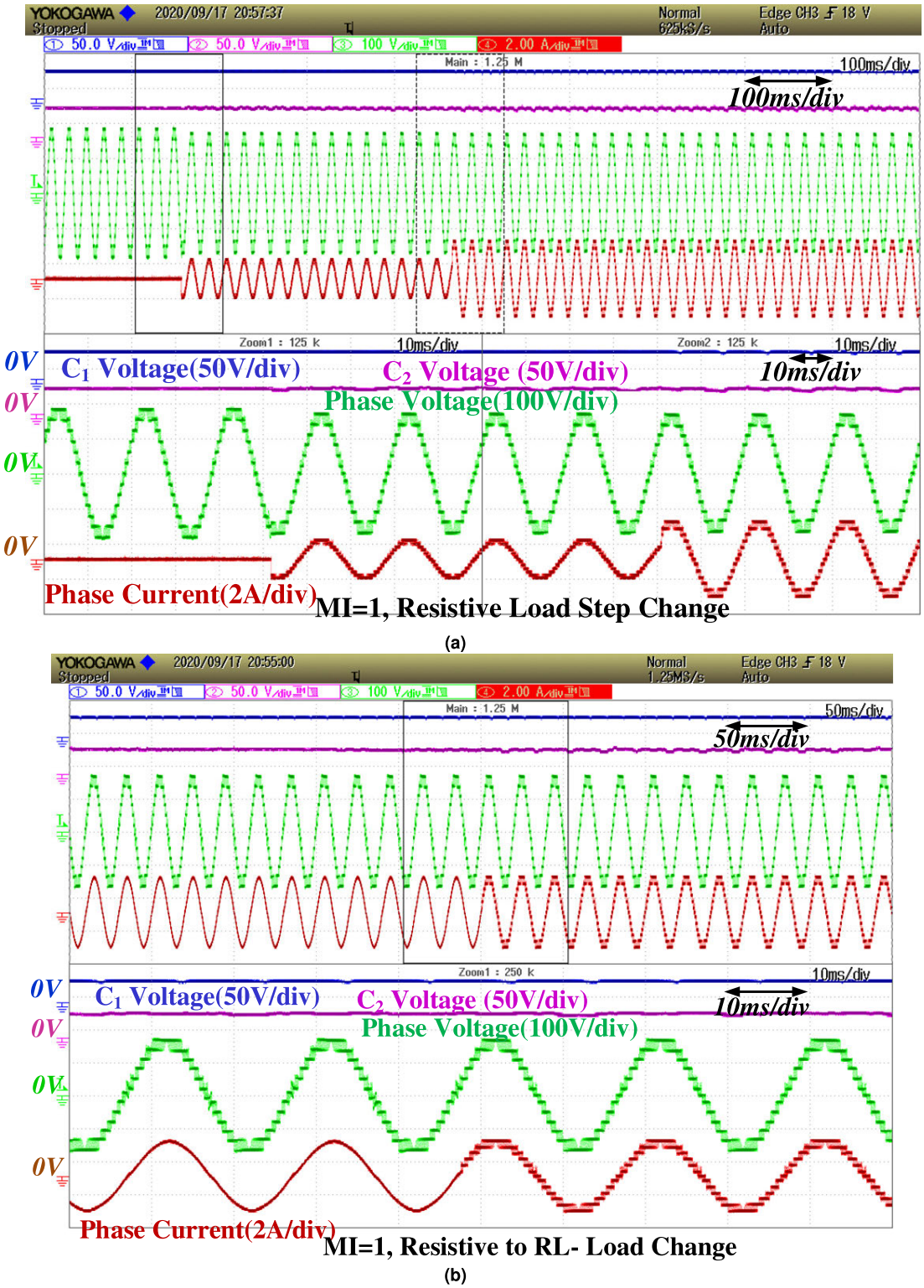

FIGURE 11. Experimental results with change in (a) R load and (b) load pf.

The proposed MLI is tested for a step-change in load type from RL to R, the results are shown in Fig. 11 (b). In this figure, it is clear that the change in the type of load RL to R results in a change in power factor, i.e., $\cos(X_L/R)$ for RL load and 1.0 for R load.

The experimental results of symmetrical source driven proposed MLI with the change in modulation index have shown in Fig. 12 (a). In this figure, the step change in MI is applied from 1 to 0.75, 0.75 to 0.5, 0.5 to 0.25. This results in the reduction of output voltage as well as current magnitudes

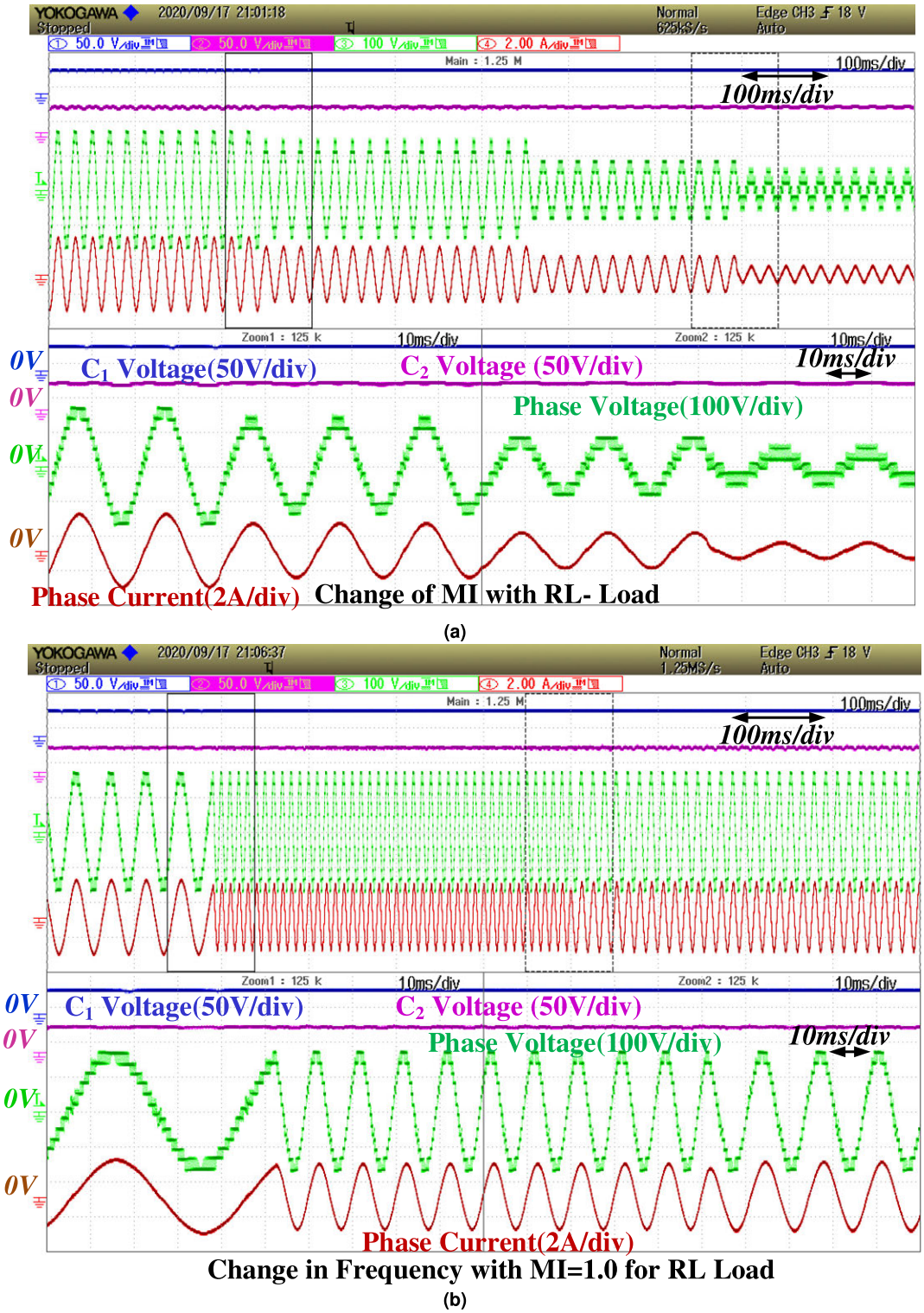

FIGURE 12. Experimental result with change in (a) output voltage frequency and (b) MI.

in proportional to the MI, which is clearly observed from Fig. 12 (a). The number of levels in the output voltage is also coming down gradually in accordance with the reduction in MI. On the bottom side of this figure, a zoomed version of step-change in 1 to 0.75 and 0.75 to 0.5 are shown. The proposed MLI is also tested for a step-change in frequency operation at MI = 1, i.e., 25Hz, 100Hz, and 75Hz, the results are shown in Fig. 12 (b). The 50 Hz operation of

the proposed MLI results is already shown in Fig. 8 to Fig. 12. All these experimental results are evidence that the capacitors are inherently balanced for step-change in load type, load magnitude, MI, and frequency.

V. CONCLUSION

In this paper, a new family of dual input-driven multilevel inverters with the integration of switched-capacitor units for attaining the boost capability as well as multilevel voltage has been discussed. For this, various multilevel inverters have been analyzed with the symmetrical/asymmetrical dc sources as well as different switched capacitor arrangements, and the detailed pros and cons of all configurations are presented. The higher voltage level generation, step-up operation, and lower voltage stress of the switches have been the main features of the proposed topologies. The comparative analysis is provided to highlight the benefits of the proposed topologies over the various multilevel inverters present in the literature. To show the effectiveness of the proposed topologies, a laboratory prototype of PT-I with the symmetrical sources is designed in the laboratory which will produce 13 levels and associated experimental results are provided. Different real-time operating conditions (like a step change in load, power factor, MI, and frequency) have been tested with the proposed topology and the experimental results show good agreement with the simulation results.

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