IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 3, 2021, accepted April 28, 2021, date of publication May 3, 2021, date of current version May 13, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3077055

A New High Gain Active Switched Network-Based Boost Converter for DC Microgrid Application

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This publication was made possible by Qatar University Collaborative research project grant # [QUCG-CENG-19/20-5] from the Qatar University. The statements made herein are solely the responsibility of the authors. Open Access funding provided by the Qatar National Library.

ABSTRACT This paper deals with an active switched inductor network-based high gain boost converter. By using less number of components in circuit topology, a higher gain in voltage can be attained at a small duty cycle value by using the proposed converter, which helps in reducing the switch voltage stress and conduction loss. In addition, it draws continuous input current, has lower diode voltage stress, and lower passive component voltage ratings. The operating principles and key waveforms in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) are presented. Parameter design, power loss calculation, characteristics, and comparative study with other non-isolated converters have been presented. Finally, a 200W hardware prototype is constructed and the viability of the proposed converter is verified through the experimentally obtained results.

INDEX TERMS Boost converter, active switched inductor, DC microgrid, high gain converter.

I. INTRODUCTION

A great deal of research has been carried throughout the world to explore renewable energy sources to cope up with the ever-increasing depletion of natural resources and their harmful effects on the environment as well. Although, Photovoltaic (PV) and wind generation, etc. being the renewable energy sources provide valuable environmental and economic features, there are some drawbacks associated with the utilization of these sources such as low output voltage. Distributed generation systems are local small scale power generation systems utilizing renewable energy resources to fulfill the increasing demand for electricity and environmental affairs. Fuel cells, solar PV, etc. are some of the renewable energy sources which are integrated with the DC microgrid in such systems as shown in Fig. 1. A DC microgrid is the most viable solution for the integration of PV generation systems with the AC power grid and DC loads. Solar PV is one of the most important sources of energy for the DC distributed generation system [1], [2]. The operation of the microgrid is possible in both grid-connected mode and islanding mode, where the most important matters are the system consistency and sustainability [3]. High voltage gain DC-DC converters are essential to step up and alleviate the low and variable DC voltages (12V–128V) obtained from the solar PV in DC microgrid system having the bus bar voltage up to 400 V DC [4]–[7]. High voltage gain DC-DC converters mainly

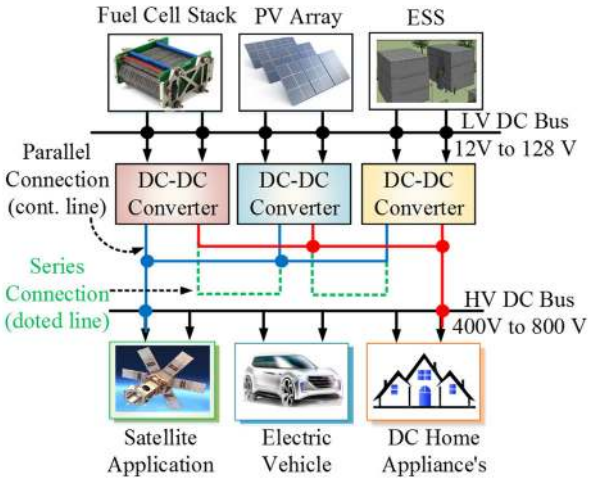

FIGURE 1. Structure of DC microgrid.

The associate editor coordinating the review of this manuscript and approving it for publication was Sonia F. Pinto.

provide a large conversion ratio, and high efficiency, and they are small in size [8].

Various topologies proposed for high step-up DC-DC converter in the literature mainly aim to achieve a high voltage gain for a reasonable duty ratio value with high converter efficiency value and low voltage stress value across the components [9]. The isolated and non-isolated converters are the two types of DC-DC boost converter which have their advantages and disadvantages depending on their application and requirements [3]. A high gain in voltage can be achieved by using the traditional boost DC-DC converter. However, the voltage stress across the switch is equal to the output voltage and the gain in voltage is limited by the voltage/current stress across/through the switch at large duty cycle values. Therefore, the selection of a high rating switch to meet the switch voltage stress requirement leads to high conduction loss [10]. To achieve high voltage gain, isolated converter structures such as half/full-bridge, flyback, push/pull, and forward converters have been suggested through the literature by adjusting the transformer or coupled inductor turn ratio [11]–[14]. However, there are some setbacks of these converter structures such as bulky circuitry, high switch voltage spikes, dissipation of power, transformer core saturation, and the converter active switch suffers high voltage stress because of the transformer leakage inductance. Furthermore, the requirement of a high frequency transformer, a non-dissipative snubber circuit, and an additional active clamping circuit leads to an increase in cost and size of these converters [15], [16].

The applications where galvanic insulation is not required, DC-DC converters of the non-isolated type are incorporated to attain a high voltage gain thereby reducing the overall size, weight, and volume since a high frequency transformer is not present and hence leading to an improved efficiency. The different non-isolated converter topologies discussed in the existing literature so far can be categorized as either with or without broad conversion range converters [17]. Cascade boost, quadratic boost, traditional boost converter combined with switched-capacitor technique, voltage lift, and capacitor–diode voltage multiplier are a few most commonly used non-isolated high gain converters [1], [2], [10]. However, the switched-inductor/capacitor stages incorporated in these converter configurations increase the voltage stress across the switches, the components count, cost, and complexity of the circuit. Furthermore, the switch voltage stress in the switched-inductor boost converter is relatively high with a limited value of gain, and in quadratic converters switch voltage stress value is the same as output voltage [18]. On the other hand, in the cascade boost converter, even though the two switches can be combined to make one switch to reduce circuit complexity, the voltage and current stress across the switch are still high [19]. The major drawback of the converter topologies based on switched capacitor cells and voltage lift cells is high power switches and diodes current stress due to the presence of capacitor networks, hence leading to efficiency reduction. A high gain and high efficiency can be achieved by employing the interleaved converter technique with a lesser number of control switches and filter size reduction [20]. However, the parallel connection of numerous converters leads to increased complexity and drive circuitry. Furthermore, the other drawbacks associated with this technique are complex switching control logic, high voltage/current stress, and high loss in energy [2].

To achieve a high gain in voltage, this paper proposes a novel converter topology with reduced current stress across active switches to provide a stable constant dc voltage. The proposed topology has the advantage of providing a high voltage gain, low current stress, and low conduction loss on the active switches, simplified control, and high efficiency. The current is equally shared by both the switches and thereby reducing the conduction loss. The proposed converter topology is a transformer-less design. Both the switches are connected in parallel and thereby reducing the switch current stress. Therefore, the power circuit of the proposed converter can be designed by using low current rating switches. The solar PV panels can be integrated at 400-V bus of a dc microgrid system by incorporating the proposed converter because of the common ground connection of source and load. The proposed converter is more appropriate and a better option for PV application of 400V DC microgrid because of its properties of achieving high voltage gain, operation in a wide duty range, and unidirectional power flow. As required for the PV applications, the proposed converter is able to draw a continuous input current with low ripples from the input source. To step-up the voltage, the stages of diode/capacitor are cascaded together which in turn limits the switches, diodes, and capacitors voltage stresses. The proposed converter is a viable solution for the integration of solar PV panels into a DC microgrid because of the above-mentioned benefits where a high overall output voltage can be obtained by incorporating the proposed converter with each PV panel.

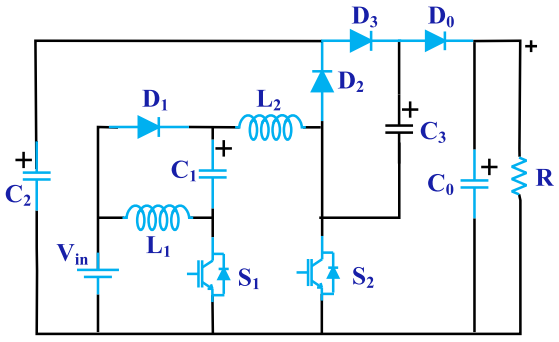

FIGURE 2. Power circuit of the proposed converter.

II. PROPOSED TOPOLOGY

The power circuit of the proposed converter is displayed in Fig. 2. It is consisting of two inductors L_1 and L_2 which have the same inductance value and switch S_1 and switch S_2 are both being turned ON and OFF at once. There are four

diodes (D_0 to D_3) and four capacitors (C_0 to C_3) in the circuit. The working principles and the steady-state analysis of the proposed converter in both CCM and DCM are discussed below.

The analysis of the steady-state characteristics for the proposed converter has been carried out on the basis of certain assumptions. First of all, considering all the circuit components to be ideal. Neglecting the ON-state resistance of the active switches, the forward voltages drop of the diodes and the effective series resistance (ESR) of the inductors and capacitors. However, it is assumed that both the inductors have equal inductance value and all the capacitors are large enough, and the capacitor voltages are considered to be constant.

A. WORKING PRINCIPLE IN CCM

The proposed converter consisting of two switches that are operating at the same time with the same duty pulse and duty ratio. Therefore, the proposed converter has two operating modes in CCM as CCM_1 and CCM_2.

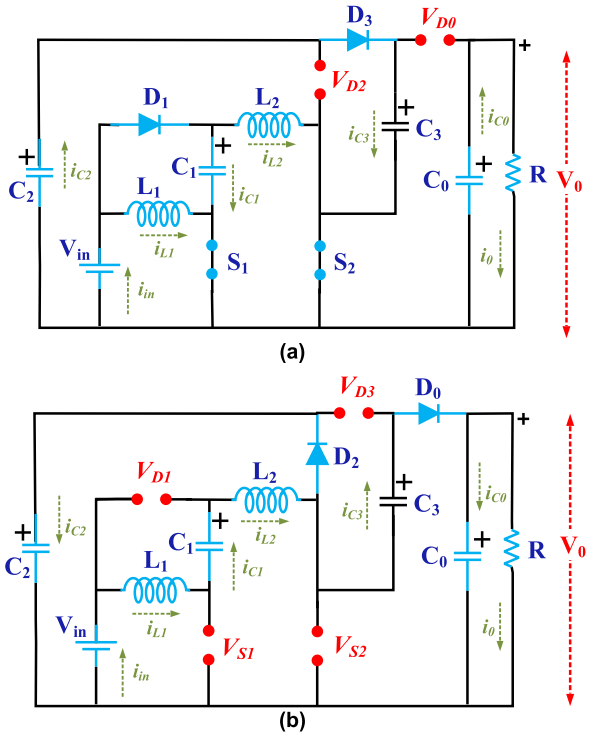

FIGURE 3. Modes of operation of the proposed converter (a) CCM_1 and (b) CCM_2.

***CCM*$_1$**: The switch S_1 and switch S_2 both are kept ON during mode I. The equivalent circuit of the proposed converter for this mode is displayed in Fig. 3(a). The input supply V_{in} charges inductor L_1 via switch S_1, the capacitor C_1 via diode D_1 and switch S_1, and inductor L_2 via diode D_1 and switch S_2, respectively. Simultaneously, capacitor C_3 is charged by capacitor C_2 via diode D_3 and switch S_2, and the energy stored in capacitor C_0 is transferred to the load R. Therefore, the voltages across the inductors L_1 and L_2, and capacitors C_1 and C_3 can be expressed as,

$$\begin{cases} V_{L1} = V_{L2} = V_{in} \\ V_{C1} = V_{in} \\ V_{C3} = V_{C2} \end{cases} \tag{1}$$

where, V_{L1} and V_{L2} are the voltages across inductors L_1 and L_2, respectively; the voltages across capacitors C_1 and C_3 are V_{C1} and V_{C3}, respectively. The characteristics waveform of the proposed converter for each component in ideal condition is displayed in Fig. 4.

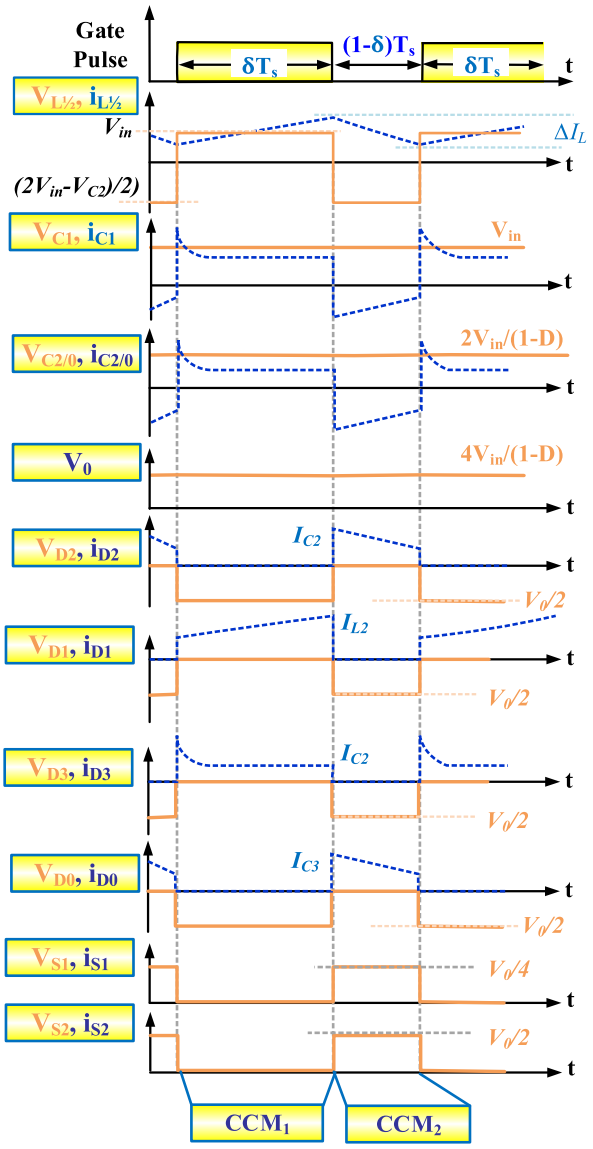

FIGURE 4. Characteristics waveform of the proposed converter in CCM.

***CCM*$_2$**: During mode 2, switch S_1 and switch S_2 are both being turned OFF simultaneously. Mode 2 equivalent circuit of the proposed converter is displayed in Fig. 3(b). In mode 2, the input supply V_{in} charges the output capacitor C_0, inductor L_1, capacitor C_1, inductor L_2, and capacitor C_3 via diode D_0. At the same time, capacitor C_2 is charged by the input

supply voltage V_{in}, inductor L_1, capacitor C_1, and inductor L_2 through diode D_2. Therefore, the voltages across the inductors L_1 and L_2 can be calculated by using equations (2) and (3),

$$\begin{cases} V_{L1} + V_{L2} = V_{in} + V_{C1} + V_{C3} - V_0 \\ V_L = \dfrac{2V_{in} + V_{C3} - V_0}{2} \end{cases} \tag{2}$$

$$\begin{cases} V_{L1} + V_{L2} = V_{in} + V_{C1} - V_{C2} \\ V_L = \dfrac{2V_{in} - V_{C2}}{2} \end{cases} \tag{3}$$

where $V_{L1} = V_{L2} = V_L$; the value of capacitor voltage for the output capacitor C_0 is same as the output voltage V_0. From (1) and (3),

$$\begin{cases} V_{in}\delta + \left(V_{in} - \dfrac{V_{C2}}{2}\right)(1-\delta) = 0, \\ V_{C2} = \dfrac{2V_{in}}{1-\delta} \end{cases} \tag{4}$$

where δ is the duty ratio. From (1) and (2),

$$\begin{cases} V_{in}\delta + \left(\dfrac{2V_{in} + V_{C3} - V_0}{2}\right)(1-\delta) = 0, \\ V_0 = \dfrac{2V_{in}}{1-\delta} + V_{C2} \end{cases} \tag{5}$$

From (4) and (5), in the ideal condition, the output voltage and output current are expressed as,

$$\begin{cases} V_0 = \dfrac{4V_{in}}{1-\delta} \\ I_0 = \dfrac{1-\delta}{4} I_{in} \end{cases} \tag{6}$$

Therefore, by simplifying (6) the voltage gain is expressed as,

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{4}{1-\delta} \tag{7}$$

B. WORKING PRINCIPLE IN DCM

The proposed converter work in DCM as soon as the inductor current reaches zero level in CC_2 of CCM. Therefore, there are three different working modes in DCM for the proposed converter: DCM_1, DCM_2, and DCM_3.

***DCM*$_1$**: The working principle of DCM_1 is the same as that of CCM_1. The peak values of currents through the inductors L_1 and L_2 can be calculated by using equation (8),

$$(I_{L1})_P^I = (I_{L2})_P^I = \frac{V_{in}\delta T_S}{L} \tag{8}$$

***DCM*$_2$:** During mode 2, both the switches S_1 and S_2 are kept OFF. The peak values of currents through the inductors L_1 and L_2 in this mode can be calculated by using equation (9),

$$(I_{L1})_P^{II} = (I_{L2})_P^{II} = \frac{(2V_{in} - V_{C2} - V_0)\,\delta_2 T_S}{2L} \tag{9}$$

***DCM*$_3$**: During mode 3, switch S_1 and switch S_2 are both being turned OFF simultaneously. The power circuit in DCM_3 for the proposed converter is displayed in Fig. 5(a) and its respective characteristics waveform in ideal condition is displayed in Fig. 5(b). Zero energy is stored in both the induc-

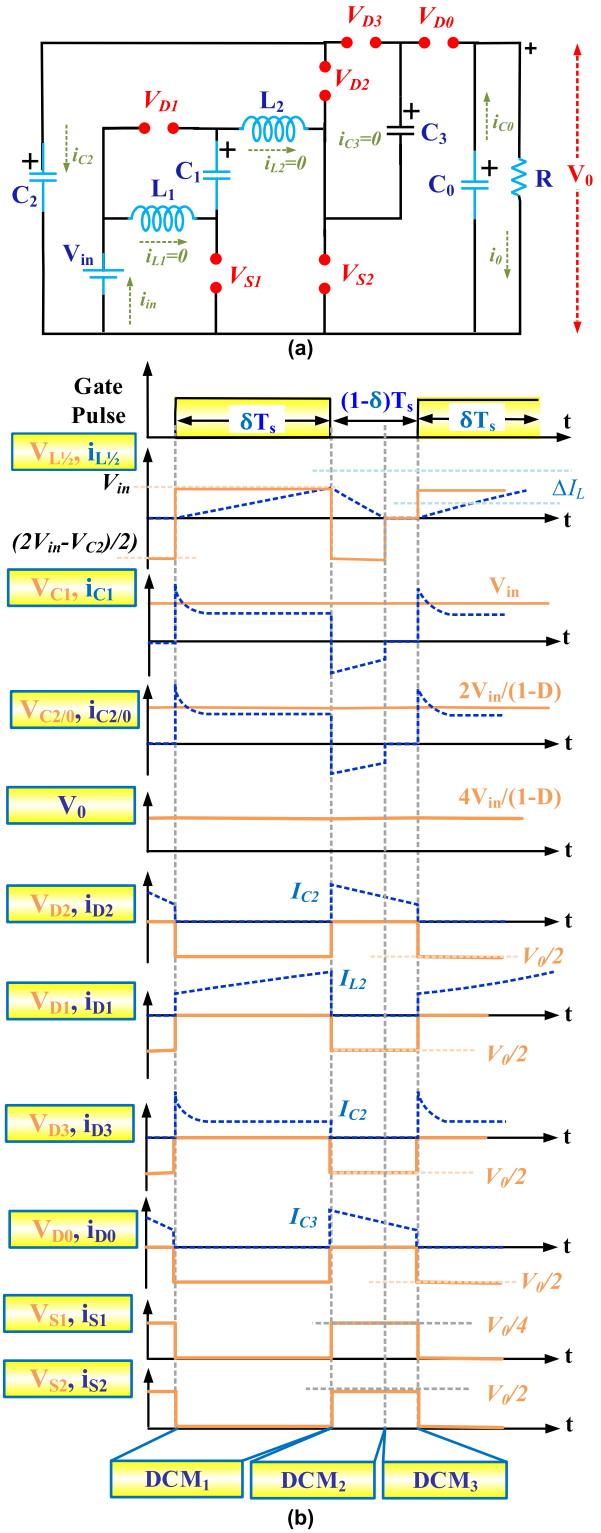

FIGURE 5. (a) Power circuitry in DCM_3 and (b) Characteristics waveform of the proposed converter in DCM.

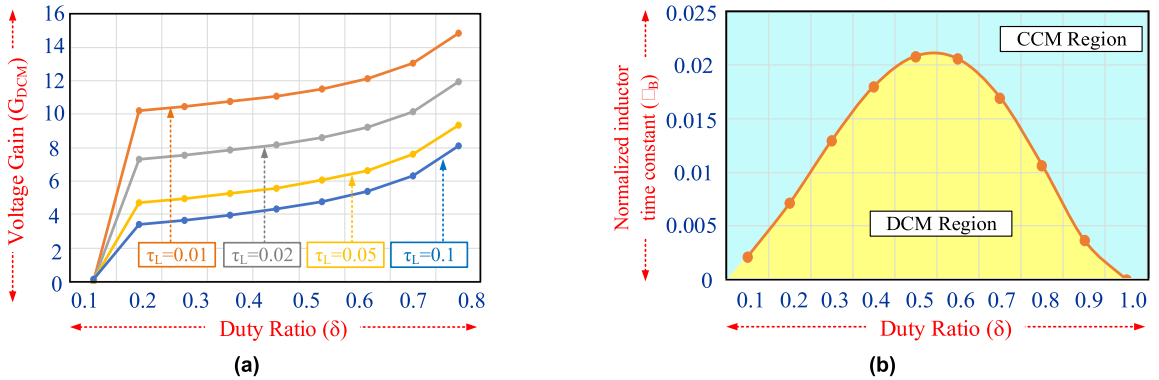

FIGURE 6. (a) Gain in Voltage and (b) DCM boundary condition w.r.t. duty ratio for the proposed converter.

tors L_1 and L_2. Hence, only the energy stored in the capacitor C_0 connected at the output is transferred to the load R. The value of δ_2 can be obtained by (8) and (9),

$$\delta_2 = \frac{2V_{in}\delta}{(2V_{in} - V_{C2} - V_0)} \tag{10}$$

From the characteristics waveform, the average value of the current through the output capacitor for one switching period is expressed as,

$$I_{C0} = \frac{\frac{1}{2}\delta_2 T_S\,(I_{L1})_P - I_0 T_S}{T_S} = \frac{1}{2}\delta_2\,(I_{L1})_P^I - I_0 \tag{11}$$

From (8) & (10), under steady-state conditions

$$\frac{(V_{in}\delta)^2\,T_S}{(2V_{in} - V_{C2} - V_0)\,L} = \frac{V_0}{R} \tag{12}$$

After rearranging (12),

$$G_{DCM} = \frac{\delta}{1-\delta} + \delta\sqrt{\frac{\delta}{(1-\delta)^2} + \frac{1}{\tau_L}} \tag{13}$$

where the normalized time constant for the inductor (τ_L) is defined as $\tau_L = \frac{L}{RT_S}$. Fig. 6(a) shows the variation of the voltage gain of the proposed converter in DCM with the change in duty ratio.

Boundary conditions can be obtained by equating $G_{CCM} = G_{DCM}$. Thus, the normalized boundary time constant for the inductor (τ_{LB}) can be obtained as,

$$\tau_{LB} = \frac{(1-\delta)^2\,\delta^2}{4 - 2\delta} \tag{14}$$

Fig. 6(b) shows the boundary condition of CCM and DCM of the proposed converter w.r.t. duty ratio. It is also observed that, if τ_L is greater than τ_{LB}, the proposed converter works in CCM.

III. EFFECT OF INDUCTOR MISMATCHED

The operation of proposed converter depends on the values of the inductors L_1 and L_2. Hence, the currents through inductors L_1 and L_2 depend on the values of inductors L_1 and L_2.

A. WHEN VALUE OF L_1 LARGER THAN VALUE OF L_2

The characteristics waveform of the inductors L_1 and L_2 currents are shown in Fig. 7(a) below. In this case the converter operates in three modes as follows,

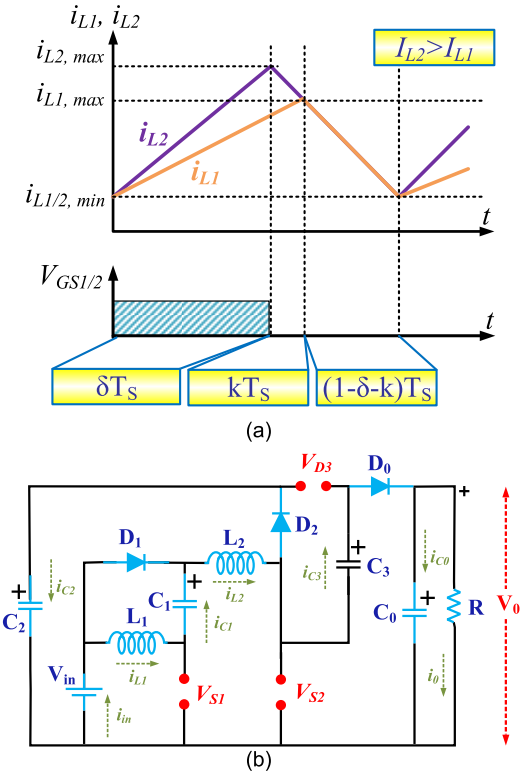

FIGURE 7. When $L_1 > L_2$ (a) inductor currents, and (b) Mode II.

1) MODE I (δT_S)

In this mode, switches S_1 and S_2 are turned ON and equivalent circuitry is same as mode I of CCM. The input supply V_{in} charges inductor L_1 via switch S_1, the capacitor C_1 via diode D_1 and switch S_1, and inductor L_2 via diode D_1 and switch S_2, respectively. Simultaneously, capacitor C_3 is charged by capacitor C_2 via diode D_3 and switch S_2, and the energy

stored in capacitor C_0 is transferred to the load R. The input current I_{in} is the sum of inductors currents i.e. $I_{in} = I_{L1} + I_{L2} + I_{C1}$. The slope of the inductor L_1 and L_2 currents can be obtained as follows,

$$\frac{d\,(I_{L1})}{dt} \approx \frac{V_{in}}{L1}, \frac{d\,(I_{L2})}{dt} \approx \frac{V_{in}}{L2} \tag{15}$$

In this mode, the current through inductor L_2 is larger than current through inductor L_1 since $L_2 < L_1$.

2) MODE II (kT_S)

This mode occurs for small time duration of kT_s as shown in Fig. 7(a). When switches S_1 and S_2 are just turned OFF. The equivalent circuitry is shown Fig. 7(b), where diode D_1 is forward biased. During this mode, the current through inductor L_1 increases with a positive slope and the current through inductor L_2 decreases with large negative slope. The value of current through inductor L_2 is larger than current through inductor L_1. Also, the input current I_{in} is equal to inductor L_2 current i.e. $I_{in} = I_{L2}$ and the resultant current through diode D_1 is subtraction of inductors L_2 and L_1 currents. i.e. $I_{L2} - I_{L1}$. The slope of the inductors L_1 and L_2 currents are obtained as follows,

$$\frac{d\,(I_{L1})}{dt} \approx \frac{V_{C1}}{L1} \approx \frac{V_{in}}{L1}, \quad \frac{d\,(I_{L2})}{dt} \approx \frac{V_{in} - V_{C2}}{L2} \approx \frac{V_{in} + V_{C3} - V_o}{L2} \tag{16}$$

This mode ends as soon as the currents through inductor La and Lb are equal, and circuitry operates in mode III.

3) MODE III (1-k-δT_S)

In this mode, switches S_1 and S_2 are turned OFF and equivalent circuitry is same as CCM mode II. In mode 2, the input supply V_{in} charges the output capacitor C_0, inductor L_1, capacitor C_1, inductor L_2, and capacitor C_3 via diode D_0. At the same time, capacitor C_2 is charged by the input supply voltage V_{in}, inductor L_1, capacitor C_1, and inductor L_2 through diode D_2. In this case, input current and the current through inductor L_2 and L_1 are equal i.e. $I_{in} = I_{L1} = I_{L2}$. The voltage across inductor L_1 and L_2 can be obtained as follows,

$$\frac{d\,(I_{L1})}{dt} = \frac{2V_{in} - V_o}{L_1 + L_2}, \quad \frac{d\,(I_{L2})}{dt} = \frac{2V_{in} - V_o}{L_1 + L_2} \tag{17}$$

Using small approximation and inductor volt second balance,

$$For\ L_1 \Rightarrow V_{in}(\delta) + V_{in}(k) + \frac{2V_{in} + V_{C3} - V_o}{L_1 + L_2} L_1 \times (1 - k - \delta) = 0 \tag{18}$$

$$For\ L_2 \Rightarrow V_{in}(\delta) + (V_{in} + V_{C3} - V_o)k + \frac{2V_{in} - V_o}{L_1 + L_2} L_2 \times (1 - k - \delta) = 0 \tag{19}$$

Solving (18)-(19), voltage gain of TBC is obtained as,

$$\left.\frac{V_o}{V_{in}}\right|_{L_1 > L_2} = \frac{4}{(1 - \delta)} \tag{20}$$

IV. COMPARATIVE ANALYSIS

In this section, a comparative study of the proposed converter with other similar high gain converter structures is presented, such as the multilevel boost converter [26], non-isolated DC-DC boost converter with voltage-lift technique [18], Traditional switched inductor based DC-DC boost converter [21], converter-I in [22], modified SEPIC converter in [23], ASL-SU2C-VO-configuration [24], and modified SEPIC converter (MSC) [25]. The number of components, normalized voltage stress across the switches, switch current stress, efficiency at rated power, and the gain in voltage for these converters are presented in Table 1. The proposed converter achieves a higher voltage gain as compared to the topologies presented in [18], [21]–[26] for the same duty cycle range. Therefore, small voltage rating active switches having small ON-state resistance can be used in the circuit, which leads to the reduction of cost.

The converters presented in [21], [23], and [25] utilizes only one power switch. However, high voltage stress has been generated across the switch and the voltage gain is lower than the topology proposed. The number of diodes used in the converters [18] and [21] is the same as the proposed converter. However, their voltage gain is lower and the switch voltage stress is higher than the proposed converter.

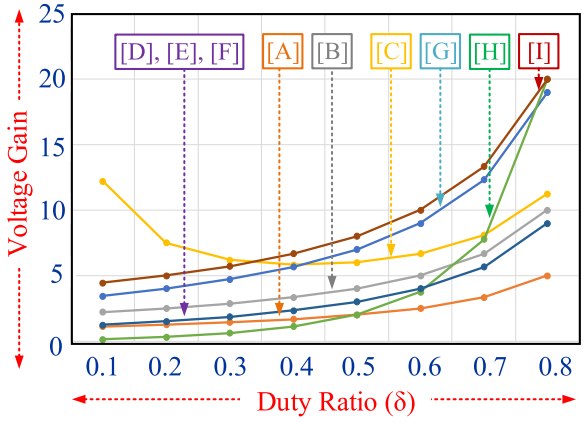

FIGURE 8. A Comparative graphical representation of the proposed converter with different converters for the voltage gain with respect to duty ratio.

From Fig. 8, the proposed converter is observed to be providing a higher gain in voltage in comparison with the converters presented in [21]–[26]. Furthermore, the output and input of the proposed converter and the converters in [18], [21], [23], and [26] are at common ground, while the rest of the other converters are suitable for floating load conditions only. Table 1 indicates that the proposed converter provides a lesser switch voltage stress as compared to the converters in [18], [21]–[25]. The efficiency of the proposed converter is observed to be higher than all the other converters. The efficiency of a converter depends on different factors such as the components count, their types, and voltage/current ratings. The comparison with regards to switch current stress

TABLE 1. Comparative study of the proposed converter with other existing DC-DC converters.

Conv.	Reactive components count		Semiconductor Components count		Total compo nents	CCM Voltage gain (M)	Normalized Switch voltage stress	Switch current stress	Efficiency	Output port
	Inductor	Capacitor	Switches	Diodes						
A	1	1	1	1	4	$1/(1-\delta)$	1	I_{in}	-	Grounded
B	1	3	1	3	8	$2/(1-\delta)$	1/2	$I_{in}+I_{C1}$	94.6% at 100W	Grounded
C	2	2	2	4	10	$(1+\delta)/\delta(1-\delta)$	1/(1- δ)M	$2I_{in}/1+\delta$	-	Grounded
D	2	1	1	4	8	$(1+\delta)/(1-\delta)$	1	I_{in}	95.2% at 50W	Grounded
E	2	1	2	1	6	$(1+\delta)/(1-\delta)$	(1+M)/M	$2I_{in}/1+\delta$	92.7% at 40W	Floating
F	2	3	1	2	8	$(1+\delta)/(1-\delta)$	(1+M)/2M	I_{in}	92.2% at 100W	Grounded
G	3	4	1	4	12	$(3+\delta)/(1-\delta)$	M/(3+ δ)	$I_{in}+I_{C1}$	94.4% at 250W	Floating
H	3	3	1	3	10	$\delta/(1-\delta)^2$	1	$I_{in}+I_{C1}+I_{C2}$	91.4% at 100W	Grounded
I	2	4	2	4	12	$4/(1-\delta)$	1/2, 1/2	$I_{in}/2$, $I_{in}/2$	96.5% at 200W	Grounded

A: Traditional Boost Converter, B: multilevel boost converter [26], C: non-isolated DC-DC boost converter with voltage-lift technique [18], D: Traditional switched inductor based DC-DC boost converter [21], E: converter-I in [22], F: modified SEPIC converter in [23], G: qZS-BCVLSI-configuration [24], H: modified SEPIC converter (MSC) [25], I: proposed converter.

among the different converters indicates that the proposed converter has the lowest switch current stress through the active switches and the value is half the value of input current. Hence, active switches with low current rating are required as the total input current is shared by these two active switches. Generally, the increase in the rating of a device leads to an increment in its ON-state resistance. The proposed converter topology requires lower rating components and hence it comes up with a low-cost design and generates higher efficiency.

From the comparative analysis, the proposed converter is observed to be providing a reduced value of switch voltage and switch current stresses in comparison with the other converters. Hence, small voltage rating active switches having small ON-state resistance can be used in the circuit. The proposed converter can attain a high voltage gain and an improved efficiency as compared to the other converters. Furthermore, the common ground connection of source and load in the proposed converter circuit makes it highly suitable for DC Microgrid integrated with solar PV.

V. EFFICIENCY ANALYSIS

The total power loss for the proposed converter comprises of the loss in the inductors, loss in the switches, and loss in the diodes. The power circuit of the proposed converter considering the non-ideality of different circuit components is displayed in Fig. 9. Where Equivalent Series Resistance (ESR) for the inductor L_1 and inductor L_2 are indicated by r_{L1} and r_{L2}, respectively. Similarly, r_{D1}, r_{D2}, r_{D3}, and r_{D0} are internal resistance; the drops in forward voltages for the diodes D_1, D_2, D_3, and D_0 are V_{F1}, V_{F2}, V_{F3}, and V_{F0}, respectively. Whereas, the forward ON state resistances of the control switches S_1 and S_2, are indicated by R_{S1} and R_{S2}, respectively.

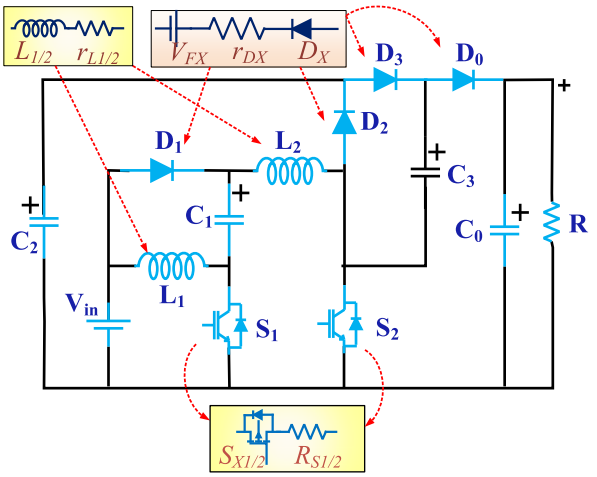

FIGURE 9. The power circuit of the proposed converter considering the non-ideality of different circuit components.

A. INDUCTOR LOSS

The power loss in the inductor includes the core loss and the copper loss.

$$P_L = Core\ Loss + Copper\ Loss \tag{21}$$

For an MPP of 125 μ, the inductor core loss is obtained as follows:

$$P_{Lcore} = 0.33B^{1.98}f^{1.64}A_C l_m \tag{22}$$

where, B is the half of the ac flux swing, f is the frequency, A_C is the core cross-sectional area, and l_m is the core mean magnetic path length.

The RMS value of inductor L_1 and L_2 is calculated as

$$\left.\begin{aligned} I_{L1(RMS)} &= \frac{I_{in}}{2} = \frac{V_0^2}{RV_{in}} \\ I_{L2(RMS)} &= \frac{I_{in}}{2} = \frac{V_0^2}{RV_{in}} \end{aligned}\right\} \tag{23}$$

Thus, total inductor copper loss is calculated as

$$\left.\begin{aligned} P_{LCu} &= I_{L1(RMS)}^2 r_{L1} + I_{L2(RMS)}^2 r_{L2} \\ &= \left(\frac{32V_{in}}{(1-\delta)^2 R}\right)^2 r_L \end{aligned}\right\} \tag{24}$$

Thus, total inductor power loss is calculated as

$$P_L = 0.33B^{1.98} f^{1.64} A_C l_m + \left(\frac{32V_{in}}{(1-\delta)^2 R}\right)^2 r_L \tag{25}$$

B. SWITCH LOSS

The switching power losses of S_1 and S_2 are denoted by P_{SW-S1} and P_{SW-S2}, respectively. Where P_{SW-S} denotes the total switching loss during switching and can be expressed as,

$$\begin{aligned} P_{SW-S} &= \sum_{i=1,2} P_{SW-Si} \\ &= \frac{1}{2T}\left\{\begin{aligned} &(I_{S1} \times V_{S1})(t_{R-S1} + t_{F-S1}) \\ &+ (I_{S2} \times V_{S2})(t_{R-S2} + t_{F-S2}) \end{aligned}\right\} \end{aligned} \tag{26}$$

where, the rising and falling times of S_1 and S_2 are indicated by t_{R-S1}, t_{F-S1}, and t_{R-S2}, t_{F-S2}, respectively; the value of average switch current through S_1 and S_2 are indicated by I_{S1} and I_{S2}, and the switch voltages of S_1 and S_2 are indicated by V_{S1}, and V_{S2} respectively. The switch conduction losses of S_1 and S_2 are calculated by using equation (27)

$$\left.\begin{aligned} P_{con} &= I_{S1(RMS)}^2 r_{DS1} + I_{S2(RMS)}^2 r_{DS2} \\ &= \left(\frac{32V_{in}\delta}{(1-\delta)^2 R}\right)^2 r_{DS} \end{aligned}\right\} \tag{27}$$

Thus, the total loss by the switches is calculated as

$$P_S = P_{SW-S} + P_{con} \tag{28}$$

C. DIODE LOSS

The power loss contributed by the diode is the addition of loss by internal forward voltage drop (V_F) and loss by internal forward resistance (r_D) which is calculated as

$$P_{D,loss} = P_{D(VF)} + P_{D(rD)} \tag{29}$$

The power loss by the diode due to the forward voltage drop of V_F is calculated as,

$$\left.\begin{aligned} P_{D(VF)} &= \left(I_{D1(avg)} + I_{D2(avg)} + I_{D3(avg)} + I_{D0(avg)}\right) V_F \\ &= \left(\frac{8(1-\delta)V_{in}}{(1-\delta)^2 R}\right)^2 V_F \end{aligned}\right\} \tag{30}$$

The diode power loss caused by the internal forward resistance r_L is calculated as,

$$\left.\begin{aligned} P_{D(r_D)} &= \left(I_{D1(RMS)} + I_{D2(RMS)} + I_{D3(RMS)} + I_{D0(RMS)}\right)^2 r_D \\ &= \left(\frac{4(4-3\delta)V_{in}}{(1-\delta)^2 R}\right)^2 r_D \end{aligned}\right\} \tag{31}$$

Therefore, the efficiency of the proposed converter can be calculated by using equations (25)-(31) as (32), shown at the bottom of the page.

VI. DESIGN OF CIRCUIT COMPONENTS

The inductor and capacitor design is an essential element of the converter design. The selection of inductors is done on the basis of the inductor current, while the capacitor is selected on the basis of the capacitor voltage.

A. INDUCTOR DESIGN

The equivalent voltage developed across both the inductors L_1 and L_2 are obtained as,

$$V_{L1} = V_{L2} = L\frac{di}{dt} \tag{33}$$

The inductor value is selected on the basis of the average value of charging current, its ripples, duty ratio, and switching frequency. The ripple current through each inductor in the charging condition is obtained as follows,

$$\frac{V_{in}\delta T_S}{L} = \Delta i_{L1} = \Delta i_{L2} \tag{34}$$

$$\left.\begin{aligned} \eta &= \frac{P_o}{P_{in} + P_{loss}} = \frac{P_o}{P_{in} + P_L + P_S + P_{D,loss}} \\ &= \frac{P_o}{P_{in} + P_{LCore} + P_{LCu} + P_{SW-S} + P_{con} + P_{D(VF)} + P_{D(r_D)}} \\ &= \frac{2(1-\delta)^4 I_{in} R V_o^2 T}{\left(\begin{aligned} &2T\left[\begin{aligned} &(1-\delta)^4 R\left\{V_{in}R + 0.33B^{1.98} f^{1.64} A_C l_m I_{in}\right\} \\ &+ 16V_{in}^2 I_{in}\left\{64\left(r_L + \delta^2 r_{DS}\right) + 4(1-\delta)^2 V_F + (4-3\delta)^2 r_D\right\} \end{aligned}\right] \\ &+ V_{in} I_{in}(1-\delta)^3 R^2\left\{I_{S1}\left(t_{R-S1} + t_{F-S1}\right) + 2I_{S2}\left(t_{R-S2} + t_{F-S2}\right)\right\} \end{aligned}\right)} \end{aligned}\right\} \tag{32}$$

where, the values of ripple currents for the inductor L_1 and inductor L_2 are indicated by Δi_{L1} and Δi_{L2}, respectively. Therefore, for the CCM operation of the proposed converter, the critical values of each inductor can be calculated as,

$$(L_1)_{Cri} = (L_2)_{Cri} = \frac{V_{in}\delta T_S}{\Delta i_{L1/2}} = \frac{V_{in}\delta}{\Delta i_{L1/2} f_S} \tag{35}$$

Thus, the value of both the inductors can be chosen based on (29), where Δi_{L2} is 20-40% of the average inductor current value and f_s is the switching frequency to control the switch.

B. CAPACITOR DESIGN

The capacitor value is controlled by its charging current, the voltage ripple across it, duty ratio, and switching frequency. During CCM_1 the Capacitors C_1 and C_3 are being charged and being discharged during CCM_2 with a value of current equal to I_{L1}. Thus, the capacitor voltage ripple for C_1 and C_3 can be obtained as follows,

$$\Delta V_{C1} = \frac{i_{L1}\,(1-\delta)\,T_S}{C_1} = \frac{i_{L1}\,(1-\delta)}{C_1 f_S} = \Delta V_{C3} \tag{36}$$

Capacitors C_0 is charged in Mode I and discharged in Mode II with a value of current equal to I_0. Thus, the capacitor voltage ripple for C_0 can be obtained as,

$$\Delta V_{C0} = \frac{i_0\,(1-\delta)\,T_S}{C_0} = \frac{i_0\,(1-\delta)}{C_0 f_S} \tag{37}$$

Capacitors C_2 is charged in Mode II with a value of current equal to I_{L1}. Thus, the capacitor voltage ripple for C_2 can be obtained as,

$$\Delta V_{C2} = \frac{i_{in}\,(1-\delta)\,T_S}{2C_2} = \frac{i_{in}\,(1-\delta)}{2C_2 f_S} \tag{38}$$

With the help of (36)-(38), the critical values of capacitors C_1, C_2, C_3, and C_0 can be calculated by using equations (36)-(41),

$$C_1 = C_3 \geq \frac{i_{in}\,(1-\delta)}{2\Delta V_{C1} f_S} \tag{39}$$

$$C_0 \geq \frac{i_0\,(1-\delta)}{\Delta V_{C0} f_S} \tag{40}$$

$$C_2 \geq \frac{i_{in}\,(1-\delta)}{2\Delta V_{C2} f_S} \tag{41}$$

where, ΔV_{C1}, ΔV_{C2}, and ΔV_{C0} are the voltage ripple contents of the capacitors C_1, C_2, and C_0 respectively; i_0 is the output current.

C. SELECTION OF DIODES

It is observed that diodes D_1 and D_3 are only conducting in Mode I to charge the Capacitors C_1 and C_3, respectively. The diodes D_2 and D_0 are conducting in Mode 2 to charge the Capacitors C_2 and C_0, respectively. The maximum value of voltage stress across all the diodes are expressed as follows,

$$Diode\ D_1: \begin{cases} 0, & 0 < t < \delta \\ -\dfrac{V_0}{2}, & \delta < t < \delta T_S \end{cases} \tag{42}$$

$$Diode\ D_2: \begin{cases} -\dfrac{V_0}{2}, & 0 < t < \delta \\ 0, & \delta < t < \delta T_S \end{cases} \tag{43}$$

$$Diode\ D_3: \begin{cases} 0, & 0 < t < \delta \\ -\dfrac{V_0}{2}, & \delta < t < \delta T_S \end{cases} \tag{44}$$

$$Diode\ D_0: \begin{cases} -\dfrac{V_0}{2}, & 0 < t < \delta \\ 0, & \delta < t < \delta T_S \end{cases} \tag{45}$$

Therefore, the diodes are selected to sustain the voltage stress shown in (46).

$$V_{D1} \geq \frac{V_0}{4}, \quad V_{D2} = V_{D3} = V_{D0} \geq \frac{V_0}{2} \tag{46}$$

D. SELECTION OF SWITCHES

The switches S_1 and S_2 have been selected on the basis of their respective voltage stress values in the circuit. The switch voltages across S_1 and S_2 are observed to be zero in Mode I. The maximum voltage stress values of the switches S_1 and S_2 is expressed as follows,

$$Switch\ S_1: \begin{cases} 0, & 0 < t < \delta \\ \dfrac{V_0}{4}, & \delta < t < \delta T_S \end{cases} \tag{47}$$

$$Switch\ S_2: \begin{cases} 0, & 0 < t < \delta \\ \dfrac{V_0}{2}, & \delta < t < \delta T_S \end{cases} \tag{48}$$

Therefore, the switches S_1 and S_2 have been selected to sustain the voltage stress shown in (49).

$$V_{S1} \geq \frac{V_0}{4}, \quad V_{S2} \geq \frac{V_0}{2} \tag{49}$$

TABLE 2. Design considerations for the proposed converter.

Parameters	Prototype
Power	200 W
Input Voltage (V_{in})	30 V (Ideal)/32V (expt.)
Duty ratio	0.7
Output voltage (V_0)	400 V
Load	800 Ω
Switching freq.	100 kHz
Inductor L_1 and L_2	≈300 µH, 20A (shell type,)
Capacitor C_1	≈50 µF, 400 V
Switches S_1, S_2	V_{DS}=900 V, i_D=36 A, R_{ON}=65 mΩ (C3M0065090)
Diodes (D_0-D_3)	V_{RRM}=400 V, i_F=30 A, R_{ON}=0.01Ω, V_F=0.8 V (STTH30R04)

VII. EXPERIMENTAL ANALYSIS

A 200W laboratory prototype of the proposed converter is develop to validate the theoretical analysis. A list of specifications for the different circuit components of the prototype is presented in Table 2. Furthermore, the ultra-fast recovery diode STTH30R04 is used for all the diodes D_1, D_2,

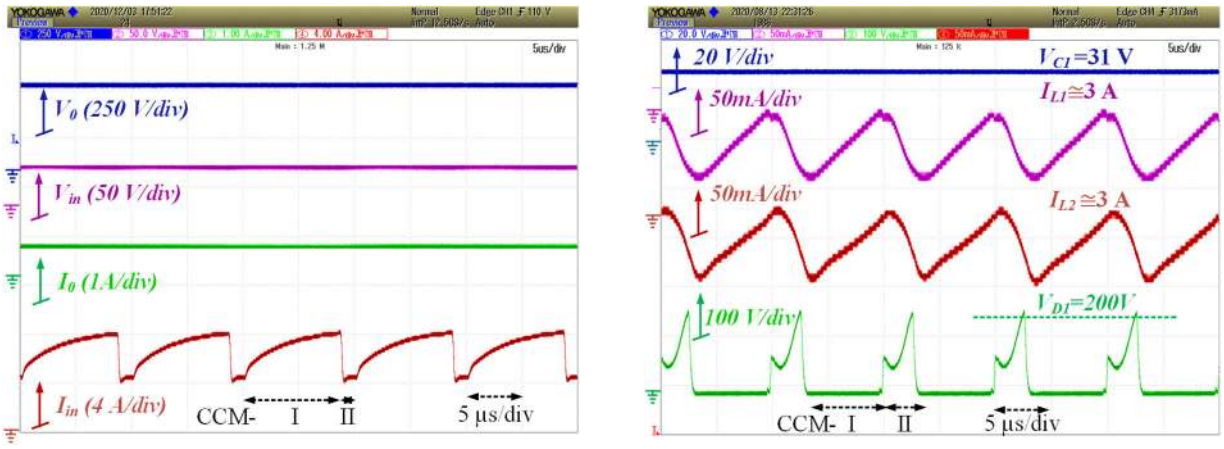

FIGURE 10. Experimentally resulted waveforms for the proposed converter (a) input/output currents and voltages, and (b) inductor currents, voltage across capacitor C_1 and diode D_1.

D_3, and D_0, and silicon carbide MOSFET C3M0065090 is used as the switches S_1 and S_2 for high switching operation and better efficiency. The experimental results are presented in Fig. 10 with the values of $V_{in} = 32$V, $V_0 = 400$V, $f_s = 100$ kHz, and $P_0 = 200$W. The experimentally obtained waveforms of input/output voltages and currents are displayed in Fig. 10(a). The average values of output voltage and output current are observed as 399V and 480mA, while the input voltage with non-ideality and input current average values are observed as 31.5V and 6.3A. The input current is observed to be continuous and increasing with a constant slope in the ON-state and decreasing in the OFF-state because of charging and discharging of inductor L_1 and inductor L_2, respectively. The experimentally obtained waveforms of the currents through inductor L_1 and inductor L_2 along with the voltages across diode D_1 and capacitor C_1 are displayed in Fig. 10(b). The average values of the inductor currents for inductor L_1 and inductor L_2 are observed as 3A and 3.2A, respectively. The experimentally obtained results for the inductor currents have an offset of 3.5A to show the inductor current ripples. The diode D_1 is observed to be forward-biased in the ON state and reversed biased in the OFF state. The PIV across diode D_1 is 50% of the output voltage and its value is equal to (-200V). Fluctuations in voltage waveform are observed for the diode D_1 due to the practical mismatch of inductance value (L_1 and L_2). The voltage across capacitor C_1 is observed as 31V which is almost the same as input voltage. In order to refer and validate the experimentally obtained waveforms of the voltages across diodes D_2, D_3, and D_0, the waveform of the output current I_0 is also displayed in Fig. 11(a). The PIV across all the diodes D_2, D_3, and D_0 is the same as output voltage i.e. -200V. The value of average output current is observed as 480mA. Fig. 11(b) displays the experimentally obtained waveforms of the voltages across capacitors C_2, C_3, and C_0 and waveform of the input current I_{in} in order to refer and validate. The voltages across capacitors C_2, C_3, and C_0 are observed as 199V, 198V, and 398V respectively. Fig. 11(c) presents the experimentally obtained waveforms of the currents through switches S_1 and S_2 and the voltage across switch S_2, the output voltage is also shown for reference and validation purposes. The maximum value of switch voltage stress across S_2 is observed as 200V in CCM_2 which is 50% of the output voltage value. The currents through the switches S_1 and S_2 are observed to be almost same. Fig. 11(d) shows the dynamic behavior of the proposed converter with a change in input voltage at the constant duty ratio and load. It is observed from the experimentally obtained results, that the proposed system giving stable output voltage and current. A disturbance is initiated from the load and source sides to analyze the proposed converter's performance in disturbed condition. The reference of output voltage is set at 400V and the dynamic response of the system is verified by varying the input voltage and the step change in the load resistance as shown in Fig. 12(a) and Fig. 12(b) respectively. As seen from Fig. 12(a), constant output voltage 400V is achieved even when the input voltage varies from the 32V to 40V at the constant power (fixed load resistance). It is observed that, there is no spike in input current during the transition. Similarly, the load resistance is changed to examine the stability of the proposed converter in closed loop to achieve the constant output voltage 400.19V is shown in Fig. 12(b). Here, the load current is varying from 0.03mA to 0.48mA to 0.6mA and the change in the input current can assure the power balance between the input and the output.

The theoretically and experimentally achieved voltage gain of the proposed converter is shown in Fig. 13(a). The parasitic internal resistance of different circuit components is the main cause of the difference between theoretical and experimentally achieved voltage gain values. It can observed from the mathematical analysis, the drop in voltage gain is inversely proportional to the input voltage. Hence with increase in the input voltage, the drop in the output voltage is decreasing.

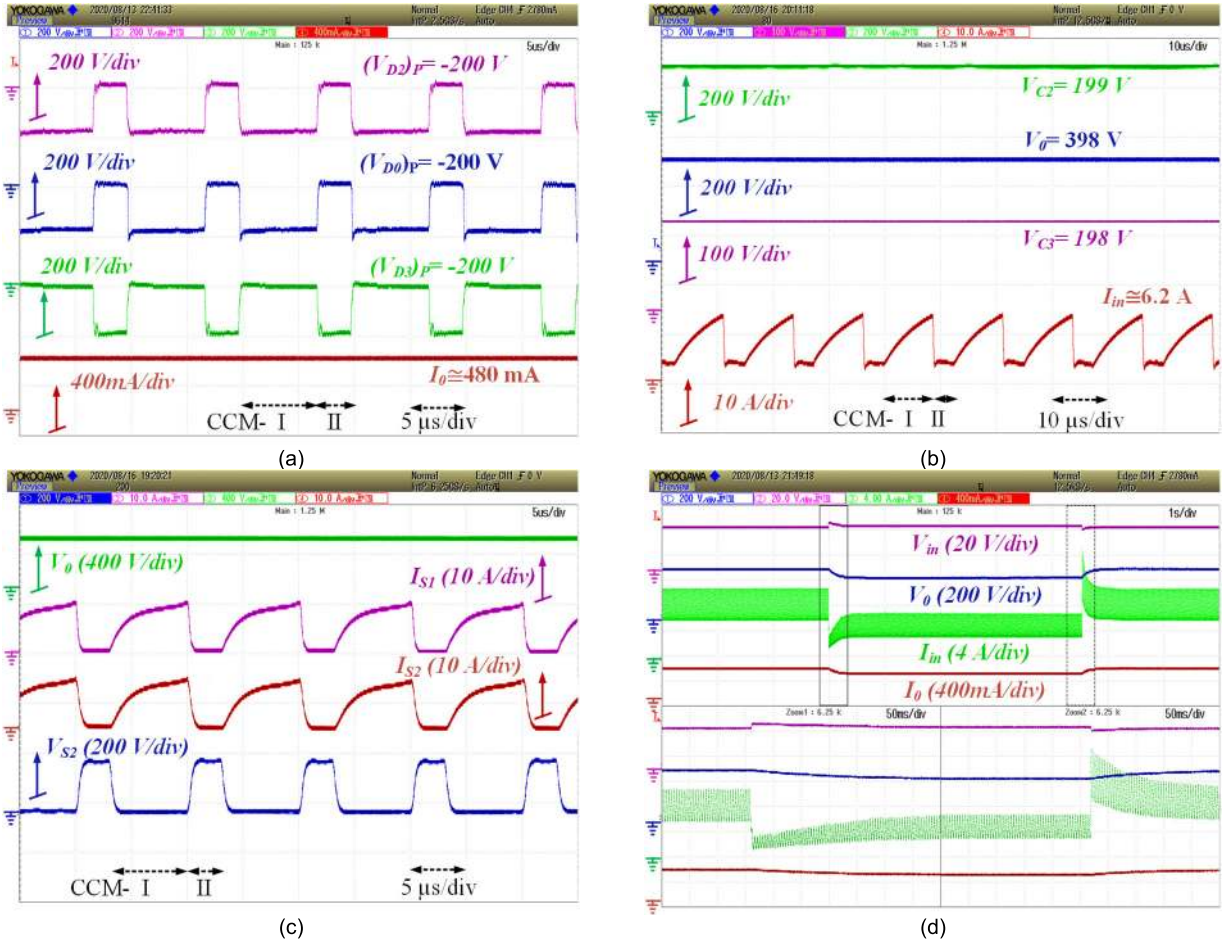

FIGURE 11. Experimental waveform of (a) voltage across diode D_2, D_0, D_3 and output current (b) voltage across capacitor C_2, C_3, C_0 and input current, (c) switch voltage and switch current stress for S_1 and S_2 and (d) dynamic variation of input-output voltage and current with change in duty ratio from 0.6 to 0.5 to 0.6.

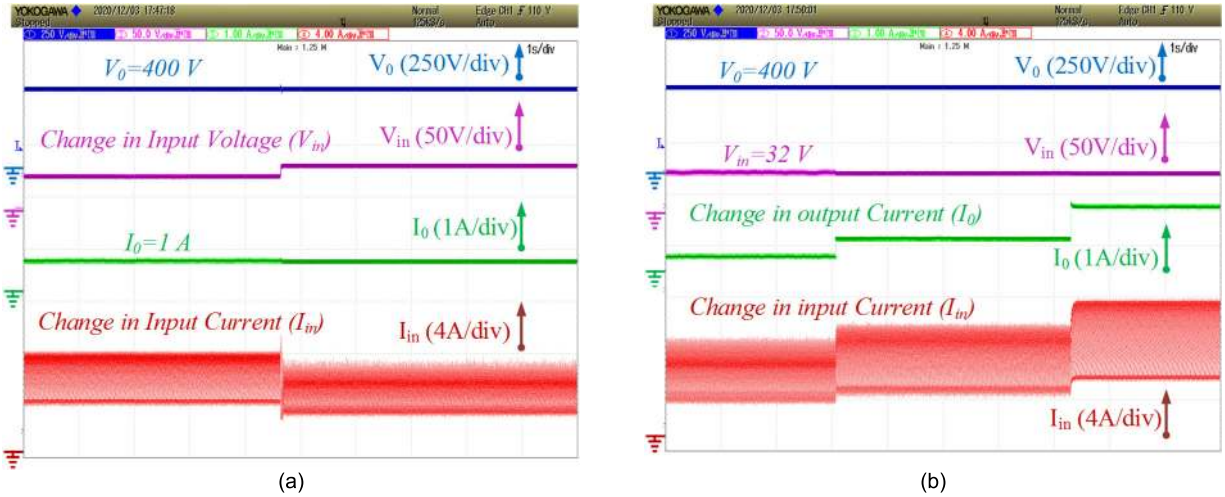

FIGURE 12. Dynamic variation of input-output voltage and current with change in (a) input voltage at constant load and (b) change in load at constant input voltage.

The conduction loss in the proposed converter is depends on the current through each of the components and most of the current through each component directly depends on the input current. Hence at a constant power, the input current is decreasing with increase in the input voltage. Therefore, from mathematical analysis at different input voltage with constant

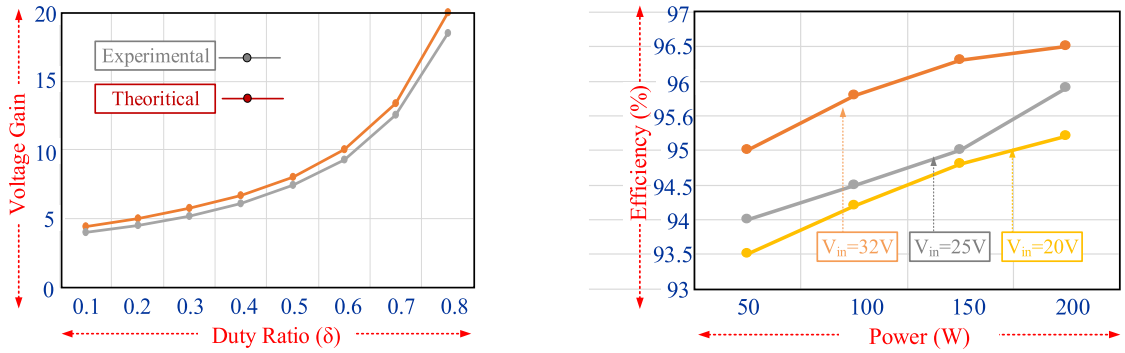

FIGURE 13. (a) Voltage gain comparison between theoretical and experimental value and (b) efficiency with respect to output power for the proposed converter.

power, the proposed converter is experimentally verified and the observed efficiency at different input voltages is plotted in the Fig. 13(b). It can be observed that, the maximum efficiency achieved by the proposed converter is 96.5% at the 200W power with 32V as input voltage.

VIII. CONCLUSION

The DC-DC high gain boost converter with active switched inductor network for 400V DC microgrid has been presented in the paper. The proposed converter has utilized two switches to reduce the current stress. The active switched inductor network and voltage multiplier structure have been effectively arranged to boost the output voltage and for the equal distribution of capacitor voltage stress. Furthermore, the presented topology drains a continuous current from the input supply. Hence, high-voltage boost ability and continuous input current make it suitable for PV and fuel cell applications. A detailed CCM and DCM analysis of the proposed converter has been presented along with the discussion about their boundary conditions. The theoretical and mathematical analysis has been validated by the experimental results. The converter has been regulated at different duty cycle values to test and verify its performance and the peak efficiency is achieved by the proposed converter at 200 W and its value is 96.5%.

ACKNOWLEDGMENT

This publication was made possible by Qatar University Collaborative research project grant # [QUCG-CENG-19/20-5] from the Qatar University. The statements made herein are solely the responsibility of the authors. Open Access funding provided by the Qatar National Library.

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