A New High Precision Low Offset Dynamic Comparator for High Resolution High Speed ADCs

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***Abstract*— A new low offset dynamic comparator for high resolution high speed analog-to-digital application has been designed. Inputs are reconfigured from the typical differential pair comparator such that near equal current distribution in the input transistors can be achieved for a meta-stable point of the comparator. Restricted signal swing clock for the tail current is also used to ensure constant currents in the differential pairs. Simulation based sensitivity analysis is performed to demonstrate the robustness of the new comparator with respect to stray capacitances, common mode voltage errors and timing errors in a TSMC 0.18μ process. Less than 10mV offset can be easily achieved with the proposed structure making it favorable for flash and pipeline data conversion applications.**

***Keywords*—dynamic comparator, offset, ADC, pipeline, flash**

I. INTRODUCTION

In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high resolution and high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device in question. One such application where low power, high resolution and high speed are required is Analog-to-Digital Converters (ADCs) for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. In the literature one will find that a major emphasis has been made in regard to the inter-stage gain amplifiers but very little effort has been made towards the design of comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the high constant power consumption. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less power as compared to the pre-amplifier based comparators. However, these dynamic comparators suffer from large offsets making them less favorable in flash based ADC architectures. In pipeline ADCs, digital correction techniques along with adequate over-range protection can tolerate such large offsets.

In the literature, a few dynamic comparators can be found, e.g. Resistor divider (or Lewis-Gray) [1], Differential pair [2], Capacitive differential pair [3]-[4], however, very little emphasis is placed on actual details of operation of these structures [5]. Few authors talk about how non-idealities due to process variation affect these structures along with experimental results to compare offset values of different structures [5]. These experimental offset values vary from 75mV to 300mV. However, the literature is devoid of any information on how other non-idealities such as imbalance in parasitic capacitors, common mode (CM) voltage errors or clock timing errors affect these structures. The operation and the effects of non-idealities of such dynamic comparators have been investigated in this paper. A new dynamic comparator structure which achieves a low offset has been developed. In the new comparator structure, inputs are reconfigured [6]-[7] from the typical differential pair comparator [2] so that each differential pair branch contributes equal current at the meta-stable operating point (or trip point) along with keeping the differential pair's tail current in saturation region. Comparison of the new architecture with respect to typical differential pair structure [2] is made as both structures share the same base structure. Simulation based sensitivity analysis with respect to different non-idealities has been carried out to validate the advantages of the new structure over typical differential pair comparator.

II. DYNAMIC COMPARATOR DESIGN

A. Differential Pair Comparator

A fully differential typical dynamic comparator is shown in Fig. 1 [2]. The comparator consists of two cross coupled differential pairs with inverter latch at the top. Comparison is made based on the inverter currents, which are related to the inputs, when the ϕ_{clk} goes high. The trip point can be changed by appropriate input transistor sizing [2], [5].

Few points are worth noting in regard to the problems present in this structure. The first drawback of this comparator is related to the clocking of the tail current. When clock signal goes high, the tail current will go into linear region and will be

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function of the inputs of the respective differential pair. If there are any non-idealities or mismatches present (from the point of view of symmetry), the two inverter tail currents will not be same and will result in large offset for the comparator. The second problem is related to the inputs of a differential pair. A large difference between the two inputs to a differential pair will result in the turning off one of the differential pair transistor and all of the tail current will be drawn into the other transistor. Hence, in effect comparator will be only comparing V_{in}^{+} with V_{ref}^{+} (or V_{in}^{-} with V_{ref}^{-}) rather than a comparison of differential V_{in} with differential V_{ref}. The third potential problem is associated with the previous code dependent biased decision. This can happen if there is some charge imbalance left from previous decision at one of the nodes of the comparator which can affect next decision.

To overcome the drawbacks of the typical differential pair mentioned above, a new dynamic comparator has been proposed in the next sub-section which addresses the above listed problems.

B. Proposed Comparator

Proposed dynamic comparator structure is shown in Fig. 2. Operation of this dynamic comparator is same as the typical case. Here also the decision is been made during the period when the ϕ_{clk} goes high. The comparator will have a meta-stable point when both the inverter currents are same.

Few modifications have been made to this structure as compared to the typical structure. The first modification is related to the tail current clock signal. Instead of using the same clock as that for the top switches, which goes from V_{SS} to V_{DD}, a same phase restricted voltage swing clock ($\phi_{clk,B}$) has been used, i.e. $\phi_{clk,B}$ high is less than V_{DD}, which can be easily generated from the main clock by using desired high voltage of an inverter or by using resistor ladder. The restricted swing clock is used to ensure that differential pair tail current remains in the saturation region rather than going into linear region. Thus a constant tail current is achieved. This is very important during the time the comparator is making a decision. The second modification is related to the input signals. As pointed out in the typical differential pair comparator, one of the input transistors will be turned off if there is a large input differential and will result in the comparison of two signals rather than comparison of the two differential signals. To address this problem V_{in}^{+} and V_{ref}^{+} (and V_{in}^{-} and V_{ref}^{-}) are combined in one differential pair as compared to V_{in}^{+} and V_{in}^{-} (and V_{ref}^{+} and V_{ref}^{-}) [6]-[7]. Hence, for a case where all the input transistors are of the same size and no imbalance is present, at the trip point of the comparator, the transistors M_1 and M_2 will have same current, as well as, M_3 and M_4 will have same current. Therefore, all four input transistors will contribute respective currents for making a decision.

The third possible modification is related to the previous code dependent errors. To address this issue, the internal nodes, D_1 and D_2, can be reset to V_{DD} during the phase when the comparator is not making a decision, i.e. when ϕ_{clk} is low [8]. This will ensure all the internal nodes are reset before the comparator goes into the decision mode. However, if parasitic capacitance imbalance is present between D_1 and D_2, resetting these nodes to V_{DD} can increase the offset.

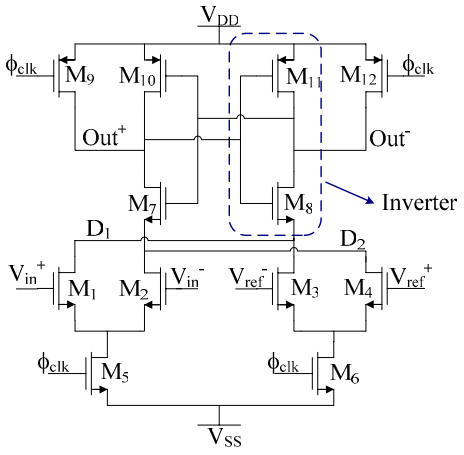

Figure 1. Fully differential typical dynamic comparator

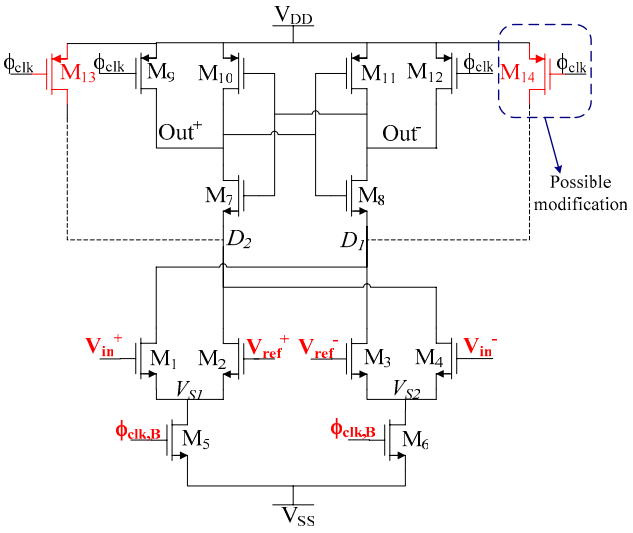

Figure 2. Proposed dynamic comparator

III. SENSITIVITY ANALYSIS

To understand how different variables can affect the offset of a comparator, sensitivity analysis is required. For this all the variables need to be identified. The main variables for a comparator will be widths and lengths, threshold voltages and mobilities of all transistors, input and reference CM voltages, clock signals' high and low voltages along with rise and fall timings, different parasitic node capacitances etc. Robustness of comparator will be defined by small sensitivity to these variables. Common centroid layout techniques for matching critical transistors along with the use of dummy transistors will reduce the mismatches associated with transistors. Hence, the most important, less studied and comparator performance restricting variables will be the parasitic capacitance imbalance between axis symmetric nodes of the comparator. If the comparator is symmetric, also with respect to all non-idealities,

then the comparator offset will be zero. Clock timing errors and CM voltage errors will also contribute to the offset.

Before we define the sensitivity of a comparator with respect to a variable, we need to define the offset of a comparator. The offset of a comparator can be defined by additional differential input signal from the ideal differential input to achieve a desired output, Fig. 3. Sensitivity of the comparator can then be defined as,

$$S_X^{V_{OS}} = \frac{V_{OS}}{\Delta X} \quad (1)$$

where ΔX is the amount of imbalance in the variable. Therefore, the sensitivity is directly proportional to the offset and smaller value of offset will imply lesser sensitivity of the comparator to the respective variable.

IV. Simulation Results

The typical structure, Fig. 1, and the proposed structure, Fig. 2, are designed in TSMC 0.18µ process. Key values used for both structures are listed in Table I and the CM voltages for the inputs and the references are assumed to be at 0V. To show the combined advantages of input reconfiguration and restricted clock, both the structures are simulated (transient) for static offset performance with two different tail current clocks (ϕ_{clk} and $\phi_{clk,B}$). Transient simulations are carried out with minimum differential step size of 0.4mV.

First consider that an additional parasitic capacitance (C_P) is present at the negative output node (OUT^-). Table II lists the approximate simulated offset voltages for two different C_P values. The offset low value in Table II, as well as for other tables, is defined by the maximum additional differential input voltage over differential reference which still results in V_{OUT}^+ to go to V_{SS}, whereas, offset high value is defined by the minimum additional differential input voltage over differential reference needed to make V_{OUT}^+ to go to V_{DD}. Ideally both these values should be same but due to previous decision of the comparator the offset low and high can easily be different. In that case, the region between offset low and high will be an undefined region as the output of the comparator will be function of previous input values. In average sense, offset can also be defined by the average value of offset low and high. For C_P of 2fF, the offset is more than 80mV for the typical differential pair with tail clock of ϕ_{clk}, whereas, it drops to around 30mV for the proposed structure with the same tail current clock and further drops to around 1mV with modified restricted tail clock ($\phi_{clk,B}$). Hence, a factor of at least 80 reduction in offset can be achieved when the proposed structure with restricted clock is used as compared to the typical differential pair structure with tail clock of ϕ_{clk} for output node parasitic imbalance of 2fF case. Table III summarizes the simulated offset values for the case when the additional parasitic capacitance is present at the OUT^- and the internal nodes D_1 and D_2 are reset to V_{DD} when clock is low. In this case, the proposed structure with $\phi_{clk,B}$ has offset less than 0.5mV, whereas, for the typical differential pair with ϕ_{clk} it can be easily more than 40mV. This suggests that resetting D_1 and

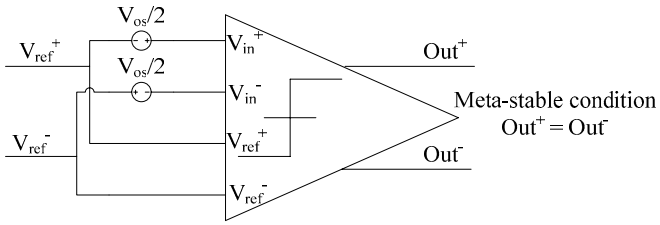

Figure 3. Dynamic comparator offset definition

TABLE I. KEY VALUES USED FOR SIMULATIONS

Power Supply	V_{DD} = 0.9V, V_{SS} = -0.9V
Input transistor sizing	W/L = (6µ / 0.4µ) x 4
Tail current transistor sizing	W/L = (6µ / 0.4µ) x 2
Inverter transistor sizing	PMOS: W/L = (0.7µ / 0.35µ) x 4
	NMOS: W/L = (0.75µ / 0.35µ) x 1
Clocks	Rise and Fall time = 10ps
	Pulse width = 5ns; Period = 10ns
	ϕ_{clk}: High = 0.9V; Low = -0.9V
	$\phi_{clk,B}$: High = -0.3V; Low = -0.9V
Reference	V_{ref}^+ = 187.5mV; V_{ref}^- = -187.5mV
Switches (PMOS)	W/L = 1.5µ / 0.4µ

D_2 to V_{DD} when clock is low can further reduce the offset in the proposed structure and make the structure robust to the parasitic imbalance at the output node.

Similar simulations are performed for the case when there is an additional parasitic capacitance at the internal node D_1. Table IV and V summarizes the simulated offset values for C_P = 2fF and 4fF. For the case where internal nodes D_1 and D_2 are untouched, the proposed structure with $\phi_{clk,B}$ has offset less than 1mV, whereas, for the typical differential structure with ϕ_{clk} is significantly large. If the internal nodes, D_1 and D_2, are pulled to V_{DD} during the phase when clock is low, the typical structure with ϕ_{clk} has around 38mV offset for C_P = 4fF, and the offset drops to 7mV for the propose structure with $\phi_{clk,B}$. In this case, parasitic imbalance at the internal node causes more offset if these internal nodes are to reset to V_{DD}, making the comparator more sensitive to this kind of imbalance. For a comparator with common centroid layout design, this imbalance of the parasitic capacitance can be easily reduced. However, the output nodes will have two gate capacitances, three diffusion capacitances, interconnect capacitances and the capacitance coming from circuitry connected to these nodes. To reduce the capacitive load and the error in it, a cascade of two inverters should be used. Still significant capacitance imbalance at the output nodes can be present. Therefore, resetting the internal nodes D_1 and D_2 can help in reducing the overall comparator offset.

Another source of non-ideality can come from the CM voltage errors. Input signal CM voltage can differ from reference CM voltage due to previous inter-stage gain amplifier in a pipeline ADC or due to mismatches in different components. Table VI summarizes offsets due to input CM voltage error. For the typical structure without D_1 and D_2 reset

to V_{DD}, the offset is expected to be at least twice the CM voltage error as one of the transistors in the differential pair is nearly turned off and only comparison of one input value to the corresponding reference value will be made. Therefore, to reach meta-stable point, the input has to compensate for the CM voltage error first. However, for the proposed structure, small CM voltage error will cause nearly similar percentage change in the current of M_1 and M_4 transistors (and also opposite sign percentage change in M_2 and M_3 transistor currents). As the sum of M_1 and M_3 transistor currents is compared to that of M_2 and M_4, the overall error will be reduced and will result in smaller offset. The last source of error considered here is due to timing error in the clocking scheme. For this it is assumed that the clocks for the switches used to reset OUT^+ and D_2 nodes to V_{DD} are delayed or advanced by 1ps. Table VII lists the offset voltages for this case. From the point of view of CM voltage errors and the timing errors, the proposed structure shows less sensitivity to such errors as compared to the typical differential pair and resetting D_1 and D_2 nodes can further reduce the offset. In both cases, offset can be reduced from tens of milli-volt range for typical differential pair structure to only milli-volt range.

V. CONCLUSIONS

A new dynamic comparator was proposed for high speed high resolution ADC application. In the new design, inputs were reconfigured from the typical structure along with a use of restricted clock for the tail current. Simulation based sensitivity analysis was carried out with respect to imbalance in parasitic capacitances, CM voltage errors and timing errors. The proposed structure shows significantly lower sensitivity to the errors as compared to the typical structure. Reset of the input transistor drain nodes and use of buffers at the output nodes can further reduce the offset. The modifications made to the typical differential pair dynamic comparator can easily reduce the overall offset to only few milli-volts as compared to hundreds of milli-volts.

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TABLE II. COMPARATOR OFFSET DUE TO C_P AT OUT^-

Structure	C_P (fF)	Offset Voltages (Low, High) (mV)	
		Tail current clock: ϕ_{clk}	*Tail current clock: $\phi_{clk,B}$*
Typical Diff. pair	1	(25, 82)	(-205, 221)
	2	(85, 154)	(-202, 237)
Proposed structure	1	(15.2, 15.6)	(-0.8, -0.4)
	2	(31.2, 31.6)	(-1.0, -0.6)

TABLE III. OFFSET DUE TO C_P AT OUT^- WITH D_1 AND D_2 RESET

Structure	C_P (fF)	Offset Voltages (Low, High) (mV)	
		Tail current clock: ϕ_{clk}	*Tail current clock: $\phi_{clk,B}$*
Typical Diff. pair	1	(19, 20.2)	(-25, 32)
	2	(40.4, 41.8)	(-18, 41)
Proposed structure	1	(8.2, 8.6)	(-0.4, 0)
	2	(16.4, 16.8)	(-0.4, 0)

TABLE IV. OFFSET DUE TO C_P AT D_1 NODE

Structure	C_P (fF)	Offset Voltages (Low, High) (mV)	
		Tail current clock: ϕ_{clk}	*Tail current clock: $\phi_{clk,B}$*
Typical Diff. pair	2	(-10, 38)	(-199, 226)
	4	(1, 52)	(-196, 229)
Proposed structure	2	(3.8, 4.2)	(0, 0.4)
	4	(7.6, 8.0)	(0.2, 0.6)

TABLE V. OFFSET DUE TO C_P AT D_1 NODE WITH D_1 AND D_2 RESET

Structure	C_P (fF)	Offset Voltages (Low, High) (mV)	
		Tail current clock: ϕ_{clk}	*Tail current clock: $\phi_{clk,B}$*
Typical Diff. pair	2	(18.8, 20)	(429, -)
	4	(38.8, 40.2)	(>1000, -)
Proposed structure	2	(8.4, 8.8)	(3.2, 3.6)
	4	(16.8, 17.2)	(6.4, 6.8)

TABLE VI. OFFSET DUE TO I/P COMMON MODE VOLTAGE ERRORS

Structure	CM errors (mV)	Offset Voltages (Low, High) (mV)	
		D_1 & D_2 not reset to V_{DD}	*D_1 & D_2 reset to V_{DD}*
Typical with tail clk ϕ_{clk}	10	(-32, 14)	(-11, -9)
	-10	(-12, 35)	(9, 11)
Proposed with tail clk $\phi_{clk,B}$	10	(-2.2, -1.8)	(-1.2, -0.8)
	-10	(1.8, 2.2)	(0.8, 1.2)

TABLE VII. OFFSET DUE TO CLOCK TIMING ERRORS

Structure	Delay (ps)	Offset Voltages (Low, High) (mV)	
		D_1 & D_2 not reset to V_{DD}	*D_1 & D_2 reset to V_{DD}*
Typical with tail clk ϕ_{clk}	1	(-17, 29)	(0, 1.2)
	-1	(-26, 19)	(-1.2, 0)
Proposed with tail clk $\phi_{clk,B}$	1	(0.6, 1)	(0, 0.4)
	-1	(-1, -0.6)	(-0.4, 0)