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A new HVDC grid test system for HVDC grid dynamics and protection studies in EMT-type software

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Keywords: electromagnetic transient simulation, HVDC grid, power system fault, power system protection, test system

Abstract

This paper proposes a new HVDC grid test system for electromagnetic transient analysis, suitable for HVDC power system studies ranging from protection to dynamic studies investigating converter behaviour and interactions. In the recent past research interest in HVDC grids has increased, leading to a multitude of studies concerning dc power flow and optimal power flow, dynamics and HVDC grid protection. However, each of these studies makes use of different grid topologies, configurations and transmission line parameters. In this paper, a standard HVDC grid test system is proposed and an implementation in EMT-type software is provided. The implementation in EMT-type software makes use of a frequency dependent cable model, continuous converter model and a reduced dc breaker model. By means of a protection study, the effectiveness and computational efficiency of the proposed HVDC grid test system is demonstrated. The model with its parameters will be made publicly available.

1 Introduction

Voltage source converter-based high-voltage dc (VSC-HVDC) grids are considered as the next step for connection of remote renewable energy sources to the main ac grid. Moreover, a HVDC grid is considered as upgrade for the existing high voltage ac grid [1, 2]. Much research is currently being undertaken regarding several challenges such as optimal power flow in HVDC grids, HVDC grid control and protection.

For ac power system studies, it is commonly accepted to use standard test networks such as the IEEE N-bus systems [3], the two area system of [4] or the nine-bus system of [5]. For dc power system studies, a variety of HVDC grids has recently been used in the literature. Together with grid topology, the system parameters such as transmission line lengths, dc voltage and converter ratings also differ considerably. As these choices affect the outcome of the research, comparison of these different studies is not straightforward. Only one HVDC grid test system has until now been proposed [6]. The test system is subdivided in three independent dc subsystems. However, even the meshed subsystem on its own contains seven converters and ten lines, making electromagnetic transient simulations cumbersome.

In this paper, a HVDC grid test system is proposed, suitable for dc power system studies in electromagnetic transient programs. An implementation of the HVDC grid test system is made in PSCAD and is publicly available [7, 10]. In contrast with [6], the test system consists of only four dc nodes, which allows implementation in educational versions of commercially available EMT-type software. The system accommodates two offshore wind farms, connected to the main grid by means of a four-terminal meshed dc system. For the HVDC grid test system, standard parameters based on currently existing technology are proposed. Furthermore, the test system, including a continuous modular multilevel converter (MMC) model [8, 9] and a frequency-dependent cable model is implemented in EMT-type software, namely PSCAD [7, 10]. This model can be used for electromagnetic transient studies of the dc power system, such as dc fault transient and protection studies or grid and converter dynamic studies. Furthermore, the implementation of the HVDC grid test system is flexible in that it allows adaptation of each component to study different phenomena. To demonstrate the HVDC grid test system, a case study regarding HVDC grid protection is performed. For this case study, a basic protection algorithm is developed. The protection algorithm provides high-speed selective protection based on traveling waves.

The paper is structured as follows. Section 2 describes the grid layout and parameters for the HVDC grid test system. Next, Section 3 introduces the components of the HVDC grid test system for implementation in PSCAD. In Section 4, the basic protection algorithm is developed and results from fault studies using the HVDC test system are presented.

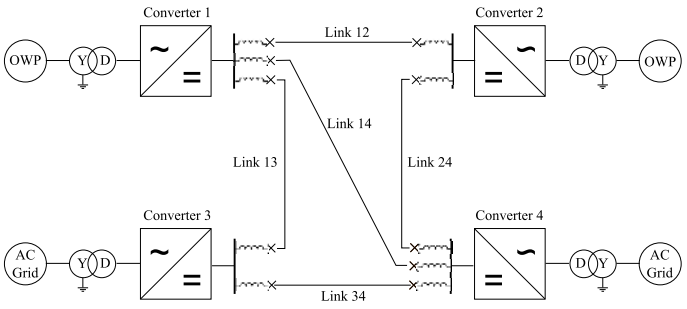

Fig. 1: Proposed four-terminal HVDC grid test system.

	Conv. 1,2,3	Conv. 4	
Rated power	900	1200	[MVA]
Ac grid voltage	400	400	[kV]
Ac converter voltage	380	380	[kV]
Transformer u_{k}	0.15	0.15	[pu]
Ac grid reactance X_{ac}	17.7	13.4	[Ω]
Ac grid resistance R_{ac}	1.77	1.34	[Ω]
Arm capacitance C_{arm}	29.3	39	[μF]
Arm reactor L_{arm}	84.8	63.6	[mH]
Arm resistance R_{arm}	0.885	0.67	[Ω]
Bus filter reactor	10	10	[mH]

Table 1: Converter and grid parameters.

2 HVDC grid test system layout

This section presents the HVDC grid test system layout, parameters and control.

Fig. 1 shows the HVDC grid test system proposed in this paper. The HVDC grid consists of two converters (Converter 1 and 2), connected to offshore ac wind farms, that feed two onshore converters (Converter 3 and 4) connected to the mainland ac grid. The mainland ac grid is modelled by two independent ac voltage sources. The system configuration is symmetric monopolar with a dc voltage of $\pm$ 320 kV. The ac grid and HVDC converter parameters are shown in Table 1.

The HVDC grid consists of two links of 200 km length (links 13 and 14), one link of 150 km (link 24) and two links of 100 km (links 12 and 34). A bus filter reactor of 10 mH is connected in series with the converter and the dc bus. Dc breakers are included at the end of each transmission line. The series reactor for the dc breakers has a value of 100 mH, similar as in [11].

The high-level control system for each MMC consists of two outer controllers and separate inner current controllers for positive and negative sequence current control. The outer controllers for converter 1 and 2 are set to control the active power, while converter 3 and 4 control the direct voltage. For direct voltage control, droop control is implemented to increase the reliability of the HVDC grid. Additionally, all converters

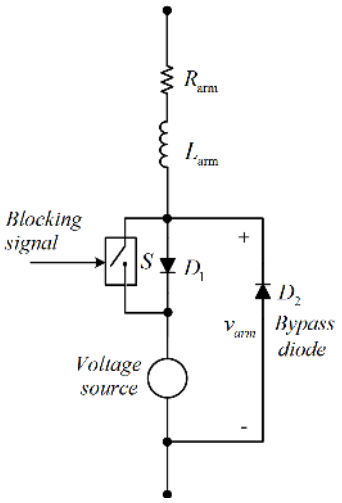

Fig. 2: Equivalent branch model of a converter arm.

are (also) set to control the reactive power to a given reference. The outer controllers provide current references in the dq-reference frame to the positive sequence inner controller. The negative sequence current controller is implemented to suppress second order harmonics in the dc-side current and voltage, and to keep the ac-side current balanced during asymmetrical fault conditions. The current references for the negative sequence inner controller are set to zero. The inner current controllers give desired phase voltage references in the dq-reference frame, independently for the positive and negative sequences [12].

3 HVDC Grid Components

This section describes the converter and breaker model included in the HVDC grid test system.

3.1 Converter

The MMC is used as the converter topology in the proposed test grid model as it offers additional advantages over conventional VSCs [2].

3.1.1 Converter model

The HVDC grid test system is simulated using the continuous MMC model [8, 9]. The model is based on the equivalent branch model of an arm of the MMC as shown in Fig. 2. The branch is characterised by the arm resistance, the arm inductance and an ideal voltage source. The ideal voltage source represents the submodule capacitor chain in the arm of the MMC. The voltage of the source represents the instantaneous voltage inserted by the submodules in the arm. The continuous model is also capable of describing the blocked state of the MMC. This feature enables the model to accurately describe the performance of the MMC at start-up and during fault conditions.

3.1.2 Converter Control

The internal control of the MMC is based on the open-loop approach using estimation of stored energies [13]. Unlike feedback control which measures the total capacitor voltages in the arms, open-loop control estimates these voltages using the desired alternating voltage and the measured alternating current. It is assumed that a voltage sharing system is provided to distribute the total arm voltage in each arm evenly between all submodules in the arm. The open-loop controller provides six insertion indices (n_{arm}) governing each arm in the MMC. These are calculated based on the ratio between the desired arm voltage and the total capacitor voltage in the arm.

3.1.3 Converter Protection

As the converter IGBTs and diodes cannot withstand large overcurrents, protective measures must be taken in order to prevent converter damage in case of short circuits. Two types of converter protection are considered in this paper.

First, overcurrent protection prevents damage to IGBTs by keeping the current within the safe operating area (SOA). The maximum instantaneous limit for the IGBT current, I_{CM}, is typically twice the maximum continuous IGBT current I_C. Therefore, IGBTs are blocked for protection whenever the current exceeds 0.8 I_{CM}. When IGBTs are blocked, the current is diverted to the converter diodes or protective thyristors.

Second, an undervoltage criterion is used to trip the converter IGBTs. Controllability of the converter is lost in case of too low arm voltages. In case of such events, the IGBTS of the converter are blocked.

3.2 Cables

For the links, 320 kV XLPE insulated cables suitable for offshore applications are used. The cable consists of a core conductor, a lead sheath and steel armor, separated by XLPE insulation layers. The parameters for the cable geometry and materials are enlisted in Table 2, based on several sources [14, 15, 16]. At the inner insulation layer, semiconductor screens of 1.7 mm and 1.9 mm are applied, incorporated in the outer radius of the XLPE insulation in Table 2. The ground return is modelled with a constant resistivity of 1 $\Omega \cdot$ m, typical for wet soil [17]. The surge impedance of the cable is 33.73 Ω and the propagation velocity is 183.5 km/ms.

The cables are modelled using the frequency dependent (phase) model available in PSCAD. This is a distributed parameter model which is able to accurately represent transient behaviour. The armour and sheath are assumed to be perfectly grounded, hence they can be eliminated by Kron reduction. This implies that the voltages in armour and sheath remain limited, which is a realistic assumption for submarine HVDC power cables [17, 18].

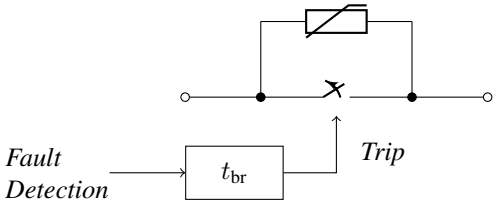

Fig. 3: Dc breaker model.

Table 2: Cable parameters

	Outer radius [mm]	ρ [Ωm]	ϵ_{rel} [-]	μ_{rel} [-]
Core	19.5	1.7e-8	-	1
Insulation	48.7	-	2.3	1
Sheath	51.7	2.2e-7	-	1
Insulation	54.7	-	2.3	1
Armour	58.7	1.8e-7	-	10
Insulation	63.7	-	2.3	1

3.3 Dc Breaker

The grid model offers the possibility to insert a dc breaker at the end of each transmission line. The breaker model proposed in this paper represents the basic functionality of a dc breaker, unbound to a specific implementation. Basically, a dc breaker inserts a countervoltage that drives the fault current to zero and absorbs the energy that is present in the system after a fault. The countervoltage is inserted after a certain time delay, depending on breaker technology. The energy absorption is typically performed by a parallel surge arrester, which also determines the maximum countervoltage. Due to the time delay and the high rate of rise of the dc fault current, a series reactor is typically provided to limit the rate of rise of the current [19].

To incorporate these functions, the breaker is modelled as a switch in parallel with a surge arrester. The surge arrester is rated at 150% of the nominal pole-to-ground voltage. This implies a co-operation of breakers at both poles to clear pole-to-pole faults. The delay caused by the mechanical breaker is incorporated by a time delay between fault detection and opening of the switch (Fig. 3). This time delay t_{br} can be set to several milliseconds to simulate a hybrid HVDC breaker or tens of milliseconds to simulate a mechanical dc breaker.

4 Case study

This section demonstrates the proposed HVDC grid test system by a protection study in PSCAD. First, a basic protection method for cable protection based on traveling waves is developed. Second, several short circuit faults are applied in the system and the results are discussed.

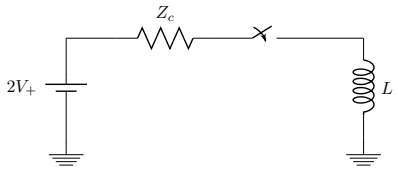

Fig. 4: Simplified scheme for reflection of a wave by an inductor.

4.1 Protection method

The HVDC grid test system allows to include a protection algorithm for the HVDC grid test system. This paper proposes a first implementation based on protection with fast dc breakers. Due to the high rate of rise of the fault current and the limited maximum interruptible current by dc breakers, protection must be organized on a timescale of milliseconds. As at this timescale, traveling wave behavior is dominating the transient [20], fault detection must be based on traveling wave concepts.

The proposed detection method for discriminating the faulted dc link is based on the reflection of the voltage wave at the series inductors of the breakers. For a transmission line terminated by a large inductor, the simplified scheme of Fig. 4 can be used to determine the reflection of a wave [21]. In this scheme, the transmission line is represented by a Thévenin equivalent with amplitude twice the value of the incoming voltage wave and resistance the characteristic impedance Z_c. The solution for the inductor current and voltage is

$$\begin{aligned} i_L =& \frac{2V_+}{Z_c}(1 - e^{-t/(L/Z_c)}) \\ v_L =& 2V_+ e^{-t/(L/Z_c)}. \end{aligned} \tag{1}$$

This indicates that, for a large inductor, the current through the inductor is at first zero and the voltage over the inductor twice the value of the incoming wave.

Solid faults create a voltage wave with an amplitude of the dc voltage and a negative sign. The voltage polarity thus changes when an incoming wave is reflected at the inductor. Therefore, a negative voltage indicates that a fault has occured on a cable. To account for the fact that the voltage only drops to zero in case of a fault directly at the breaker, a threshold voltage larger than zero is chosen. The suitability of this criterion depends on the location of the fault, fault impedance and on the size of the inductor. This fault detection method works for low impedance faults and cables with limited lengths.

4.2 Results

First, the continuous converter model is compared against a more detailed model to validate the continuous model for fault transient simulations. Second, the results for the HVDC grid protection study are discussed.

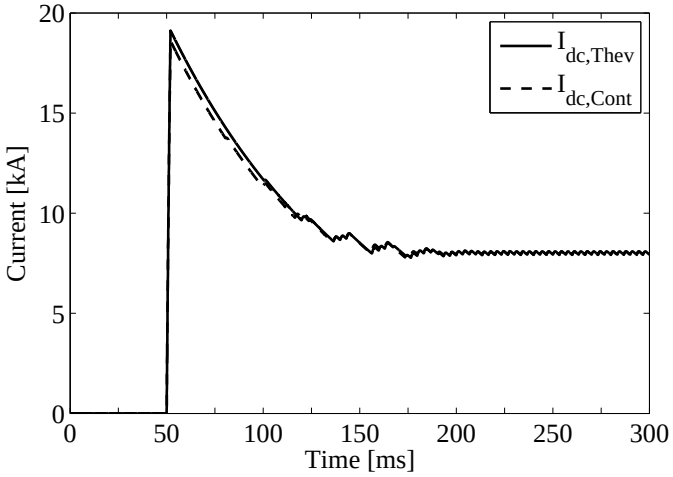

Fig. 5: Dc fault current for pole-to-pole fault at converter terminals for continuous model and Thévenin equivalent converter model.

4.3 Comparison to another equivalent converter model

In this section, the continuous converter model with blocking capability is compared against an equivalent converter model representing each arm as Thévenin equivalent [22] (further referred to Thévenin equivalent model) for a pole-to-pole fault directly at the converter terminals. This equivalent model gives the same results as a switching model with linear switches. The Thévenin equivalent model has been extended in a similar way as [8] to include fault blocking capability.

The dc fault current for a fault occurring at 50 ms is plotted in Fig. 5. For easy comparison of the fault currents, blocking of IGBTs is assumed to occur 2 ms after fault inception. The fault current for both converter models shows a high degree of similarity. The Thévenin equivalent model reaches a higher maximum current than the continuous model, due to different initial conditions and controls (different capacitor voltages and inserted number of submodules). At 52 ms, the converter IGBTs are blocked and the energy built up in the arm reactors is released. Both models show the same decaying behaviour, however, the Thévenin equivalent model has a slightly higher current due to the higher maximum current. After some time, the fault currents of both converter models converge to a value around 8 kA pulsating at 6 times the nominal frequency, indicating uncontrolled rectifier behaviour of the blocked converter.

The continuous model with blocking capability is therefore suitable for simulating dc fault transients, while it reduces computational complexity compared to more detailed models.

4.4 Dc Short Circuit Faults

This section describes the results of the simulations for a dc fault in the grid. The following faults are consecutively treated:

1. Pole-to-pole fault in middle of link 13.

2. Pole-to-ground fault in middle of link 13.
3. Pole-to-pole fault at converter 1 side of link 13.
4. Pole-to-ground fault at converter 1 side of link 13.

The fault represents a solid fault, modelled with a small resistor of 0.01 Ω.

4.4.1 Fault in middle of link 13

Fig. 6 shows the currents at the positive pole and the pole-to-pole voltages after a pole-to-pole fault in the middle of link 13. The pole-to-pole fault occurs at 50 ms at a distance of 100 km away from the converter. The voltage drops to almost the negative of the nominal value, due to reflection of the voltage wave at the inductors. Using the wave propagation speed, it can be calculated that the first wave reaches the pole after 0.54 ms and that the time between successive reflections of the wave is 1.08 ms, being twice the time for the wave to travel over 100 km.

The maximum current in the faulted pole is 4.8 kA. The current is mainly delivered by the converter, whereas the infeed of the neighboring cables is limited due to the series inductors. The converter IGBTs were not blocked as the maximum arm current did not exceed the overcurrent threshold. The fastest rate-of-rise of the fault current is 4 kA/ms. The voltage on the faulted link is almost fully inversed, while the voltages at the bus and other links are much less affected. Therefore, it is possible to identify the faulted link only from the voltage. After opening of the breaker, it takes about 5 ms to drive the fault current to zero. The voltage inserted by the surge arresters increases the pole-to-ground voltage by 480 kV. This can be seen in the voltage at the moment of interruption; the voltage reaches at maximum 672 kV.

In Fig. 7, the currents and voltages at bus 1 for the fault are shown for a longer time period. It can be noted that resonances occur after fault clearing. These resonances die out about 100 ms after the fault. From inspection, the resonances on link 14 and bus 1 seem to consist of more than one frequency.

Fig. 8 shows the positive pole currents and voltages at bus 1 for a pole-to-ground fault in the middle of link 13. Comparing with Fig. 6, the converter contribution and contributions of each link are slightly less than in the case of pole-to-pole faults. Therefore, the maximum current in the positive pole of the faulted link is 4.18 kA. However, in the pole-to-ground voltages, a similar travelling wave behaviour can be noted. Therefore, by considering pole-to-ground voltages, the faulted pole can be detected and cleared by opening the breakers at both ends.

4.4.2 Fault at converter 1 side of link 13

In Fig. 9, the positive pole currents and positive pole-to-ground voltages at bus 1 are shown for a pole-to-pole fault at the converter 1 side of link 13. The pole-to-ground voltage of the faulted link is clamped to zero by the fault. Travelling wave behaviour in the currents and voltages is absent due to the fault occurence direct at the begining of the link.

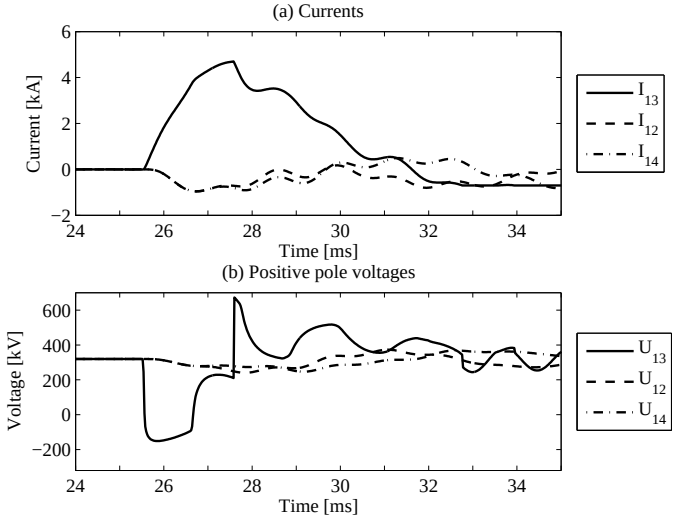

Fig. 6: Positive pole currents and pole-to-ground voltages at the bus 1 after a pole-to-pole fault in the middle of link 13.

Again, the voltages on the other links and on the bus are much less affected, making it possible to detect the faulted link using only the voltage threshold. The fault is almost immediately detected and cleared after 6.5 ms. The maximum fault current is 5.14 kA. The maximum voltage after fault breaking is 465 kV, caused by the surge arrester. For the breakers at bus 3, this represents the worst case scenario for fault detection. However, even with attenuation of the wave over the line, the reflection of the wave is sufficient to discriminate the faulted link.

Fig. 10 shows the positive pole currents and pole-to-ground voltages at bus 1 for a pole-to-ground fault at the converter 1 side of link 13. Similar conclusions as in the previous section can be drawn comparing the pole-to-pole fault with the pole-to-ground fault.

5 Conclusion

This paper proposes a generic four-terminal HVDC grid test system suitable for electromagnetic transient analysis of HVDC power systems. The HVDC test system can serve as standard HVDC grid test system, enabling comparison of research results for a wide variety of studies. Together with the grid layout, parameters have been proposed as to present a realistic test scenario for dc power system studies.

An implementation of the HVDC grid test system in the educational version of EMT-type software and a simple protection scheme based on travelling waves have been presented. For the cables, a frequency dependent distributed parameter model is used. The converter model that is implemented is the continuous model with blocking capability. The breaker model

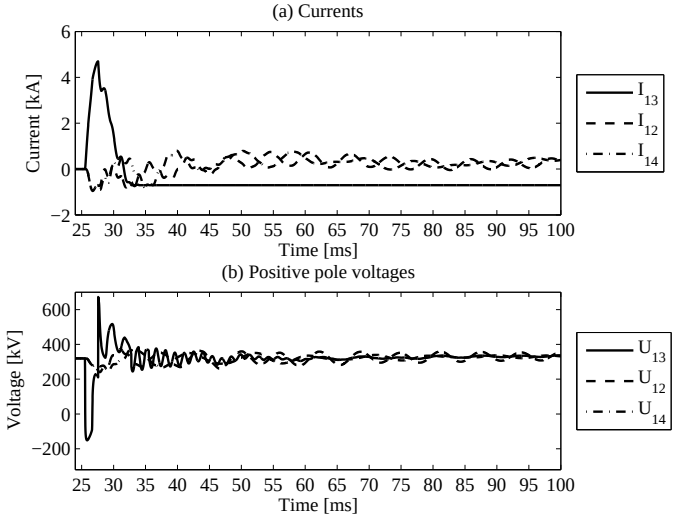

Fig. 7: Positive pole currents and pole-to-ground voltages at the bus 1 after a pole-to-pole fault in the middle of link 13.

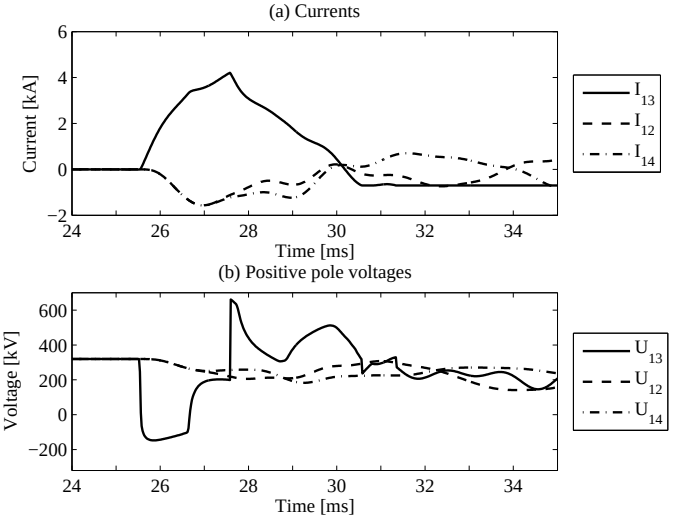

Fig. 8: Positive pole currents and pole-to-ground voltages at the bus 1 after a pole-to-ground fault in the middle of link 13.

provides the basic functionality, which allows to focus on the interaction of the breaker with the dc power system.

The results of the transient study demonstrate the usability of the HVDC grid test system for HVDC grid protection studies. Because of the frequency dependent distributed parameters cable model, the traveling wave behaviour during the fault transient is accurately captured. Furthermore, the continuous model gives a correct response towards fault transients, compared to a more detailed model. The study hence shows that the HVDC grid test system is well suited for electromagnetic transient studies in a limited version of commercially available EMT-type software.

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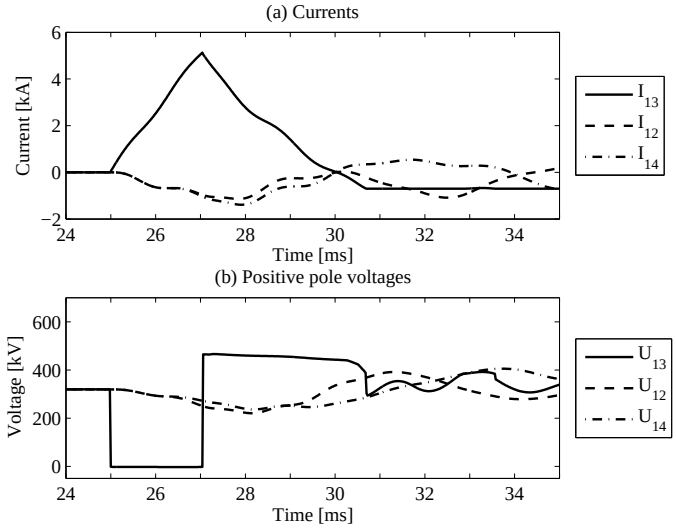

Fig. 9: Positive pole currents and pole-to-ground voltages at the bus 1 after a pole-to-ground fault at converter 1 side of link 13.

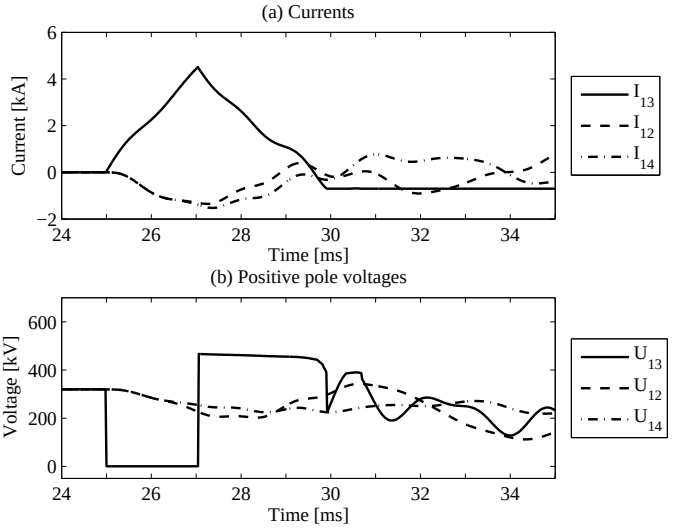

Fig. 10: Positive pole currents and pole-to-ground voltages at the bus 1 after a pole-to-ground fault at converter 1 side of link 13.

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