A New Low-Frequency State Model of a Three-Phase Three-Switch Three-Level Fixed-Frequency PWM Rectifier

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ABSTRACT

This paper presents a new dynamic model of a three-phase, three-switch, three-level, fixed-frequency Pulse-Width-Modulated (PWM) rectifier. The modeling approach uses the state-space averaging technique in continuous current mode. The averaging process is applied on two time intervals: the switching period for average current evaluation, and the mains period for average voltage computation. A basic mathematical model of the converter is first established. A simplified time-invariant model is then deduced using rotating Park transformation. The steady-state regime is analyzed on the basis of the obtained model, and converter design criteria are consequently discussed. Numerical simulations are carried out in order to demonstrate the effectiveness of the proposed modeling approach.

I – INTRODUCTION

AC-to-DC three-phase converters are increasingly required to provide high input power factor, low line current distortion, fixed output voltage and robustness to load and utility voltage unbalances. Several topologies that satisfy these requirements have been proposed recently [1]. Among these structures, the three-switch, three-level AC-to-DC converter, known as the Vienna rectifier, is characterized by a low number of high-frequency switches, high efficiency, low design costs and low voltage stresses, which make it suitable for high or medium power applications [2]. Besides its topological advantages, this converter is also known for its low control complexity and its low sensing effort regarding the control system design and implementation [3].

In this paper, a new mathematical model of a three-phase, three-switch, three-level, fixed-frequency Pulse-Width-modulated (PWM) rectifier, operating in continuous current mode, is developed from a control design perspective. The model is elaborated using the state-space averaging technique commonly used in PWM DC-DC converters modeling problems [4]. This modeling approach is so far valid as long as the input and state variables of the converter vary slowly in time. Other modeling techniques have already been proposed in the literature, such that the averaging technique that is based on equivalent circuit manipulation [4], and the Fourier analysis based modeling approach [5]. Although their differences, they all yields at the same low-frequency representation of the converter.

The basic model firstly obtained for the converter is a nonlinear fifth-order time-varying system, and the elaboration and implementation of a corresponding suitable control law seem highly difficult. Thus, in order to simplify the eventual control design procedure, a fourth-order time-invariant model is elaborated by applying to the former one two transformations: a three-axis/two-axis frame transformation [5], known as Park transformation, and an input vector nonlinear transformation. The effectiveness of the proposed modeling approach is highlighted through numerical simulation using the Power System Blockset tool of Matlab/Simulink.

This paper is divided into five sections. In section II, a brief description of the converter topology and operation is presented. In section III, the reduced nonlinear time-invariant low-frequency model of the converter is elaborated. All the corresponding theoretical developments are indicated, including the three-axis/two-axis frame transformation and the proposed input vector nonlinear transformation. Based on the obtained model, the steady-state operating mode of the converter is analyzed in section IV. Design criteria allowing a suitable choice of the converter parameters, namely the reactive elements, are then enumerated in the section V. Finally, the numerical results showing the effectiveness of the proposed modeling approach are presented in section VI.

II – CONVERTER TOPOLOGY AND OPERATING MODE

The converter topology is presented in Fig. 1. It consists of three single-switch legs associated to each phase. Q_1 , Q_2 and Q_3 are four-quadrants switches. They are controlled in order to ensure line current shaping at the input, DC voltage regulation and middle point stabilization at the output. From an operational view, the converter can be seen as an association of three identical bi-directional boost converters, as the one presented in Fig. 2 for phase 1. Referring to this figure, we may write the following equation for phase 1:

$$v_{s,1n} = L\frac{di_{s,1}}{dt} + v_{M,n} + v_{AM} \tag{1}$$

where $v_{s,1n}$ is the phase-to-neutral voltage, $i_{s,1}$ the phase current, $v_{M,n}$ the middle point voltage with respect to the mains neutral, and v_{AM} the switch voltage defined as:

$$v_{AM} = \begin{cases} 0 & \text{if } Q_1 \text{ is turned-on} \\ v_{0,h} & \text{if } Q_1 \text{ is turned-off and } i_{s,1} > 0 \\ -v_{0,l} & \text{if } Q_1 \text{ is turned-off and } i_{s,1} < 0 \end{cases} \tag{2}$$

$v_{0,h}$ and $v_{0,l}$ being respectively the upper and lower output voltages. Hence, we may express v_{AM} as follows:

$$v_{AM} = \left[\frac{v_{0,h}+v_{0,l}}{2}\operatorname{sgn}(i_{s,1}) + \frac{v_{0,h}-v_{0,l}}{2}\right]\cdot(1-s_1) \tag{3}$$

where sgn is the signum function, and s_1 the switching function defined as:

$$s_1 = \begin{cases} 0 & \text{if } Q_1 \text{ is turned-off} \\ 1 & \text{if } Q_1 \text{ is turned-on} \end{cases} \tag{4}$$

In the same way, we can write for the other two phases the following equations:

$$v_{s,2n} = L\frac{di_{s,2}}{dt} + v_{M,n} + v_{BM} \tag{5}$$

and:

$$v_{s,3n} = L\frac{di_{s,3}}{dt} + v_{M,n} + v_{CM} \tag{6}$$

where:

$$v_{BM} = \left[\frac{v_{0,h}+v_{0,l}}{2}\operatorname{sgn}(i_{s,2}) + \frac{v_{0,h}-v_{0,l}}{2}\right]\cdot(1-s_2) \tag{7}$$

and:

$$v_{CM} = \left[\frac{v_{0,h}+v_{0,l}}{2}\operatorname{sgn}(i_{s,3}) + \frac{v_{0,h}-v_{0,l}}{2}\right]\cdot(1-s_3) \tag{8}$$

s_2 and s_3 being the switching functions corresponding to Q_2 and Q_3 respectively.

In the nominal steady-state regime with a balanced load, $v_{0,h}$ and $v_{0,l}$ are equal to $v_0/2$, where $v_0 = v_{0,h} + v_{0,l}$ is the overall output voltage. We may thus rewrite equations (3), (7) and (8) as follows:

$$v_{AM} \cong \frac{v_0}{2}\operatorname{sgn}(i_{s,1})(1-s_1) \tag{9.a}$$

$$v_{BM} \cong \frac{v_0}{2}\operatorname{sgn}(i_{s,2})(1-s_2) \tag{9.b}$$

$$v_{CM} \cong \frac{v_0}{2}\operatorname{sgn}(i_{s,3})(1-s_3) \tag{9.c}$$

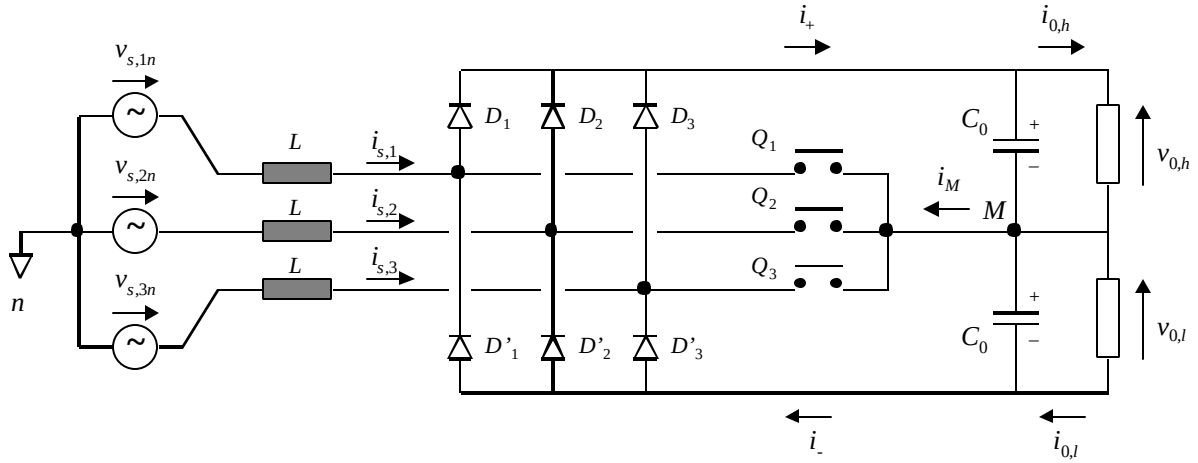

Fig. 1. Three-phase, three-switch, three-level rectifier

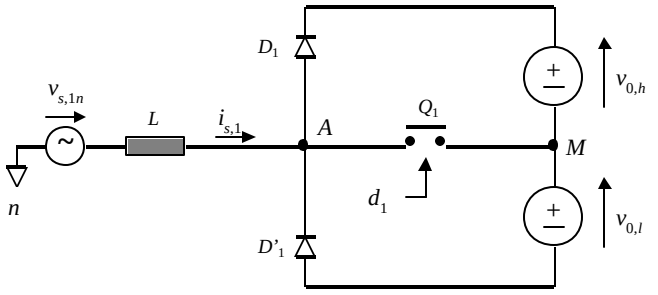

Fig. 2. Single-phase equivalent circuit

Furthermore, assuming that the utility voltages are balanced sine waves, and that the neutral is disconnected, it follows:

$$v_{s,1n}(t)+v_{s,2n}(t)+v_{s,3n}(t)=0 \quad , \quad \forall\, t \tag{10}$$

and:

$$i_{s,1}(t)+i_{s,2}(t)+i_{s,3}(t)=0 \quad , \quad \forall\, t \tag{11}$$

Using equalities (10) and (11) in equations (1), (5) and (6) yields:

$$v_{M,n}=-\frac{1}{3}\left(v_{AM}+v_{BM}+v_{CM}\right) \tag{12}$$

which can be rewritten using expressions (9):

$$v_{M,n}=-\frac{v_0}{6}\sum_{k=1}^{3}\mathrm{sgn}\left(i_{s,k}\right)\left(1-s_k\right) \tag{13}$$

The values of $v_{M,n}$ are given in Tab. 1 with respect to the switching states s_k and the sign of line currents $i_{s,k}$, $k \in \{1, 2, 3\}$. Thus, the value of $v_{M,n}$ depends only on the output voltage v_0. Referring to equations (1), (5) and (6), it is noticed that, in order to ensure line current waveshaping, the following two conditions must be always respected:

$$\left|v_{s,kn}(t)\right| > \pm v_{M,n}(t) \quad , \quad \forall\, t \text{ and } \forall\, k \in \{1,2,3\} \tag{14}$$

$$\left|v_{s,kn}(t)\right| < \pm\left(v_{M,n}+\frac{v_0}{2}\right), \quad \forall\, t \text{ and } \forall\, k \in \{1,2,3\} \tag{15}$$

Conditions (14) and (15) limit the choice of the output voltage value in the range:

$$\frac{3}{2}V_S\sqrt{6} < v_0 < 3V_S\sqrt{6} \tag{16}$$

i.e., between $3.68V_S$ and $7.34V_S$, where V_S is the RMS-value of the phase-to-neutral mains voltage.

III – STATE-SPACE AVERAGE MODELING OF THE CONVERTER

3.1. Basic model

The modeling approach applied to the converter in Fig. 1 is based on the state-space averaging technique [4]. In this method, all variables are averaged on a sampling period T_S. Including equations (3), (7), (8) and (12) in the system equations (1), (5) and (6), the equivalent average model of the converter, viewed on the AC side, is as follows:

$$\begin{bmatrix} v_{s,1n} \\ v_{s,2n} \\ v_{s,3n} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{s,1} \\ i_{s,2} \\ i_{s,3} \end{bmatrix} + \mathbf{G}\left(\frac{v_0}{2}\mathbf{SGN}+\frac{\Delta v_0}{2}\mathbf{I_3}\right)\begin{bmatrix} 1\text{-}d_1 \\ 1\text{-}d_2 \\ 1\text{-}d_3 \end{bmatrix} \tag{17}$$

where:

$$\mathbf{G}=\begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix}$$

$$\mathbf{SGN}=\begin{bmatrix} \mathrm{sgn}(i_{s,1}) & 0 & 0 \\ 0 & \mathrm{sgn}(i_{s,2}) & 0 \\ 0 & 0 & \mathrm{sgn}(i_{s,3}) \end{bmatrix}$$

$\Delta v_0 = v_{0,h} - v_{0,l}$, and $\mathbf{I_3}$ is the third-order identity matrix. d_1, d_2 and d_3 are the duty cycles of switches Q_1, Q_2 and Q_3 respectively. Note that system (17) is a time-varying model that depends on the sign of the line currents $i_{s,1}$, $i_{s,2}$ and $i_{s,3}$.

	Switching functions s_1, s_2 and s_3							
Conditions	111	110	101	011	100	001	010	000
$i_{s,1}>0$, $i_{s,2}<0$, $i_{s,3}>0$	0	$-v_0/6$	$v_0/6$	$-v_0/6$	0	0	$-v_0/3$	$-v_0/6$
$i_{s,1}>0$, $i_{s,2}<0$, $i_{s,3}<0$	0	$v_0/6$	$v_0/6$	$-v_0/6$	$v_0/3$	0	0	$v_0/6$
$i_{s,1}>0$, $i_{s,2}>0$, $i_{s,3}<0$	0	$v_0/6$	$-v_0/6$	$-v_0/6$	0	$-v_0/3$	0	$-v_0/6$
$i_{s,1}<0$, $i_{s,2}>0$, $i_{s,3}<0$	0	$v_0/6$	$-v_0/6$	$v_0/6$	0	0	$v_0/3$	$v_0/6$
$i_{s,1}<0$, $i_{s,2}>0$, $i_{s,3}>0$	0	$-v_0/6$	$-v_0/6$	$v_0/6$	$-v_0/3$	0	0	$-v_0/6$
$i_{s,1}<0$, $i_{s,2}<0$, $i_{s,3}>0$	0	$-v_0/6$	$v_0/6$	$v_0/6$	0	$v_0/3$	0	$v_0/6$

Tab. 1. Values of $v_{M,n}$ with respect to the switching states and the sign of line currents

Therefore, it is not suitable for a stationary control design process. In order to overcome this drawback, the following input transformation is proposed:

$$d'_k = (1-d_k)\left[\operatorname{sgn}(i_{s,k}) + \frac{\Delta v_0}{v_0}\right] \quad , \quad \forall\, k \in \{1,2,3\} \qquad (18)$$

Adding equation (18) to equation (17) gives:

$$\mathbf{v_s} = L\frac{d\,\mathbf{i_s}}{dt} + \frac{v_0}{2}\,\mathbf{G}\,\mathbf{d'} \qquad (19)$$

where $\mathbf{v_s} = [v_{s,1n}\ ,\ v_{s,2n}\ ,\ v_{s,3n}]^T$ is the input voltage vector, $\mathbf{i_s} = [i_{s,1}\ ,\ i_{s,2}\ ,\ i_{s,3}]^T$ the input current vector and $\mathbf{d'} = [d'_1\ ,\ d'_2\ ,\ d'_3]^T$ the new control vector.
Furthermore, at the load level, the average model of the converter is viewed as:

$$C_0\frac{d\,v_{0,h}}{dt} + i_{0,h} = i_+ = \frac{1}{2}\sum_{k=1}^{3}(1-d_k)\,i_{s,k}\left[1+\operatorname{sgn}(i_{s,k})\right] \qquad (20.a)$$

$$C_0\frac{d\,v_{0,l}}{dt} + i_{0,l} = i_- = -\frac{1}{2}\sum_{k=1}^{3}(1-d_k)\,i_{s,k}\left[1-\operatorname{sgn}(i_{s,k})\right] \qquad (20.b)$$

where $i_{0,h}$ and $i_{0,l}$ are the upper and lower output currents, i_+ and i_- the DC side currents of the diode bridge. Introducing the overall output voltage v_0, the output voltage unbalance Δv_0 and transformation (18) into equations (20) yields:

$$C_0\frac{d\,v_0}{dt} + i_{0,h} + i_{0,l} \cong \sum_{k=1}^{3} d'_k\,i_{s,k}\left[1-\frac{\Delta v_0}{v_0}\operatorname{sgn}(i_{s,k})\right] \qquad (21.a)$$

$$C_0\frac{d\,(\Delta v_0)}{dt} + i_{0,h} - i_{0,l} \cong \sum_{k=1}^{3} d'_k\,i_{s,k}\left[\operatorname{sgn}(i_{s,k}) - \frac{\Delta v_0}{v_0}\right] \qquad (21.b)$$

In the derivation of equations (21), it was assumed that $\Delta v_0/v_0 << 1$. Equations (19) and (21) represent the basic low-frequency model of the converter in the stationary frame. Although equation (19) is time-invariant, the sub-system (21) is not. Nevertheless, knowing that the output voltages variations are relatively slow with respect to the mains frequency, it seems more convenient, from a control design perspective, to consider their average on a mains period T_0 instead of the one computed on a sampling period T_S. Furthermore, the basic model can be significantly reduced by applying Park's transformation, as discussed in the next sub-section.

3.2. Frame transformation

The model defined by equations (19) and (21) can be expressed in a new rotating frame using Park's transformation. The Park's matrix is defined as [5]:

$$\mathbf{K} = \frac{2}{3}\begin{bmatrix} \sin(w_0 t) & \sin(w_0 t - 2p/3) & \sin(w_0 t - 4p/3) \\ \cos(w_0 t) & \cos(w_0 t - 2p/3) & \cos(w_0 t - 4p/3) \\ 3/2 & 3/2 & 3/2 \end{bmatrix} \qquad (22)$$

where w_0 is the mains angular frequency. Defining the new vectors $\mathbf{v_s}^r$, $\mathbf{i_s}^r$ and $\mathbf{d'}^r$ as follows:

$$\mathbf{v_s^r} \overset{\Delta}{=} \begin{bmatrix} v_{s,d} & v_{s,q} & v_{s,0} \end{bmatrix}^T = \mathbf{K}\,\mathbf{v_s} \qquad (23.a)$$

$$\mathbf{i_s^r} \overset{\Delta}{=} \begin{bmatrix} i_{s,d} & i_{s,q} & i_{s,0} \end{bmatrix}^T = \mathbf{K}\,\mathbf{i_s} \qquad (23.b)$$

$$\mathbf{d'^r} \overset{\Delta}{=} \begin{bmatrix} d'_d & d'_q & d'_0 \end{bmatrix}^T = \mathbf{K}\,\mathbf{d'} \qquad (23.c)$$

equations (19) and (21) can be arranged as given in (24).
The voltage and current zero sequence components $v_{s,0}$ and $i_{s,0}$ are eliminated, as shown by (10) and (11). A time-invariant equivalent model of the converter can be elaborated by averaging the term $[\mathbf{K}\,\mathbf{SGN}^{-1}\,\mathbf{K}^T]^{-1}$ over the mains period T_0, as mentioned above. Furthermore, the generality of the modeling approach would not be lost if we assume balanced sine wave line currents. It follows:

$$< \left[\mathbf{K}\cdot\mathbf{SGN}^{-1}\cdot\mathbf{K}^{\mathbf{T}}\right]^{-1} >_{T_0} \cong a\begin{bmatrix} 0 & 0 & \cos j \\ 0 & 0 & \sin j \\ \cos j & \sin j & 0 \end{bmatrix} \qquad (25)$$

$$v_{s,d} = L\frac{di_{s,d}}{dt} - Lw_0 i_{s,q} + \frac{v_0}{2}d'_d \qquad (24.a)$$

$$v_{s,q} = L\frac{di_{s,q}}{dt} + Lw_0 i_{s,d} + \frac{v_0}{2}d'_q \qquad (24.b)$$

$$C_0\frac{dv_0}{dt} + i_{0,h} + i_{0,l} = \frac{3}{2}\left(d'_d i_{s,d} + d'_q i_{s,q}\right) - \frac{\Delta v_0}{v_0}\left(\mathbf{d'}^r\right)^T\left[\mathbf{K}\,\mathbf{SGN}^{-1}\,\mathbf{K}^T\right]^{-1}\mathbf{i_s^r} \qquad (24.c)$$

$$C_0\frac{d\,(\Delta v_0)}{dt} + i_{0,h} - i_{0,l} = -\frac{3}{2}\frac{?v_0}{v_0}\left(d'_d i_{s,d} + d'_q i_{s,q}\right) + \left(\mathbf{d'}^r\right)^T\left[\mathbf{K}\,\mathbf{SGN}^{-1}\,\mathbf{K}^T\right]^{-1}\mathbf{i_s^r} \qquad (24.d)$$

where j denotes the phase shift between the phase voltage and the corresponding line current. The parameter a is estimated by:

$$a \cong \frac{2}{p} \cong 0.64 \tag{26}$$

Note that $\langle x \rangle_{T_0}$ is the average of x over T_0. In a unity power factor operating mode, j equals zero and, hence, we may rewrite system (24) as follows:

$$\begin{aligned}
v_{s,d} &= L\frac{di_{s,d}}{dt} - Lw_0 i_{s,q} + \frac{v_0}{2}d'_d \\
v_{s,q} &= L\frac{di_{s,q}}{dt} + Lw_0 i_{s,d} + \frac{v_0}{2}d'_q \\
C_0\frac{dv_0}{dt} &= \frac{3}{2}\left(d'_d i_{s,d} + d'_q i_{s,q}\right) - a\frac{\Delta v_0}{v_0}d'_0\, i_{s,d} - i_{0,h} - i_{0,l} \\
C_0\frac{d(\Delta v_0)}{dt} &= a\, d'_0\, i_{s,d} - \frac{3}{2}\frac{\Delta v_0}{v_0}\left(d'_d i_{s,d} + d'_q i_{s,q}\right) - i_{0,h} + i_{0,l}
\end{aligned} \tag{27}$$

As shown by equations (27), the converter in Fig. 1 may thus be represented in low-frequency domain by a fourth-order nonlinear dynamic system, having $i_{s,d}$, $i_{s,q}$, v_0 and Δv_0 as state variables, d'_d, d'_q and d'_0 as control inputs, $v_{s,d}$ and $v_{s,q}$ as disturbance inputs.

IV – STEADY-STATE OPERATING REGIME

In the following, the theoretical expressions and waveforms of all system variables are established in the steady-state regime assuming:

- a balanced three-phase voltage source, i.e.:

$$\begin{aligned}
v^*_{s,1n}(t) &= V_S^*\sqrt{2}\sin(w_0 t) \\
v^*_{s,2n}(t) &= V_S^*\sqrt{2}\sin(w_0 t - 2p/3) \\
v^*_{s,3n}(t) &= V_S^*\sqrt{2}\sin(w_0 t - 4p/3)
\end{aligned} \tag{28}$$

where V_S^* is the steady-state RMS-value of the mains phase-to-neutral voltage,

- a unity power factor operating condition, i.e.:

$$\begin{aligned}
i^*_{s,1}(t) &= I_S^*\sqrt{2}\sin(w_0 t) \\
i^*_{s,2}(t) &= I_S^*\sqrt{2}\sin(w_0 t - 2p/3) \\
i^*_{s,3}(t) &= I_S^*\sqrt{2}\sin(w_0 t - 4p/3)
\end{aligned} \tag{29}$$

I_S^* being the steady-state RMS-value of the line currents,

- and balanced output voltages, i.e.:

$$v^*_{0,h} = v^*_{0,l} = \frac{V_0^*}{2} \tag{30}$$

V_0^* denotes the steady-state fixed value of the overall output voltage. The asterisks in expressions (28) to (30) characterize the steady-state regime. Applying Park's transformation to the voltage and current expressions (28) and (29) yields time-invariant vectors expressed in the rotating frame as:

$$\mathbf{v}_\mathbf{s}^{r\,*} \overset{\Delta}{=} \begin{bmatrix} v^*_{s,d} \\ v^*_{s,q} \\ v^*_{s,0} \end{bmatrix} = \begin{bmatrix} V_S^*\sqrt{2} \\ 0 \\ 0 \end{bmatrix} \quad \text{and} \quad \mathbf{i}_\mathbf{s}^{r\,*} \overset{\Delta}{=} \begin{bmatrix} i^*_{s,d} \\ i^*_{s,q} \\ i^*_{s,0} \end{bmatrix} = \begin{bmatrix} I_S^*\sqrt{2} \\ 0 \\ 0 \end{bmatrix} \tag{31}$$

Substituting expressions (31) into system (27), the steady-state values of the control inputs are obtained as follows:

$$\begin{aligned}
d'^*_d &= \frac{2\,V_S^*\sqrt{2}}{V_0^*} \\
d'^*_q &= -\frac{2\,Lw_0 I_S^*\sqrt{2}}{V_0^*} \\
d'^*_0 &= \frac{i^*_{0,h} - i^*_{0,l}}{a\,I_S^*\sqrt{2}}
\end{aligned} \tag{32}$$

It follows from equations (32) that d'^*_d, d'^*_q and d'^*_0 control respectively the output voltage, the input current and the load unbalance. Furthermore, the power conservation law is verified:

$$3\,V_S^* I_S^* = \frac{V_0^*}{2}\left(i^*_{0,h} + i^*_{0,l}\right) \tag{33}$$

Referring to the stationary frame, the steady-state control inputs are expressed as follows:

$$\begin{bmatrix} d'^*_1 \\ d'^*_2 \\ d'^*_3 \end{bmatrix} \overset{\Delta}{=} \mathbf{K}^{-1}\begin{bmatrix} d'^*_d \\ d'^*_q \\ d'^*_0 \end{bmatrix} = \begin{bmatrix} \hat{d}'\sin(w_0 t - f) + d'^*_0/3 \\ \hat{d}'\sin(w_0 t - f - 2p/3) + d'^*_0/3 \\ \hat{d}'\sin(w_0 t - f - 4p/3) + d'^*_0/3 \end{bmatrix} \tag{34}$$

where:

$$\hat{d}' = \frac{2\,V_S^*\sqrt{2}}{V_0^*\cos f} \tag{35}$$

and:

$$\mathrm{tg}\, f = \frac{Lw_0 I_S^*}{V_S^*} \tag{36}$$

Using equation (18), we may set therefore expression (37) (in the bottom of this page), for $k \in \{1, 2, 3\}$. This expression shows that the duty cycles d_1^*, d_2^* and d_3^* vary periodically, with a $T_0/2$ period. It also emphasizes the control saturation phenomenon, which takes place periodically. Its maximum duration angle is given by:

$$g = f + \sin^{-1}\left(\frac{\left|d_0'^*\right|}{3\hat{d}'}\right) \tag{38}$$

or, using equations (32), (33) and (35):

$$g = f + \sin^{-1}\left(\frac{\Delta i_0^*}{i_{0,h}^* + i_{0,l}^*}\frac{\cos f}{2a}\right) \tag{39}$$

where $\Delta i_0^* \stackrel{\Delta}{=} \left|i_{0,h}^* - i_{0,l}^*\right|$. It is noticed from expressions (36) and (39) that, in order to reduce the undesirable effects of the control saturation, the load unbalance must be limited and the inductor value L has to be minimized.

Furthermore, following equations (13) and (18), the averaged middle point voltage may be expressed as:

$$v_{M,n} \cong -\frac{v_0}{6}\sum_{k=1}^{3}\left[1 - \frac{\Delta v_0}{v_0}\,\mathrm{sgn}\left(i_{s,k}\right)\right]d_k' \tag{40}$$

Using equation (34), it follows in steady state regime:

$$v_{M,n}^* = -\frac{V_0^*}{6}\sum_{k=1}^{3} d_k'^* = -\frac{V_0^*\, d_0'^*}{6} \tag{41}$$

Concerning the steady-state expressions of DC-side currents i_+ and i_-, they could be easily established as:

$$i_+^* = \frac{1}{2}\sum_{k=1}^{3} d_k'^* i_{s,k}^* \left[1 + \mathrm{sgn}\left(i_{s,k}^*\right)\right] \tag{42.a}$$

and:

$$i_-^* = \frac{1}{2}\sum_{k=1}^{3} d_k'^* i_{s,k}^* \left[1 - \mathrm{sgn}\left(i_{s,k}^*\right)\right] \tag{42.b}$$

Substituting equations (29) and (34) into (42.a), it yields after some manipulation to the expressions given (in the bottom of this page) by (43) for current i_+^*. Similar expressions are obtained for current i_-^*, but their corresponding intervals are shifted by p. Note that currents i_+^* and i_-^* have practically a third harmonic sine wave shape.

V – DESIGN CRITERIA

5.1. Inductors design

In order to ensure current waveshaping in steady-state regime, the common value of mains series inductors have to satisfy the following conditions, as described in Fig. 3:

$$\left.\begin{aligned} v_{s,kn}^* - v_{M,n} &> L\frac{di_{s,k}^*}{dt} \\ v_{s,kn}^* - v_{M,n} - \frac{V_0^*}{2} &< L\frac{di_{s,k}^*}{dt} \end{aligned}\right\} \quad , \quad \text{when } i_{s,k}{}^* > 0 \tag{44.a}$$

$$\left.\begin{aligned} v_{s,kn}^* - v_{M,n} &< L\frac{di_{s,k}^*}{dt} \\ v_{s,kn}^* - v_{M,n} + \frac{V_0^*}{2} &> L\frac{di_{s,k}^*}{dt} \end{aligned}\right\} \quad , \quad \text{when } i_{s,k}{}^* < 0 \tag{44.b}$$

$$d_k^* = 1 - d_k'^*\,\mathrm{sgn}\left(i_{s,k}^*\right) = \begin{cases} 1 - \hat{d}'\sin\left[w_0 t - f - 2(k-1)p/3\right] - d_0'^*/3 & , \quad 2(k-1)p/3 < w_0 t < p + 2(k-1)p/3 \\ 1 + \hat{d}'\sin\left[w_0 t - f - 2(k-1)p/3\right] + d_0'^*/3 & , \quad p + 2(k-1)p/3 < w_0 t < 2p + 2(k-1)p/3 \end{cases} \tag{37}$$

$$i_+^* = \begin{cases} \frac{\sqrt{2}}{2}\hat{d}' I_S^*\left[2\cos f + \cos\left(2w_0 t - f - 4p/3\right)\right] - \frac{\sqrt{2}}{3} d_0'^* I_S^* \sin\left(w_0 t - 2p/3\right) & , \quad 0 < w_0 t < p/3 \\ \frac{\sqrt{2}}{2}\hat{d}' I_S^*\left[\cos f - \cos\left(2w_0 t - f\right)\right] + \frac{\sqrt{2}}{3} d_0'^* I_S^* \sin\left(w_0 t\right) & , \quad p/3 < w_0 t < 2p/3 \\ \frac{\sqrt{2}}{2}\hat{d}' I_S^*\left[2\cos f + \cos\left(2w_0 t - f - 2p/3\right)\right] - \frac{\sqrt{2}}{3} d_0'^* I_S^* \sin\left(w_0 t - 4p/3\right) & , \quad 2p/3 < w_0 t < p \\ \frac{\sqrt{2}}{2}\hat{d}' I_S^*\left[\cos f - \cos\left(2w_0 t - f - 4p/3\right)\right] + \frac{\sqrt{2}}{3} d_0'^* I_S^* \sin\left(w_0 t - 2p/3\right) & , \quad p < w_0 t < 4p/3 \\ \frac{\sqrt{2}}{2}\hat{d}' I_S^*\left[2\cos f + \cos\left(2w_0 t - f\right)\right] - \frac{\sqrt{2}}{3} d_0'^* I_S^* \sin\left(w_0 t\right) & , \quad 4p/3 < w_0 t < 5p/3 \\ \frac{\sqrt{2}}{2}\hat{d}' I_S^*\left[\cos f - \cos\left(2w_0 t - f - 2p/3\right)\right] + \frac{\sqrt{2}}{3} d_0'^* I_S^* \sin\left(w_0 t - 4p/3\right) & , \quad 5p/3 < w_0 t < 2p \end{cases} \tag{43}$$

for each $k \in \{1, 2, 3\}$. The value of $v_{M,n}$, corresponding to each case, is given in Tab.1. After some mathematical developments, we obtain the following condition:

$$L < \min\left(\frac{V_0^* \sqrt{2} - 3 V_S^* \sqrt{3}}{6 w_0 I_S^*}, \frac{6 V_S^* \sqrt{3} - V_0^* \sqrt{2}}{6 w_0 I_S^*} \right) \quad (45)$$

The range of the inductor value L is thus maximized if:

$$V_0^* = \frac{9}{4} V_S^* \sqrt{6} \cong 5.51 V_S^* \quad (46)$$

Furthermore, the inductors are also designed for current ripple limitation. In this perspective, reasoning around the peak value of the line currents yields:

$$L > \frac{1}{f_S \left(\Delta i_s\right)_{\max}} \left(2 V_S^* \sqrt{2} - \frac{V_0^*}{4} - \frac{6 V_S^{*2}}{V_0^*} \right) \quad (47)$$

where f_S is the switching frequency and $(\Delta i_S)_{\max}$ the acceptable current ripple. Finally, the inductors value is chosen accordingly to conditions (45) and (47).

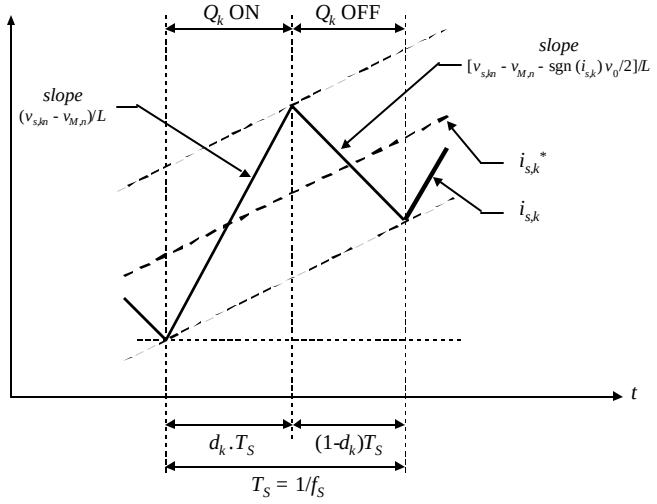

Fig. 3. Line current waveshaping

5.2. Capacitors design

The two DC side capacitors of the converter are designed in the case of a balanced load (i.e., $\Delta i_0^* = 0$). Referring to the expression (43), the magnitude of the DC side upper current ripple can be obtained as:

$$\left(\Delta \hat{i}_+^*\right) = \frac{V_S^* I_S^*}{V_0^*} \left(\frac{2}{\cos f} - 1 \right) \quad (48)$$

It follows:

$$C_0 > \frac{2 V_S^* I_S^*}{3 w_0 V_0^* \left(\Delta v_0\right)_{\max}} \left(\frac{2}{\cos f} - 1 \right) \quad (49)$$

where $(\Delta v_0)_{\max}$ is the admissible output voltage ripple.

VI – SIMULATION RESULTS

In order to verify the theoretical development in sections III and IV, a simulation work is carried out using Matlab/Simulink tool. A numerical version of the converter in Fig. 1 is implemented in low-frequency domain, as indicated in Fig. 4. The numerical values of the converter parameters and steady-state operating point are given in the appendix. The load is purely resistive. The design of the control system is not presented in this paper. The simulation results are presented in Fig. 5 As shown in Fig. 5.a, the converter operates under a unity power factor condition. Furthermore, as indicated in Fig. 5.b, the upper and lower output voltages are practically equal at $V_0^*/2$, with a relatively low voltage ripple, despite the load unbalance. In addition, referring to Fig. 5.c and 5.d, one may easily notice that the DC currents i_+ and i_- have practically the shape of two opposite-phase third-harmonic sine waves, as discussed in section IV. Furthermore, the control saturation angle g noticed in Fig. 5.e is equal to 24 degrees and, therefore, satisfies equation (39). Finally, the estimated parameter a , presented in Fig. 5.f, oscillates around 0.53, which is slightly different from the theoretical value given in (26).

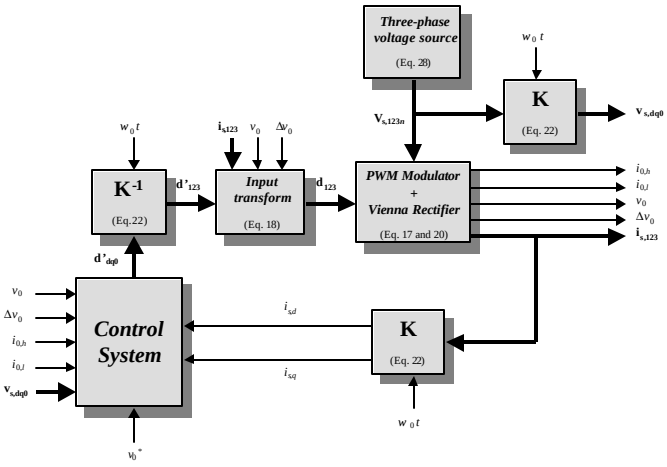

Fig. 4. Numerical implementation of the converter

VII – CONCLUSION

A new low-frequency time-invariant model of a three-phase, three-switch, three-level rectifier has been established in this paper. The steady-state unity power factor operating mode was analyzed, and design criteria concerning the choice of the

output voltage and the reactive components were also presented. The proposed modeling approach has been verified numerically using Matlab/Simulink. The model thus obtained would be suitable for control design implementation.

APPENDIX

Phase-to-neutral voltage RMS-value	$V_S^* = 120$ V
Overall output voltage	$V_0^* = 700$ V
Utility frequency	$f_0 = 60$ Hz
Switching frequency	$f_S = 50$ kHz
Mains series inductors	$L = 1$ mH, each
Output capacitors	$C_0 = 1$ mF, each
Upper load resistor	$R_{0,h} = 9.8\ \Omega$
Lower load resistor	$R_{0,l} = 19.6\ \Omega$

REFERENCES

[1] J. W. Kolar and H. Ertl, "Status of the techniques of three-phase rectifier systems with low effects on the mains", *21st INTELEC*, Copenhagen, Denmark, June 6-9, 1999.

[2] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules", IEEE Transactions on Industrial Electronics, vol.44, No.4, pp. 456-467, Aug. 1997.

[3] J. W. Kolar, F. Stögerer, J. Miniböck and H. Ertl, "A new concept for reconstruction of the input phase currents of a three-phase/switch/level PWM (Vienna) rectifier based on neutral point current measurement", *PESC'2000*, vol.1, pp. 139-146, 2000.

[4] R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching-converter power stages", Proceedings of the IEEE Power Electronics Specialists Conf., Cleveland, OH., June 8-10, 1976.

[5] R. Wu, S. B. Dewan and G. R. Slemon, "Analysis of an ac-to-dc voltage source converter using PWM with phase and amplitude control", *IEEE Transactions on Industry Applications*, vol.27, No.2, pp. 355-364, Mar./Apr. 1991.

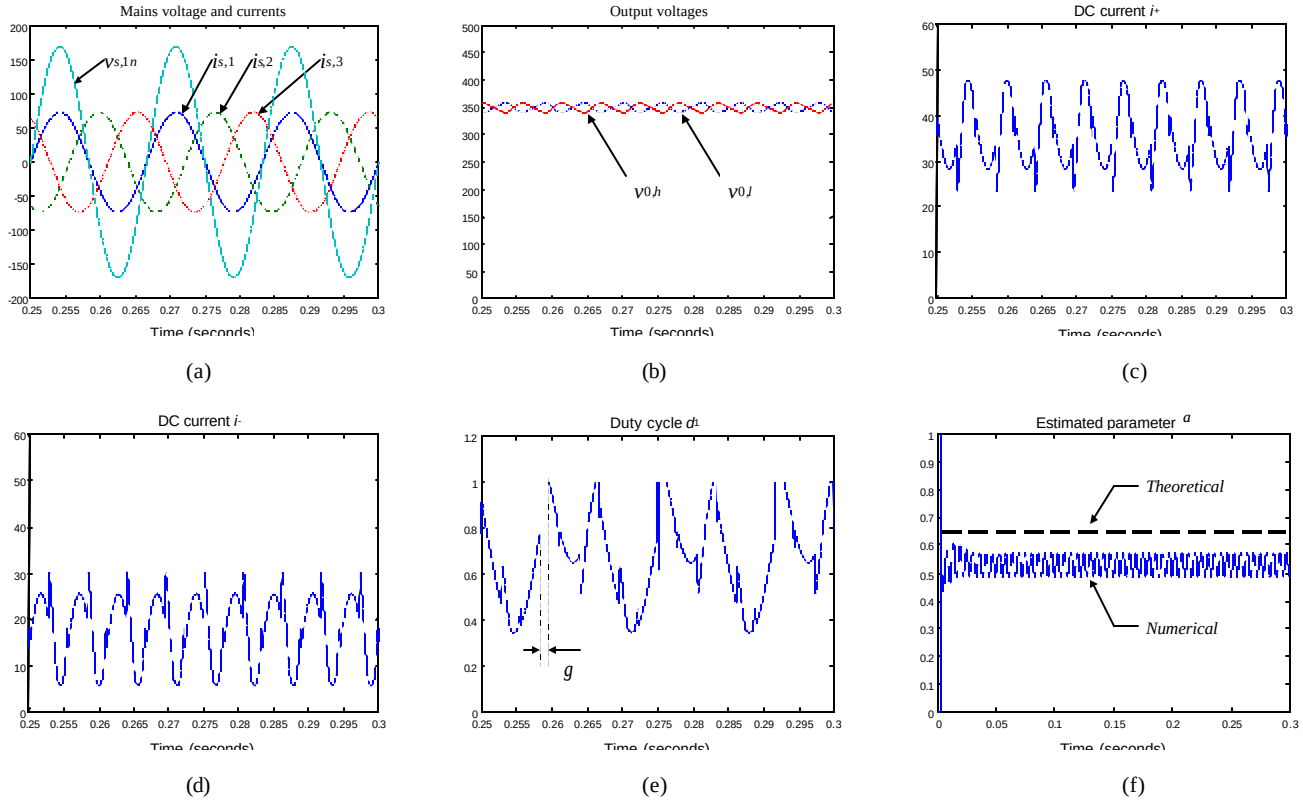

Fig. 5. Simulation results for the steady-state regime. a) Mains voltage and currents, b) Upper and lower output voltages, c), d) Upper and lower DC side currents, e) Duty cycle of switch Q_1 , f) Estimated parameter a