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A new low voltage fast SONOS memory with high-k dielectric

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Abstract

The comparison of simulated write/erase characteristics of silicon–oxide–nitride–oxide–silicon (SONOS) nonvolatile memory with different oxides SiO_2, Al_2O_3 and ZrO_2 as a top dielectric was made. We demonstrate, that an application of high-k dielectrics allows to decrease the write/erase programming voltage amplitude or programming time from 1 ms to 10 μs. The ZrO_2 suppresses parasitic electron injection from polysilicon gate. Also the design of SONOS memory based on high-k dielectrics is promising for terabit scale using hot carriers injection EEPROM and DRAM memory.

Keywords: SONOS; EEPROM; FLASH; Silicon nitride; High-k dielectrics

1. Introduction

Today the key dielectrics such as SiO_2 and Si_3N_4 are widely used in the modern silicon devices. Aggressive scaling of CMOS devices and design of DRAM stimulates the investigation of alternative to SiO_2 and Si_3N_4 high dielectric constant (high-k) dielectrics, such as Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, etc. [1,2]. Since 1990 nonvolatile semiconductor memory (NVSM) has been the technology driver of the semiconductor industry [3]. At the present time a floating gate FLASH EEPROM dominates in the NVSM market. The floating gate type of FLASH EEPROM is impossible to scale down to beyond 0.18 μm due to the difficulty in scaling the tunnel oxide [4]. However, for design of terabit EEPROM memory array it is necessary to use the channel length of 30–40 nm. On contrary, a silicon–oxide–nitride–oxide–silicon (SONOS) EEPROM potentially can be scaled up to this size [5,6]. Recently SONOS with thick bottom oxide was proposed, where write/erase (W/E) is produced due to hot electron/hole injection in nitride [7,8]. Also there were attempts to use SONOS as DRAM devices [9].

Usually SiO_2 is applied as a top oxide in a conventional SONOS. Since SiO_2 has low dielectric constant $\varepsilon = 3.9$ in comparison with Si_3N_4 ($\varepsilon = 7.5$) the electric field in top oxide is about two time larger, than in nitride. Therefore, for scaled SONOS device with comparable thickness of nitride and SiO_2 top oxide, a remarkable part of applied voltage drops on the top oxide during W/E programming. Replacing SiO_2 by high-k dielectric can decrease this undesirable voltage drop and, consequently, the total applied voltage [10–12]. Moreover, because of an electric field in high-k dielectric much less than one in SiO_2, one can expect that parasitic carrier injection [13] through top oxide should be suppressed in SONOS with high-k dielectric as a top layer. These suppositions were supported by experiment with SONOS with Al_2O_3 as a blocking oxide [11] and by preliminary simulations of W/E process in SONOS with Al_2O_3 and ZrO_2 as a top oxide [12].

The goal of the present paper is more detail investigation on the base numerical simulation of the properties of SONOS with high-k dielectrics instead of conventional SONOS with SiO_2 as a top blocking dielectric. This includes also the description of physical phenomena, which take place during W/E process and discussion the possible advantages of SONOS with high-k dielectrics. As example we considered Al_2O_3 ($\varepsilon = 9$)

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and ZrO_2 ($\varepsilon = 25$) as mostly studied high-k dielectrics with well determined energy diagram.

2. Theoretical model

One-dimensional two bands model of charge transport is used, which takes into account Shockley–Read–Hall approach for trap population, continuity and Poisson equation. This model considers carrier double injection from silicon substrate and from opposite electrode (poly-Si gate). The system evolution is described by the following equations

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{e}\frac{\partial j(x,t)}{\partial x} - \sigma \upsilon n(x,t)(N_t - n_t(x,t)) + n_t(x,t)P(x,t) - \sigma_r \upsilon n(x,t)p_t(x,t) \quad (1)$$

$$\frac{\partial n_t(x,t)}{\partial t} = \sigma \upsilon n(x,t)(N_t - n_t(x,t)) - n_t(x,t)P(x,t) - \sigma_r \upsilon p(x,t)n_t(x,t) \quad (2)$$

$$\frac{\partial p(x,t)}{\partial t} = \frac{1}{e}\frac{\partial j_p(x,t)}{\partial x} - \sigma \upsilon p(x,t)(N_t - p_t(x,t)) + p_t(x,t)P(x,t) - \sigma_r \upsilon p(x,t)n_t(x,t) \quad (3)$$

$$\frac{\partial p_t(x,t)}{\partial t} = \sigma \upsilon p(x,t)(N_t - p_t(x,t)) - p_t(x,t)P(x,t) - \sigma_r \upsilon p(x,t)n_t(x,t) \quad (4)$$

$$\frac{\partial F}{\partial x} = -e\frac{(n_t(x,t) - p_t(x,t))}{\varepsilon \varepsilon_0} \quad (5)$$

Here n, N_t, and n_t are densities of free electrons, electron traps, and occupied traps, respectively, p and p_t are the densities of free and captured holes. We assume in our model that number of traps for electrons and for holes is the same. $F(x,t)$ is the local electric field, e is the electron charge, σ is the cross-section of the trap, σ_r is the cross-section of recombination between free carrier and carrier of opposite charge captured by trap, υ is an electron and hole drift velocity, and $\varepsilon = 7.5$ is a low frequency dielectric constant of Si_3N_4. P is the probability of trap ionization per second. The drift electron and hole current density are written as $j = en\upsilon$ and $j_p = -ep\upsilon$. For trap ionization probability was used multi-phonon model, which gives good agreement with experimental results of charge transport in MNOS [14]. Within this model [15] the probability of trap ionization is

$$P = \sum_{n=-\infty}^{+\infty} \exp\left[\frac{nW_{ph}}{2kT} - S\coth\frac{W_{ph}}{2kT}\right] \times I_n\left(\frac{S}{\sinh(W_{ph}/2kT)}\right) P_i(W_t + nW_{ph})$$

$$P_i(W) = \frac{eF}{2\sqrt{2m^* W}} \exp\left(-\frac{4}{3}\frac{\sqrt{2m}}{\hbar eF}W^{3/2}\right), \quad S = \frac{W_{opt} - W_t}{W_t} \quad (6)$$

Here W_{opt} is the optical energy of trap ionization, W_t is the energy of thermal ionization, W_{ph} is the phonon energy and I_n is modified Bessel function. We assume the same W_{opt}, W_t, W_{ph} values for electron and hole traps. This assumption is supported by experimental results [16], which show the identical behavior of hole or electron retention from nitride under different applied pull voltages. For electron and hole injection both from Si and poly-Si we used Fowler–Nordheim mechanism.

Fig. 1a–c shows energy diagrams of SONOS with SiO_2, Al_2O_3, and ZrO_2 as a top blocking dielectric, respectively. For SONOS with top SiO_2 we considered energy diagram determined in [16–18]. For SONOS with

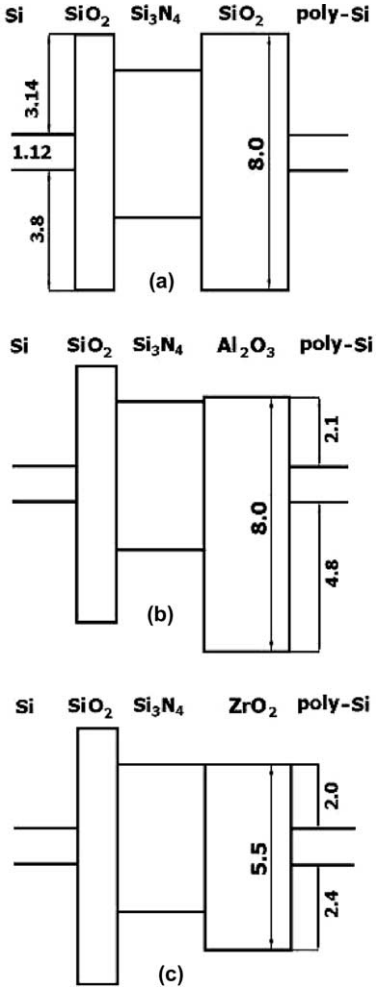

Fig. 1. Energy diagrams of SONOS with SiO_2 (a), Al_2O_3 (b) and ZrO_2 (c) as top dielectric. Energies are indicated in eV.

Al_2O_3 we used the Si/Al_2O_3 electron barrier 2.1 eV [19,20]. For the Al_2O_3 we assumed a gap of 8.0 eV and, consequently, a hole barrier at Si/Al_2O_3 interface should be of 4.8 eV. In simulation we used electron barrier at Si/ZrO_2 interface of 2.0 eV [21,22]. Gap of ZrO_2 is equal to 5.5 eV [22] and, therefore, the hole barrier at Si/ZrO_2 interface of 2.4 eV can be obtained.

3. Results and discussion

In the beginning we simulate W/E characteristics of SONOS with top SiO_2 for +10/−9 V of programming W/E voltages to compare the simulation with experiment [6]. The device geometry and W/E experiment were described in [6] (see Fig. 2). Simulations show the low W/E memory window in comparison with experiment, if we assume the nitride trap density 6×10^{18} cm^{-3}, determined in [23] for thick nitride. Agreement with experiment we get with nitride trap density not less than 5×10^{19} cm^{-3}. High trap density in SONOS with thin nitride most likely is related in excess silicon at Si_3N_4/SiO_2 interface [24].

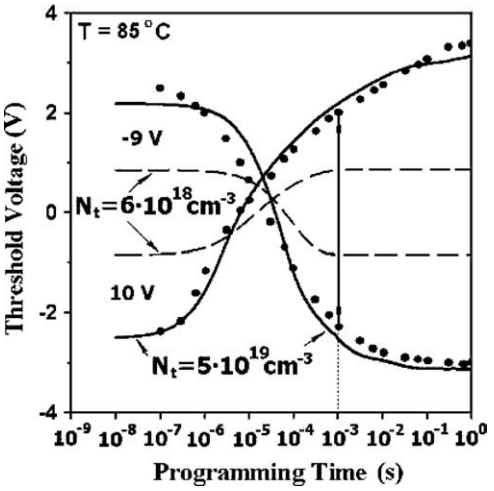

Fig. 2. Write/erase characteristics at temperature $T = 85$ °C of SONOS with SiO_2 as top dielectric, experimental results [6] (dots), simulation for $N_t = 5 \times 10^{19}$ cm^{-3} (solid line) and $N_t = 6 \times 10^{18}$ cm^{-3} (dashed line). Arrow shows W/E window for 1 ms impulse. Parameters for simulation: bottom tunnel oxide thickness 2.0 nm, nitride 4.5 nm and top oxide 5.5 nm, hole tunnel mass in bottom SiO_2 $m^*_e = 0.43\ m_o$, electron tunnel mass in bottom SiO_2 $m^*_e = 0.5\ m^*_e$, electron and hole tunnel masses in Si_3N_4 and top SiO_2 $m^*_e = m^*_h = 0.5\ m_o$. Electron and hole trap parameters in nitride are the same both for electron and hole. Trap cross-section $\sigma = 5 \times 10^{-13}$ cm^2, recombination cross-section $\sigma_r = 5 \times 10^{-13}$ cm^2, trap thermal energy $W_t = 1.8$ eV, trap optical energy $W_{opt} = 3.6$ eV, phonon energy $W_{ph} = 0.064$ eV.

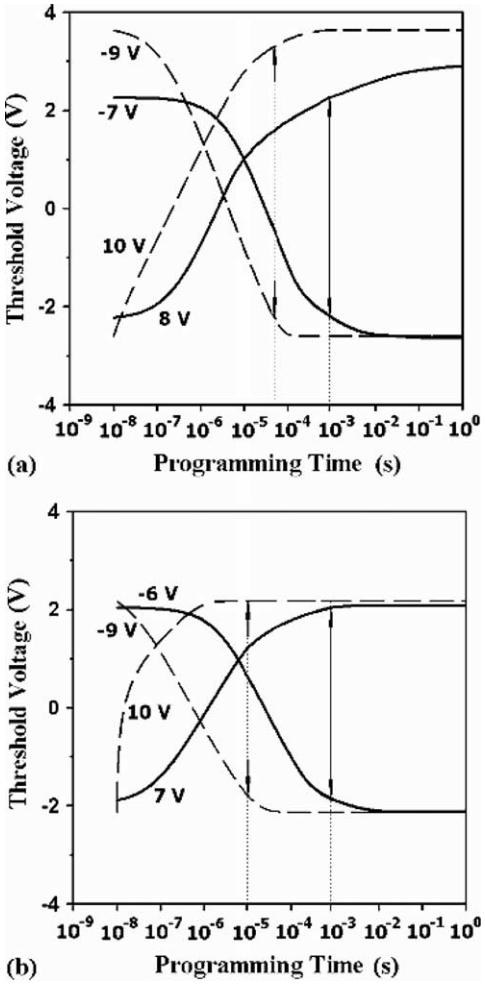

Fig. 3. Write/erase characteristics of SONOS with different top dielectrics: Al_2O_3 (a), ZrO_2 (b). SONOS geometry and simulation parameters for bottom oxide and nitride are the same, as indicated in Fig. 2. Electron and hole tunnel masses in Al_2O_3, and ZrO_2 are $m^*_e = m^*_h = 0.5m_o$. Simulations were performed for W/E voltages (+10/−9 V) (dashed lines) and for lower W/E voltages (solid lines). The last W/E voltages were chosen to get approximately 4 V memory window for pulse duration of 1 ms (solid arrow). The time position of dotted arrow shows the duration of (+10/−9 V) W/E pulse, when approximately the same memory window as in conventional SONOS can be obtained.

For simulation of SONOS with high-k dielectric, as a top oxide, we use the same geometry of SONOS device and the same parameters of traps and carrier effective masses in nitride and in bottom oxide, which were found for the best fit for SONOS with SiO_2 as a top oxide [6]. W/E characteristics for SONOS with top Al_2O_3 and with top ZrO_2 are shown in Fig. 3a and b, respectively. One can see that for the same applied voltage the time of W/E process is less and W/E window in the case of Al_2O_3 is

larger than in conventional SONOS. Our simulations shows that the same time of W/E process can be obtained for less values of applied W/E voltages (+9/−8 V in the case of Al_2O_3, and +7/−6 V in the case of ZrO_2).

The injection currents (dashed lines in Figs. 4–6) through different top dielectric (SiO_2, ZrO_2, Al_2O_3) as function of time were calculated for +9/−8 V W/E pulses. Also we show there the injection current through bottom oxide (solid line). One can see that in conventional SONOS (Fig. 4) injected current decreases for short time region because of captured charge in nitride decreases the field in bottom oxide. In the same time, the charge accumulated in nitride redistributes the electric field in SONOS, so that its value increases in top oxide and, consequently, the parasitic current of opposite sign carriers from poly-Si gate is also enhanced. This process continues up the time when balance between injecting current from Si substrate and parasitic current from gate takes place. Steady state current for −8 V of applied voltage is larger than current for applied voltage of +9 V. This is because of the barrier for electron injection from poly-Si gate is lower than barrier for hole injection (see Fig. 1).

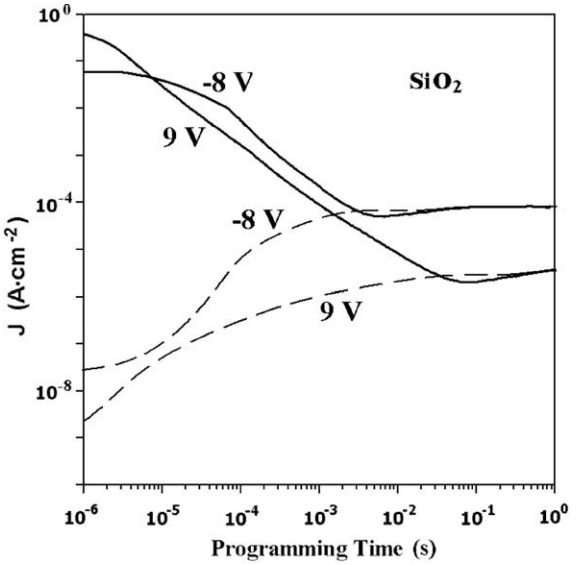

Fig. 4. The amplitude of calculated current versus programming pulse duration (+9/−8 V) on poly-Si gate of conventional SONOS structure with top SiO_2. The currents through bottom dielectric are shown by solid lines. Currents through top dielectric are marked by dashed lines.

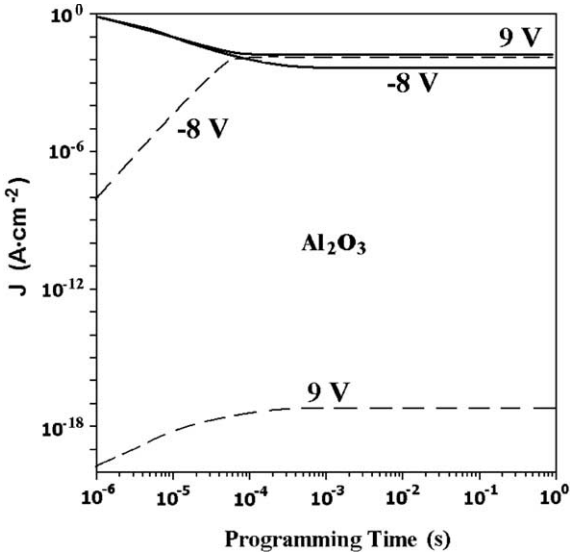

Fig. 5. The same as in Fig. 2, but for SONOS structure with top Al_2O_3.

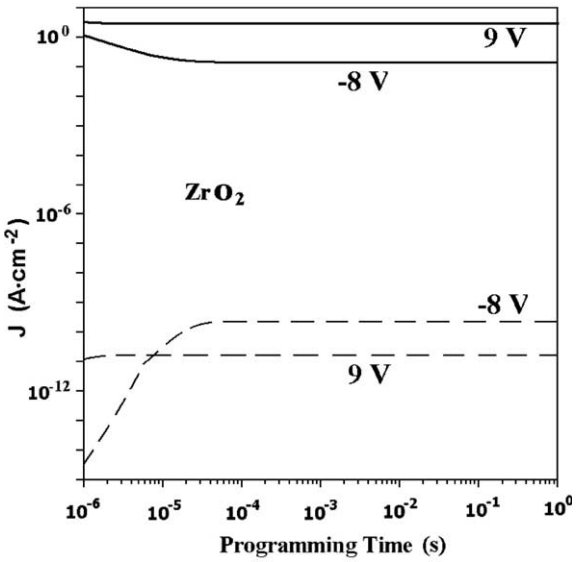

Fig. 6. The same as in Fig. 2, but for SONOS structure with top ZrO_2.

The similar behavior of current with time (Fig. 5) is observed for SONOS with Al_2O_3 as top oxide for negative polarity of applied voltage (−8 V). In this case the steady state current value is also determined by the balance of parasitic electron injection from poly-Si gate and hole injection from Si substrate. Note, that steady state current value in SONOS with Al_2O_3 is larger than for case of conventional SONOS. This effect is due to field enhancing in bottom oxide, if top SiO_2 layer is replaced by Al_2O_3 with higher dielectric constant.

For positive polarity of voltage (+9 V) the parasitic hole injection through top high-k dielectrics is strongly suppressed because of high hole barrier on poly-Si/Al_2O_3 interface (see Fig. 1). In this case there is no

balance between parasitic hole injection and electron injection from Si substrate. The steady state current value is determined by the balance of electron capturing and trap ionization in nitride volume.

Our simulation shows that for SONOS with ZrO_2 top oxide the current from Si substrate is larger than in conventional SONOS or SONOS with Al_2O_3 top oxide (Fig. 6). This is because of high value of ZrO_2 dielectric constant ($\varepsilon = 25$). Therefore, for fixed applied voltage (+9/−8 V), larger part of voltage drops on bottom oxide increasing injection current from Si substrate. It is worth to note that parasitic electron and hole injection from poly-Si gate strongly suppressed for SONOS with ZrO_2 top oxide. Energy diagrams in Fig. 7 illustrate this fact. In spite of relatively low electron barrier on poly-Si/ZrO_2 interface, the electron parasitic injection from poly-Si gate is low due to low electric field in ZrO_2 layer. The steady state current in SONOS with ZrO_2 is controlled by the balance of trap ionization and electrons capturing in nitride volume, which are injected trough bottom oxide.

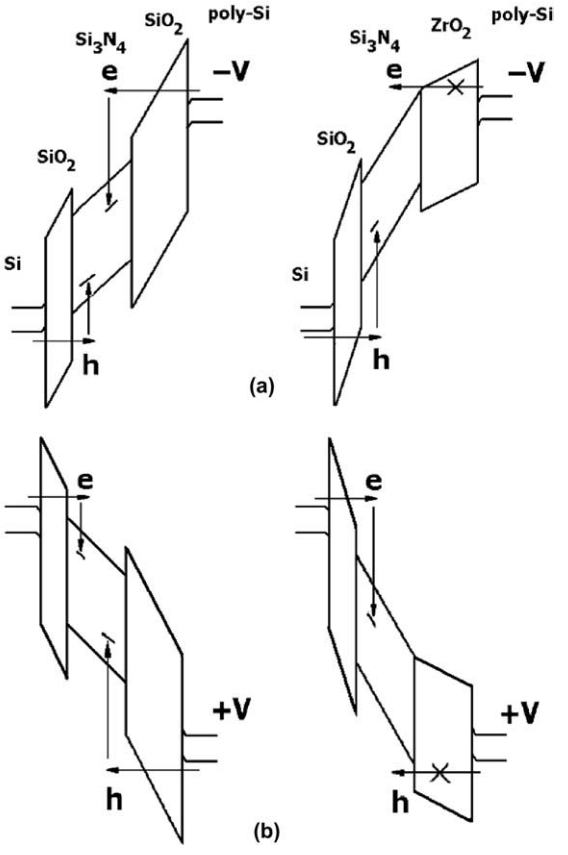

Fig. 7. The schematic comparison write/erase energy diagrams of SONOS structure with different top dielectrics: SiO_2 and ZrO_2. The arrows show injection of electrons or holes through top and bottom dielectrics when the different applied voltage (+9/−8 V) is used.

Two features of SONOS with high-k dielectric (ZrO_2) is demonstrated in Fig. 7. One of them is field enhancing in bottom oxide in SONOS with high-k dielectric. The second one is the field decreasing in the top high-k dielectric resulting in suppressing of parasitic injection from the gate. These features allow to obtain in SONOS with high-k dielectric the same W/E window as in conventional SONOS for shorter pulses duration or for lower voltage amplitude.

4. Conclusion

The simulations show that SONOS with high-k dielectric as a top oxide has the following advantages in comparison with conventional SONOS device:

(1) The W/E voltage can be decreased for the fixed programming pulse duration and SONOS geometry. This is very desirable property for giga- and terabit scale SONOS to eliminate avalanche breakdown in shallow p–n junctions in controlling transistor in peripheral MOS circuits.
(2) The using high-k dielectric for fixed W/E voltage speeds up W/E process. It allows to design the faster SONOS EEPROM on the base of high-k dielectrics.
(3) The top dielectric ZrO_2 drastically suppresses electron and hole injection from poly-Si gate.
(4) For the fixed programming time of pulse and W/E voltages the application of high-k dielectrics as a top dielectric allows to use thicker bottom SiO_2 layer, which can provide the larger retention time.
(5) The W/E window for +9/−8 V pulses in the case of Al_2O_3 is larger than in conventional SONOS.

Here we considered the SONOS with SiO_2 as bottom oxide, since due to the low dielectric constant of SiO_2 this kind SONOS provides high injection capability from Si substrate. Our simulations show that to obtain desirable property of W/E window or programming pulse duration it is important to choose top high-k dielectric with proper dielectric constant and hole and electron barriers on poly-Si/high-k dielectric interface.

We suppose that application of high-k dielectric as top layer also can decrease the W/E voltage and speed up W/E process in SONOS based on hot electron/hole carrier injection [7,8]. Also the using high-k dielectrics can decrease W/E voltage or the W/E process time in SONOS DRAM [9]. Here we simulated SONOS with Al_2O_3 and ZrO_2. Besides, others dielectrics, such as HfO_2, Y_2O_3, Ta_2O_5, TiO_2, etc. can be used for SONOS EEPROM and DRAM optimization.

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