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A New N-Level Inverter Based on Z-NPC

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Abstract: First of all, in this paper, the topology and operation of the three-phase three-level Z-source inverter based on neutral-point-clamped (Z-NPC) are studied. Moreover, different combinations of permissible switching states and control signals are explained for this inverter. In this paper, the topology of the three-phase three-level Z-NPC inverter is extended for an n-level state. Also, a combination of allowed switching states with relevant mathematical equations is presented for the proposed n-level Z-NPC inverter. In comparison with multilevel voltage-source inverters (only voltage-boost capability), the proposed multilevel Z-NPC inverter is a single-stage converter and it has a buck-boost capability of voltage. On the other hand, the control of two-stage converters compared to single-stage converters can be more difficult because of existing more active and passive components. In this paper, two new PWM control methods are also proposed for various multilevel Z-NPC inverters. One advantage of the proposed PWM control methods in comparison with conventional PWM control methods is maintaining the charge balance of the dc-link capacitors in neutral point. The correct performance of the proposed multilevel Z-NPC topology and PWM control methods are verified by the obtained results of analysis and simulations performed in the PSCAD software.

Keywords: Z-Source Inverter, Multilevel Inverter, Neutral-Point-Clamped (NPC) Inverter, Multilevel Z-NPC Inverter, DC-Link Cascaded (DCLC) Inverter, PWM Control Method.

1 Introduction

THE structure of multilevel inverters has been introduced as a suitable alternative for high power and medium voltage conditions [1, 2]. A multilevel inverter not only achieves high power ratings but also makes the use of renewable energy sources possible. The main disadvantage of multilevel inverters is their necessity to a lot of semiconductor switches [3, 4]. In recent decades, the application of multilevel inverters has been increased for having a clean energy by applying fuel cell, wind turbines and photovoltaic systems [5, 6].

Three prominent topologies for multilevel inverter structure are cascaded H-bridges (CHB-MLI), neutral-point-clamped (NPC-MLI) and flying capacitors (FC-MLI) multilevel inverters [7-9].

The conventional voltage-source and current-source inverters have been accepted for applying in medium and high power applications [1, 10]. Due to the intrinsic nature of the conventional voltage-source inverters, these inverters can only step-down their ac output voltages. Hence, these inverters can be used as more suitable topologies for medium voltage ac drives and low-voltage applications such as the grid-interfacing converters and high-speed drive converters [1-4, 11]. The conventional current-source inverters have the only current-buck capability and require a more complex control method. These inverters are known to have the characteristics such as implied output short-circuit protection and better load harmonic filtering by its' ac output capacitors. The limitation of a conventional current-source inverter (the only current–buck capability) makes it not suitable for low voltage condition [10].

One of the solutions for stepping down and stepping up the voltage in the output of inverters is the use of a Z-source inverter with either a dc source voltage or a dc source current [12-17]. The presence of an LC network in the Z-source inverter permits to generate an additional shoot-through (ST) zero switching state which is forbidden in the conventional voltage-source

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inverter [12, 14-17]. The Z-source inverters can be applied in motor drives and fuel cell systems [17-19].

Reference [10] presents the development of two-level single-phase and three phase Z-source inverters of the current-source type controlled using suitable carrier-based reference formulations and synthesized digital logics.

By extending the levels of a two-level Z-source inverter, reference [10] presents the structure of a three-level Z-source inverter based on neutral-point-clamped (Z-NPC) with a suitable PWM control method [16]. The designed Z-NPC inverter uses two unique LC networks that are connected between two isolated dc voltage sources and inverter bridge for stepping up its' ac output voltage [16, 18]. In the three-level Z-NPC inverter, all desirable benefits of three-level switching state are retained. Also, without any need to generate dead time delay in this inverter, it can be operated with a completely eliminated common-mode voltage when two LC networks are short circuited simultaneously and the inverter PWM algorithm is little modified [16, 18].

Reference [11] presents the new topology of a three-level Z-NPC inverter and a Z-source DCLC (dc-link cascaded) inverter, whose ac output voltage can be stepped down or stepped up. Both inverters use only an LC network and a split-dc source. Hence, these inverters compared to the conventional buck-boost dual Z-NPC inverters (including two LC networks and two isolated dc sources [16]) can lead to a system with lower cost. Moreover, the Z-NPC inverters presented in [11] use only the half of passive elements and just a single non-isolated dc source. Thus, these inverters compared to the conventional dual Z-NPC inverters [16] have good performance, and just the disadvantage is a low drop in high-frequency switching. This weakness can be compensated by reducing the number of elements and achieving a system with lower cost. Reference [11] uses a suitable APOD (alternative phase opposition disposition) control method.

Reference [18] presents two new topologies of three-level cascaded Z-source inverters. Both inverters use two three-phase voltage-source inverter bridges that either connected by their dc links for making the DCLC inverter or connected by their ac outputs using three single-phase transformers to achieve the dual Z-source inverter. It should be noted that the structure of DCLC inverter can be controlled only by the modified PD (phase disposition) PWM control method (because of its' lack of redundant switching states), whereas the structure of dual Z-source inverter can be controlled by both modified PD and PSC (phase-shifted-carrier) control methods [18].

Reference [20] presents the topology of a five-level Z-NPC inverter which can step down and step up the ac output voltage.

In topologies of an NPC inverter with more than three levels, controlling voltages of the dc-link capacitors in neutral point (NP) is still known as a problem [21]. Reference [21] proposed a new PWM control method for the NPC inverter based on voltage source.

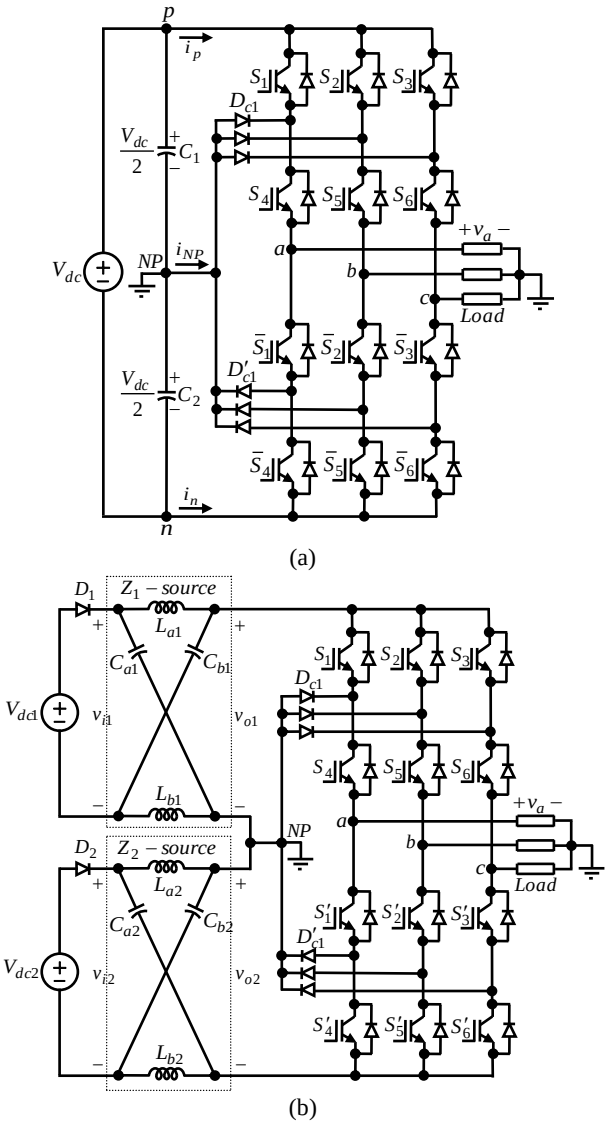


Fig. 1 The topology of three-phase three-level NPC inverters: (a) NPC inverter with a dc source voltage [22], (b) Z-NPC inverter [16, 23].

Firstly, the topology and operating principle of the three-phase three-level Z-NPC inverter are analyzed in this paper. Then, an extended structure of the three-level Z-NPC inverter is proposed. Different combinations of permissible switching states for three- and n-level Z-NPC inverters are presented. Moreover, mathematical equations for n-level Z-NPC inverter are proposed.

To achieving a suitable control for the voltages of the dc-link capacitors in neutral point (NP), in this paper, two new PWM control methods are also proposed for various multilevel Z-NPC inverters. The obtained results of analysis and simulations prove the correct operation of the proposed n-level Z-NPC inverter topology and proposed PWM control methods.

2 Review of Three-Phase Three-Level Z-NPC Inverter Topology

Fig. 1(a) shows the conventional three-phase three-level NPC inverter with a dc source voltage [22] and Fig. 1(b) shows the structure of three-phase three-level Z-NPC inverter [16, 23]. In Fig. 1, the neutral point (NP) is the grounded middle point of an NPC inverter, which by clamping the output voltage to the grounded middle point can be produced the zero voltage. In Fig. 1, v_a is the phase-voltage of phase 'a'. The topology of conventional three-level NPC inverter shown in Fig. 1(a) uses two voltage sources or two capacitors with a common point. Whereas the topology of a three-level Z-NPC inverter shown in Fig. 1(b) applies two Z-sources with two input sources (V_{dc1} and V_{dc2}) without common points. This topology allows the output voltages of Z-source networks (v_{o1} and v_{o2}) can be controlled jointly and separately [22, 23]. On the other hand, in the conventional NPC inverter topologies with more than three levels, keeping the charge balance of the dc link capacitors in neutral point is still known as a problem [21]. Moreover, the capability of voltage-boost can not be done in these topologies, which can be as disadvantages for the conventional NPC inverter topologies.

Different combinations of permissible switching states for phase 'a' switches of three-level V-NPC and Z-NPC inverters have been given in Tables 1 and 2, respectively. Considering Fig. 1(a) and Table 1, it can be observed that the maximum voltage across the each switch is equal to $V_{dc}/2$ in the three-level V-NPC inverter.

Fig. 2 shows the control signals for phase 'a' switches of three-phase three-level conventional NPC inverter with a dc source voltage and Z-NPC inverter. According to Fig. 2(b), the switching signals of S_1 switch are achieved by the set of comparison between the sinusoidal reference signal A_r and the triangular carrier waveform A_{c1} (g_1 state) and comparison between the triangular carrier waveform A_{c1} and square waveform V_{pn} (ST state). The switching signals of S_4 switch are generated only by comparison between the sinusoidal reference signal A_r and the triangular carrier waveform A_{c2} (g_4 state). The switching signals of S_1' switch are complemented with the control signal of g_1. The switching signals of S_4' switch are complemented with the set of g_1 control signal and comparison between the triangular carrier waveform A_{c2} and square waveform V_{pn} (ST state). Considering Figs. 1(b) and 2(b) and Table 2, to generate the ST switching state in Z_1-source network (upper branch) and the non-ST switching state in Z_2-source network (lower branch), the switches of S_1 to S_6 and S_1' to S_3' should be turned on. Whereas, to generate the ST switching state in lower branch and the non-ST switching state in upper branch, the switches of S_1' to S_6' and S_4 to S_6 have to be turned on [22, 23].

Fig. 3 shows the time intervals of ST and non-ST states in one time period of T, which T_{sh1} and T_{nsh1} are time intervals in switching states of ST and non-ST for the upper branch, whereas for the lower branch, T_{sh2} and T_{nsh2} are time intervals in switching states of ST and non-ST, respectively. These two ST states in upper and lower branches (T_{sh1} and T_{sh2}) boost the average voltage across the capacitors (V_C) and the average and maximum voltage across the output of Z-source network ($v_{o,av}$ and $v_{o,\max}$) [16, 23].

3 The Proposed Structure of Three-Phase N-Level Z-NPC Inverter

Fig. 4 shows the expanded structure of the basic topology of a three-phase three-level Z-NPC inverter shown in Fig. 1(b). In this topology, is the number of inverter levels. Three-phase n-level Z-NPC inverter will need the number of switches, diodes-clamped and Z-source networks. Considering Fig. 4, the minimum possible value for the extended structure of a Z-NPC inverter is equal to three. In comparison with the Z-NPC topology by applying only one LC network, the proposed Z-NPC topology can exist different values for

Table 1 The permissible switching states for phase 'a' switches of the three-level conventional NPC inverter with a dc source voltage.

The allowed switching states						v_a
S_1	S_4	D_{c1}	$\bar{S}_1$	$\bar{S}_4$	D_{c1}'	
1	1	0	0	0	1	$+\frac{V_{dc}}{2}$
0	1	1	1	0	1	0
0	0	1	1	1	0	$-\frac{V_{dc}}{2}$

Table 2 The permissible switching states for phase 'a' switches of the three-level Z-NPC inverter.

v_a		$v_{o1,\max}$	0	$-v_{o2,\max}$	0	0
$Z_1 - source$		$v_{o1,\max}$	0	0	ST state	Non-ST state
$Z_2 - source$		0	0	$v_{o2,\max}$	Non-ST state	ST state
The allowed switching states	S_1	1	0	0	1	0
	S_4	1	1	0	1	1
	S_1'	0	1	1	1	1
	S_4'	0	0	1	0	1

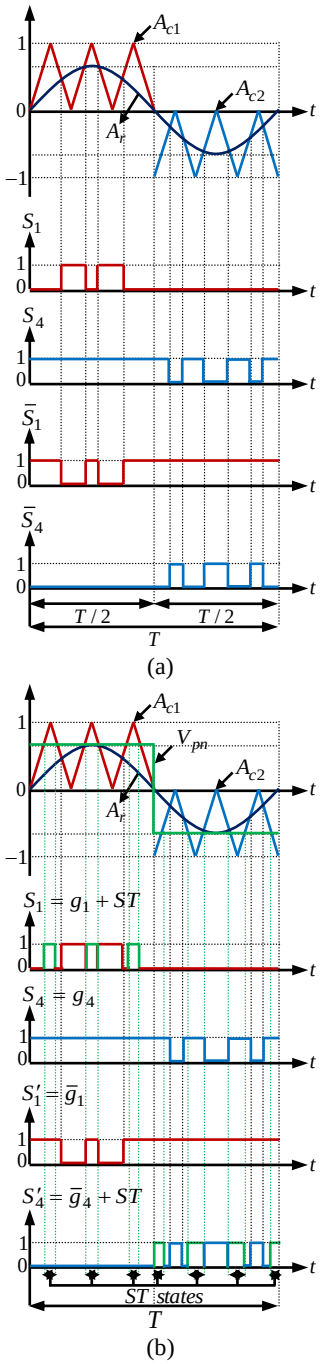


Fig. 2 The control signals for phase 'a' switches: (a) The control signals of conventional NPC inverter, (b) The control signals of Z-NPC inverter.

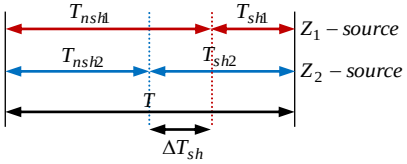


Fig. 3 An example schedule of short-circuited branches in one time period of [23].

inputs dc sources, modulation indexes, duty cycle, boost factor. Whereas, above condition cannot exist for the Z-NPC topology with an LC network. In addition, the proposed Z-NPC topology has the capability of more modularity in terms of the number of different levels with various voltage levels. The above-mentioned advantages will be proved by the achieving results of the simulation.

Table 3 shows the different combinations of allowed switching states for phase 'a' switches of the proposed n-level Z-NPC inverter.

4 The Proposed Control Methods for Variety of Z-NPC Inverter

In NPC inverter topologies with more than three levels, keeping the charge balance of the dc-link capacitors in neutral point is still known as a problem [21]. The PWM control method in [21] has been designed for the NPC inverter based on voltage source. It is noticeable that in the NPC inverter based on Z-source network, the ST switching state should be added to the control method. In this paper, two new PWM control methods for various multilevel NPC inverters based on impedance network are proposed. Fig. 5 shows the proposed control signals for phase 'a' of three-phase five-level Z-NPC inverter. Considering Fig. 5, similar to the conventional PWM control method, the proposed PWM methods use the four triangle carriers (A_c) and one sinusoidal reference (A_r) for the same values of modulation indexes and dc voltage sources and for different values of them, they use the four triangle carriers and two sinusoidal references. The only difference between two PWM control methods is the different amplitudes for triangle carriers in the proposed control methods. In first proposed method (Fig. 5(a)), the amplitude of A_{c1} and A_{c2} is the same ($A_{c1} = A_{c2}$) and the amplitude of A_{c3} and A_{c4} is similar ($A_{c3} = A_{c4}$). In second proposed method (Fig. 5(b)), the amplitude of triangle carriers for A_{c1} to A_{c4} has different values. In first proposed method, the line voltages of inverter is five level because of the same values for triangle carriers of A_{c1} and A_{c2} ($A_{c1} = A_{c2}$) and triangle carriers of A_{c3} and A_{c4} ($A_{c3} = A_{c4}$). Whereas, in second proposed method, the line voltages of inverter is seven level because of different values for triangle carriers for A_{c1} to A_{c4}. Considering Fig. 5(b), the amplitudes of A_{c1} and A_{c4} are between to $0 \le A_{c1} \le 1$ and $-1 \le A_{c4} \le 0$, respectively, and the amplitudes of A_{c2} and A_{c3} are between to "a negative number $\le A_{c2} \le 1$" and "$-1 \le A_{c3} \le$ a positive number", respectively. By increasing the amplitude of negative and positive sections for A_{c2} and A_{c3}, the waveforms of line voltages more tend to seven level. Nevertheless, the charge balance of $Z_1 -$ source to $Z_4 -$ source networks is worsened. In Fig. 5, the charge balance of $Z_1 -$ source to $Z_4 -$ source networks are controlled by

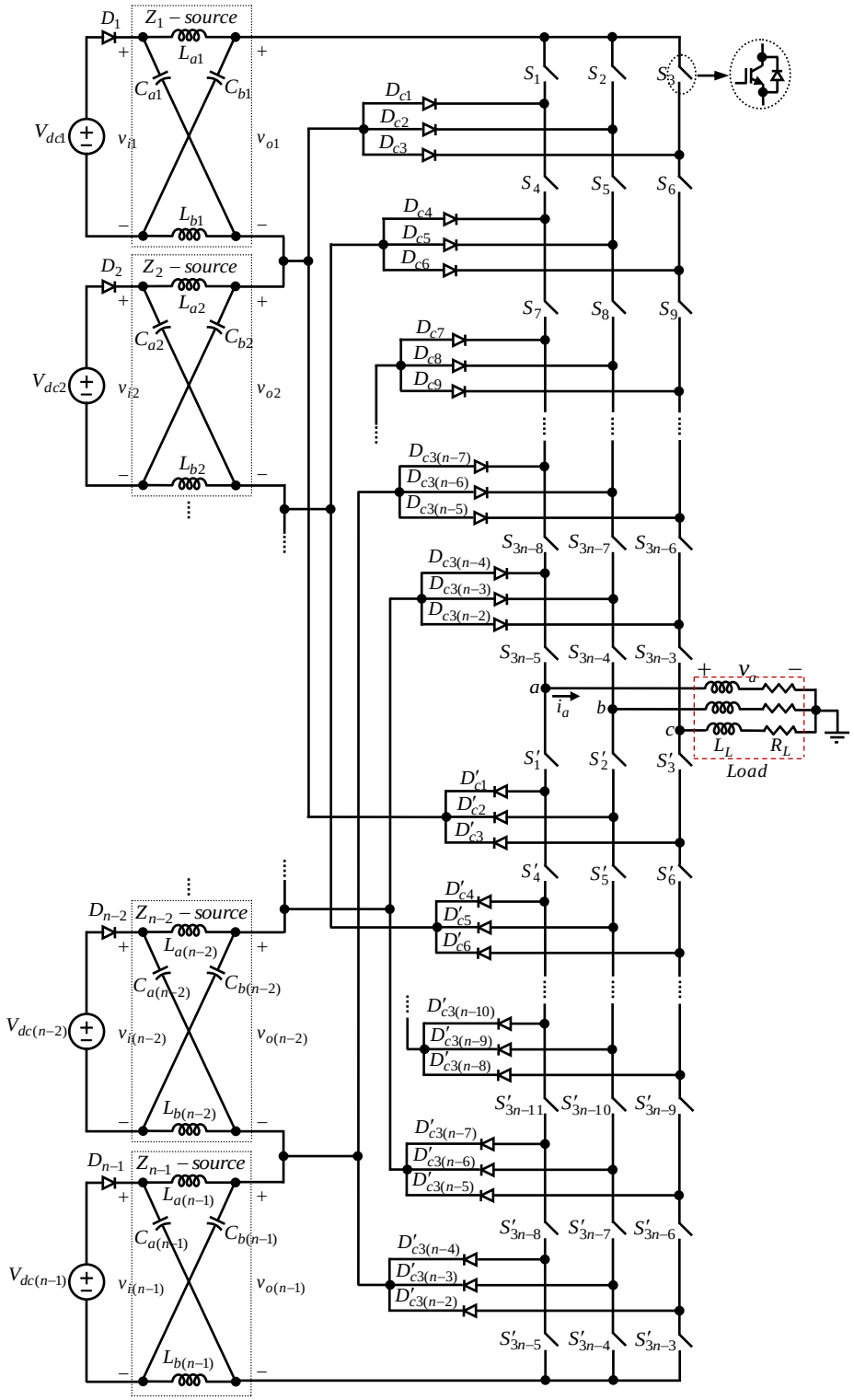


Fig. 4 The proposed structure of three-phase n-level Z-NPC inverter.

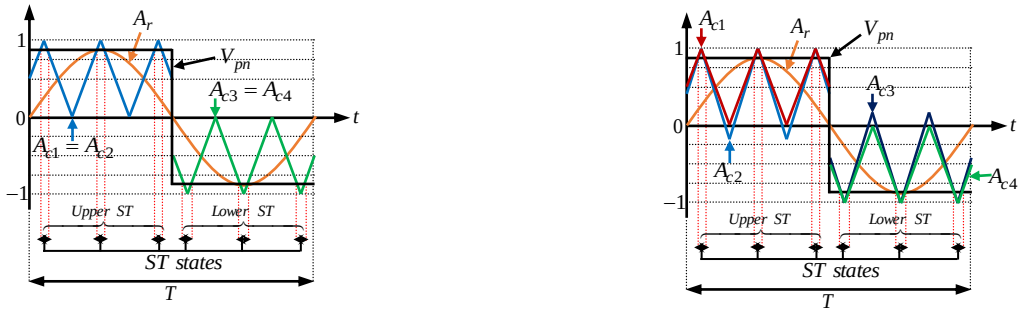
triangle carriers A_{c1} to A_{c4}, respectively. The ST switching state for Z_1 – source and Z_2 – source networks (upper ST state) is generated by comparing A_{c1} and A_{c2} with V_{pn}.

Whereas, the ST switching state for Z_3 – source and Z_4 – source networks (lower ST state) is generated by comparing A_{c3} and A_{c4} with V_{pn}. It should be noted that, besides above issue, the mentioned condition in Table 3 should be considered to control the switches of five-level Z-NPC inverter.

Considering Fig. 4, in the Z_{n-1}-source network, the

Table 3 The permissible switching states for phase 'a' switches of the proposed n-level Z-NPC inverter.

v_a		$v_{o1,\max}+\cdots+v_{o\left(\frac{n-1}{2}\right),\max}$	$v_{o2,\max}+\cdots+v_{o\left(\frac{n-1}{2}\right),\max}$	…	0	…	$-v_{o\left(\frac{n+1}{2}\right),\max}-\cdots-v_{o(n-2),\max}$	$-v_{o\left(\frac{n+1}{2}\right),\max}-\cdots-v_{o(n-1),\max}$	0	0	…	0	0
$Z_1-source$		$v_{o1,\max}$	0	…	0	…	0	0	ST state	Non-ST state	…	Non-ST state	Non-ST state
$Z_2-source$		$v_{o2,\max}$	$v_{o2,\max}$	…	0	…	0	0	ST state	ST state	…	Non-ST state	Non-ST state
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$Z_{\frac{n-1}{2}}-source$		$v_{o\left(\frac{n-1}{2}\right),\max}$	$v_{o\left(\frac{n-1}{2}\right),\max}$	…	0	…	0	0	ST state	ST state	…	ST state	ST state
$Z_{\frac{n+1}{2}}-source$		0	0	…	0	…	$v_{o\left(\frac{n+1}{2}\right),\max}$	$v_{o\left(\frac{n+1}{2}\right),\max}$	ST state	ST state	…	ST state	ST state
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$Z_{n-2}-source$		0	0	…	0	…	$v_{o(n-2),\max}$	$v_{o(n-2),\max}$	Non-ST state	Non-ST state	…	ST state	ST state
$Z_{n-1}-source$		0	0	…	0	…	0	$v_{o(n-1),\max}$	Non-ST state	Non-ST state	…	Non-ST state	ST state
The allowed switching states	S_1	1	0	…	0	…	0	0	1	0	…	0	0
	S_2	1	1	…	0	…	0	0	1	1	…	0	0
	S_3	1	1	…	0	…	0	0	1	1	…	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	S_{n-3}	1	1	…	1	…	0	0	1	1	…	1	1
	S_{n-2}	1	1	…	1	…	0	0	1	1	…	1	1
	S_{n-1}	1	1	…	1	…	1	0	1	1	…	1	1
	S'_1	0	1	…	1	…	1	1	1	1	…	1	1
	S'_2	0	0	…	1	…	1	1	1	1	…	1	1
	S'_3	0	0	…	1	…	1	1	1	1	…	1	1
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	S'_{n-3}	0	0	…	0	…	1	1	0	0	…	1	1
	S'_{n-2}	0	0	…	0	…	1	1	0	0	…	1	1
	S'_{n-1}	0	0	…	0	…	0	1	0	0	…	0	1



(a) (b)

Fig. 5 Proposed control signals of five-level Z-NPC inverter for phase 'a': (a) First proposed method, (b) Second proposed method.

average voltage across the capacitors ($V_{C(n-1)}$) and the average and maximum voltage across the output of Z_{n-1}-source network ($v_{o(n-1),av}$ and $v_{o(n-1),\max}$) are obtained as follows [12, 20]:

$$V_{Ca(n-1)}=V_{Cb(n-1)}=V_{C(n-1)}=v_{o(n-1),av}=\frac{1-D_{n-1}}{1-2D_{n-1}}V_{dc(n-1)} \quad (1)$$

$$v_{o(n-1),\max}=\frac{1}{1-2D_{n-1}}V_{dc(n-1)}=B_{n-1}V_{dc(n-1)} \quad (2)$$

where $V_{dc(n-1)}$ is the input source voltage of $n-1$ branch, $D_{n-1}=\frac{T_{sh(n-1)}}{T}$ is the duty cycle (ST factor) which $T_{sh(n-1)}$ and $T_{nsh(n-1)}$ are time intervals in

switching states of ST and non-ST, respectively, and $T_{n-1}=T_{sh(n-1)}+T_{nsh(n-1)}$ is one complete time period in Z_{n-1}-source network. Also, B_{n-1} is the boost factor of the Z_{n-1}-source network.

According to Fig. 4, by using the sinusoidal PWM (SPWM) algorithm, the maximum amplitude of output phase voltage for the Z-NPC inverter ($v_{Phase,\max}$) can be calculated as follows [12, 23]:

$$\begin{aligned} v_{Phase,\max} &= v_{Phase(Z1-Source),\max} + \cdots \\ &\quad + v_{Phase(Z(n-1)-Source),\max} \\ &= M_1 \frac{V_{dc1}}{2(1-2D_1)} + M_2 \frac{V_{dc2}}{2(1-2D_2)} + \cdots \\ &\quad + M_{n-1} \frac{V_{dc(n-1)}}{2(1-2D_{n-1})} \\ &= \sum_{k=1}^{n-1} M_k \frac{V_{dc(k)}}{2(1-2D_k)} \end{aligned} \tag{3}$$

where M_1, M_2,… and M_{n-2} are the modulation indexes for Z-source networks of Z_1, Z_2,… and Z_{n-1}, respectively.

If the Z-NPC inverter has no the distortion of the input voltage and dc-offset, the following equation can be achieved from (3) [23]:

$$\begin{aligned} v_{Phase(Z1-Source),p-p} &= v_{Phase(Z2-Source),p-p} \\ &= \cdots = v_{Phase(Z(n-1)-Source),p-p} \end{aligned}$$

$$M_1 \frac{V_{dc1}}{1-2D_1} = M_2 \frac{V_{dc2}}{1-2D_2} = \cdots = M_{n-1} \frac{V_{dc(n-1)}}{1-2D_{n-1}} \tag{4}$$

Otherwise, if the Z-NPC inverter has the distortion of the input voltage and dc-offset, these can be eliminated by using two following condition:

a) Different modulation index selection of M_1, M_2, … and M_{n-1} for Z-source networks of Z_1, Z_2, … and Z_{n-1};

b) Different short-circuited factors selection of D_1, D_2, … and D_{n-1} for Z-source networks of Z_1, Z_2, … and Z_{n-1}.

Considering (4), in the first state (the condition of a), if $D_1=D_2=...=D_{n-1}=D$, the following equation will be valid:

$$M_1 V_{dc1} = M_2 V_{dc2} = \cdots = M_{n-1} V_{dc(n-1)} \tag{5}$$

From (5), we can write:

$$\frac{M_1 \times M_4 \times \cdots \times M_{n-1}}{M_2 \times M_3 \times \cdots \times M_{n-2}} = \frac{V_{dc2} \times V_{dc3} \times \cdots \times V_{dc(n-2)}}{V_{dc1} \times V_{dc4} \times \cdots \times V_{dc(n-1)}} \tag{6}$$

Table 4 Used parameters in simulation.

Impedance-source networks	L	$0.1mH$
	C	$2mF$
Output load values	R_L	20Ω
	L_L	$1mH$
Reference signal frequency	f_r	$50\,Hz$
Switching frequency	f	$10\,kHz$

According to (3), if $D_1=D_2=...=D_{n-1}=D$, we can write:

$$\begin{aligned} v_{Phase,\max} &= M_1 \frac{V_{dc1}}{2(1-2D)} + M_2 \frac{V_{dc2}}{2(1-2D)} + \cdots \\ &\quad + M_{n-1} \frac{V_{dc(n-1)}}{2(1-2D)} \end{aligned} \tag{7}$$

From (7), the amplitude of output phase voltage (v_{Phase}) can be varied within the following limits:

$$0 \le v_{Phase} \le \frac{1}{2(1-2D)} \min\left\{V_{dc1}, V_{dc2}, \ldots, V_{dc(n-1)}\right\} \tag{8}$$

Considering (4), in the second state (the condition of b), if $M_1=M_2=\cdots=M_{n-1}=M$, the following equation will be valid:

$$\frac{V_{dc1}}{1-2D_1} = \frac{V_{dc2}}{1-2D_2} = \cdots = \frac{V_{dc(n-1)}}{1-2D_{n-1}} \tag{9}$$

From (9), we can write:

$$\begin{aligned} &\frac{(1-2D_2)\times(1-2D_3)\times\cdots\times(1-2D_{n-2})}{(1-2D_1)\times(1-2D_4)\times\cdots\times(1-2D_{n-1})} = \\ &\frac{V_{dc2}\times V_{dc3}\times\cdots\times V_{dc(n-2)}}{V_{dc1}\times V_{dc4}\times\cdots\times V_{dc(n-1)}} \end{aligned} \tag{10}$$

According to (3), if $M_1=M_2=\cdots=M_{n-1}=M$, we have:

$$\begin{aligned} v_{Phase,\max} &= M \frac{V_{dc1}}{2(1-2D_1)} + M \frac{V_{dc2}}{2(1-2D_2)} + \cdots \\ &\quad + M \frac{V_{dc(n-1)}}{2(1-2D_{n-1})} \end{aligned} \tag{11}$$

From (11), the amplitude of output phase voltage (v_{Phase}) can be varied within the following limits:

$$0 \le v_{Phase} \le \frac{M}{2} \times \sum_{k=1}^{n-1} \left(\frac{V_{dc(k)}}{1-2D_k} \right) \tag{12}$$

Obviously, to establish the expressed provision in (4), both condition of a, and b are possible to be merged.

5 Simulation Results

5.1 First case (when the values of modulation indexes and dc voltage sources are the same)

The used parameters in simulations are given in Table 4. By using Table 4 and proposed control methods, Figs. 6 to 8 show the simulation results for five-level Z-NPC inverter when $M_1 = M_2 = M_3 = M_4 = 0.6$ and $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = 30V$.

Considering above parameters and Table 4, the following results can be obtained for three-phase five-level Z-NPC inverter. The ST duty cycles (D_1 to D_4) are equal to 0.4.

$$D_1 = D_2 = D_3 = D_4 = D = \frac{T_{sh}}{T} = 1 - M = 1 - 0.6 = 0.4$$

Fig. 6 shows the capacitors' voltages of Z_1 – source to Z_4 – source networks (V_C) for the same values of modulation indexes and dc voltage sources. From (1), the calculated values for capacitors' voltages are equal to $90V$, which similar to simulation results shown in Fig. 6. Fig. 7 shows the ST states and the output voltages of upper branch (Z_1 – source and Z_2 – source networks) and lower branch (Z_3 – source and Z_4 – source networks) for the same values of modulation indexes and dc voltage sources. Considering Figs. 5(b) and 7(b), in second proposed method, the amplitudes of A_{c1} and A_{c4} are between to $0 \le A_{c1} \le 1$ and $-1 \le A_{c4} \le 0$, respectively, and the amplitudes of A_{c2} and A_{c3} are between to $-0.1 \le A_{c2} \le 1$ and $-1 \le A_{c3} \le 0.1$, respectively. From (2), the minimum and maximum of output voltages for Z_1 – source to Z_4 – source networks (v_{o1} to v_{o4}) are equal to $0V$ and $150V$, respectively, which similar to simulation results

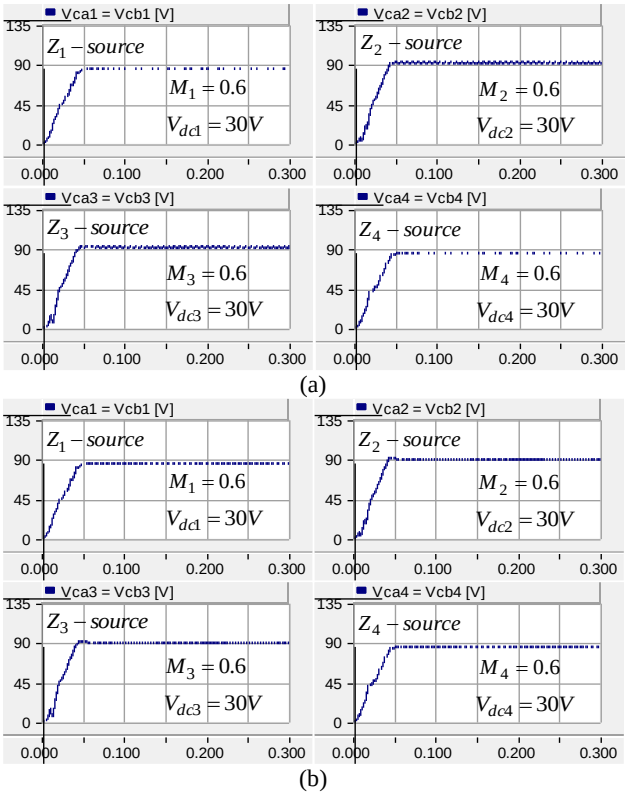


Fig. 6 Capacitors' voltages of LC networks for the same values of M and V_{dc}: (a) First proposed method, (b) Second proposed method.

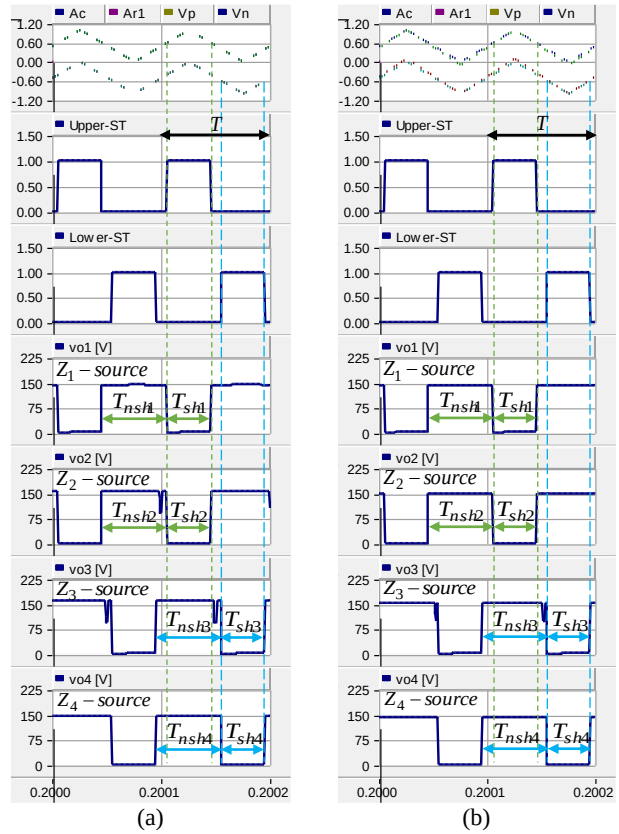


Fig. 7 ST states and output voltages of LC networks for the same values of M and V_{dc}: (a) First proposed method, (b) Second proposed method.

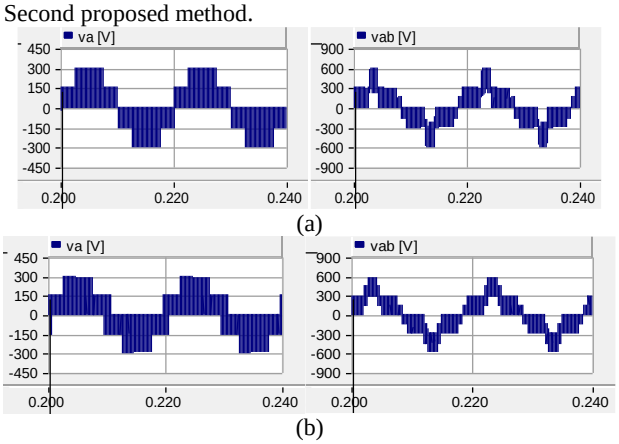


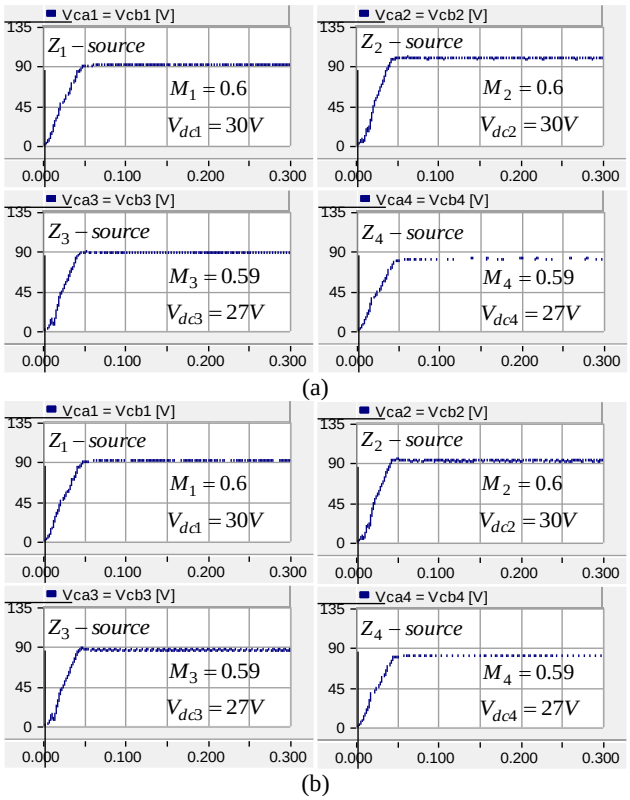
Fig. 8 Phase voltage of phase 'a' (v_a) and line voltage (v_{ab}) for the same values of M and V_{dc}: (a) First proposed method, (b) Second proposed method.

shown in Fig. 7. According to Fig. 7(b), it can be observed that the charge balance of LC networks is better by suitable selection of amplitudes for A_{c2} and A_{c3}. Fig. 8 shows the phase-voltage of phase 'a' (v_a) and the line-voltage (v_{ab}) for the same values of modulation indexes and dc voltage sources. It can be observed that by suitable selection for the amplitudes of A_{c2} and A_{c3}, the waveforms of line voltages tend to seven level. From (6), we have:

$$\frac{M_1M_4}{M_2M_3}=\frac{V_{dc2}V_{dc3}}{V_{dc1}V_{dc4}}\Rightarrow\frac{0.6\times0.6}{0.6\times0.6}=\frac{30\times30}{30\times30}\Rightarrow1=1$$

5.2 Second case (when the values of modulation indexes and dc voltage sources are different)

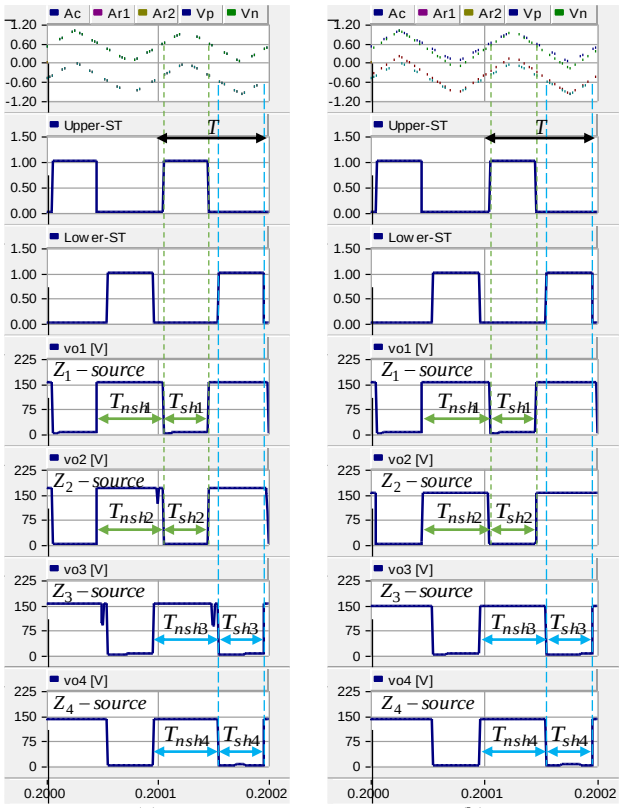
By using Table 4 and proposed control methods, Figs. 9 to 11 show the simulation results for five-level inverter when $M_1=M_2=0.6$, $M_3=M_4=0.59$, $V_{dc1}=V_{dc2}=30V$ and $V_{dc3}=V_{dc4}=27V$. Considering above parameters for input voltages and modulation indexes, the following results can be obtained for three-phase five-level Z-NPC inverter. The ST duty cycles for D_1 and D_2 are equal to 0.4, whereas, they will be equal to 0.41 for D_3 and D_4. From (1), the capacitors' voltages of V_{Ca1} and V_{Ca2} are $90V$, whereas, they are $88.5V$ for V_{Ca3} and V_{Ca4}, which shown in Fig. 9. Fig. 10 shows the ST states and the output voltages of upper branch (Z_1 – source and Z_2 – source networks) and lower branch (Z_3 – source and Z_4 – source networks) for different values of modulation indexes and dc voltage sources. In second proposed method, the amplitudes of A_{c2} and A_{c3} are between to $-0.2\le A_{c2}\le1$ and $-1\le A_{c3}\le0.2$, respectively. From (2), the minimum and maximum of output voltages for



(a)

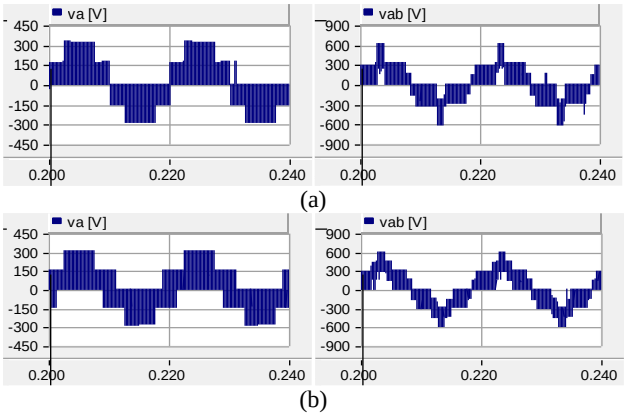
(b)

Fig. 9 Capacitors' voltages of LC networks for different values of M and V_{dc}: (a) First proposed method, (b) Second proposed method.



(a) (b)

Fig. 10 ST states and output voltages of LC networks for different values of M and V_{dc}: (a) First proposed method, (b) Second proposed method.



(a)

(b)

Fig. 11 Phase voltage of phase 'a' (v_a) and line voltage (v_{ab}) for different values of M and V_{dc}: (a) First proposed method, (b) Second proposed method.

Z_1 – source to Z_4 – source networks (v_{o1} to v_{o4}) are equal to $0V$ and $150V$, respectively, which similar to simulation results shown in Fig. 10. It can be observed that under various values for modulation indexes and input voltages, the minimum and maximum voltages across the outputs of LC networks are the same. Fig. 11 shows the phase-voltage of phase 'a' (v_a) and the line-voltage (v_{ab}) for different values of modulation indexes and dc voltage sources. For $D_1 = D_2 = 0.4$, $D_3 = D_4 = 0.41$, $V_{dc1} = V_{dc2} = 30V$ and $V_{dc3} = V_{dc4} = 27V$, from (10), we have:

$$\frac{(1-2D_2)(1-2D_3)}{(1-2D_1)(1-2D_4)} = \frac{V_{dc2}V_{dc3}}{V_{dc1}V_{dc4}} \Rightarrow \frac{(1-0.8)\times(1-0.82)}{(1-0.8)\times(1-0.82)} = \frac{30\times27}{30\times27} \Rightarrow 1=1$$

The obtained simulation results prove the correctness performance of five-level Z-NPC inverter and proposed control methods under different conditions. On the other hand, the mentioned advantages in section 3 are also re-verified.

6 Conclusion

In this paper, the topologies, operation principles, permissible switching states, and control signals of the three-phase three-level NPC inverters based on voltage- and Z-source (V-NPC and Z-NPC) have been reviewed. The V-NPC inverter in comparison with Z-NPC inverter has some disadvantages such as 1- The balance control of the capacitors in neutral point (NP) is hard, 2- Do not have a stepping-up capability in the output voltage. In this paper, due to the importance of multilevel inverters to achieve higher power by using the dc voltage sources with lower voltage levels, the extended structure of three-phase three-level Z-NPC inverter has been proposed. The proposed Z-NPC topology compared to the Z-NPC topology with an LC network has different values for inputs dc sources, modulation indexes, duty cycle, boost factor. Moreover, the proposed Z-NPC topology has the number of different levels with various voltage levels. On the other hand, due to the importance of keeping the charge balance of capacitors for topologies with more than three levels, two new PWM control methods for various multilevel Z-NPC topologies have been proposed in this paper. The simulation results have been used to prove the correctness performance of the proposed structure and PWM control methods and above-mentioned advantages.

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