A NEW OPTIMUM TOPOLOGY SWITCHING DC-TO-DC CONVERTER

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ABSTRACT

A novel switching dc-to-dc converter is presented, which has the same general conversion property (increase or decrease of the input dc voltage) as does the conventional buck-boost converter, and which offers through its new optimum topology higher efficiency, lower output voltage ripple, reduced EMI, smaller size and weight, and excellent dynamic response. One of its most significant advantages is that both input and output current are not pulsating but are continuous (essentially dc with small superimposed switching current ripple), thus resulting in a close approximation to the ideal physically nonrealizable dc-to-dc transformer. The converter retains the simplest possible structure with the minimum number of components which, when interconnected in its optimum topology, yield the maximum performance.

The new converter is extensively experimentally verified, and both the steady state (dc) and the dynamic (ac) theoretical model are correlated well with the experimental data. Both theoretical and experimental comparisons with the conventional buck-boost converter, to which an input filter has been added, demonstrate the significant advantages of the new optimum topology switching dc-to-dc converter.

1 INTRODUCTION

It is commonly believed that the buck, boost, and buck-boost converters are the simplest possible switching structures to realize dc-to-dc level conversion. However, even though structurally quite simple, they do possess some undesirable characteristics, such as pulsation of input or output current, or both. This paper introduces a new converter that has all the desirable properties of buck and boost power stages alone, without acquiring any of their undesirable attributes, and yet with retention of a very simple structure.

This work was supported in part by Subcontract No. A72042-RHBE from TRW Systems Group under NASA Prime Contract NAS3-19690, by Subcontract No. DO4803-CFCM from TRW Systems Group under NASA Prime Contract NAS3-20102, and by the Naval Ocean Systems Center through MIPR No. N0095377MP09018.

Section 2 gives motivation and guidelines to be followed in the synthesis of new switching converters, equally simple but with significantly improved performance, through converter *optimum topology*.

A revised look at these three "basic" converters, and the correlation among their topologies and functions, leads in Section 3 to study of the generic properties of the cascade connection of buck and boost converters. Especially, the recognition of the fact that the conventional buck-boost converter may be considered as a *special case* derived from one kind of cascade connection (buck converter followed by a boost converter) leads quite naturally in Section 3 to the discovery of the *new optimum topology switching dc-to-dc converter*.

In Section 4 the steady state (dc) and dynamic (ac) models of the new switching converter are obtained in the canonical circuit form, and are experimentally verified.

The importance of the *optimum interconnection* of elements is emphasized in Section 5, where the new converter and conventional buck-boost with an input filter, consisting of the same components, are extensively compared both theoretically and experimentally. The superior performance, significantly higher efficiency, and much lower switching ripple are demonstrated for the new converter.

Finally, in Section 6 it is illustrated how the new converter can be implemented in a closed-loop regulator.

2 MOTIVATION AND METHODOLOGY IN THE SEARCH FOR NEW SWITCHING CONVERTER TOPOLOGIES

Several factors and observations, which initially may seem unrelated, will be discussed first because they do in fact motivate and contribute to the search for new switching dc-to-dc converters.

Consider the three common switching dc-to-dc converters, the buck, the boost and the buck-boost shown in Fig. 1. While in Fig. 1a the topological structure of these converters independent of any particular switch realization is shown, in Fig. 1b a bipolar transistor and commutating diode realization of the switch S is used. In each case the basic dc-to-dc conversion function is achieved by control of the switch fractional closed time (transistor on time), or duty ratio, $D(0 < D < 1)$.

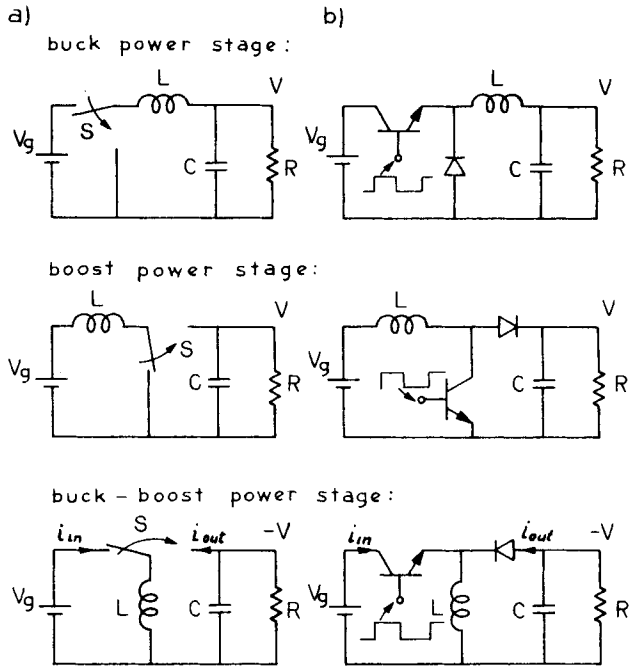

Fig. 1. Three common switching dc-to-dc converters: a) topological configuration independent of switch realization; b) bipolar transistor implementation of the switch S.

Out of three configurations in Fig. 1 only the buck-boost converter is capable of producing the general dc conversion function, that is either decrease (for $D < 0.5$) or increase (for $D > 0.5$) of input dc voltage, since ideally $V/V_g = D/(1 - D)$. The other two converters either always decrease input dc voltage ($V/V_g = D$) as in the buck converter, or increase it ($V/V_g = 1/(1 - D)$) as in the boost converter.

However, all three converters have some serious drawbacks. Consider, for example, the input and output currents for the buck-boost converter (designated i_{in} and i_{out} in Fig. 1) in the continuous conduction mode (inductor current does not fall to zero during the switching interval T_s): in spite of operation in the continuous conduction mode, *both* currents are *pulsating* as illustrated in Fig. 2.

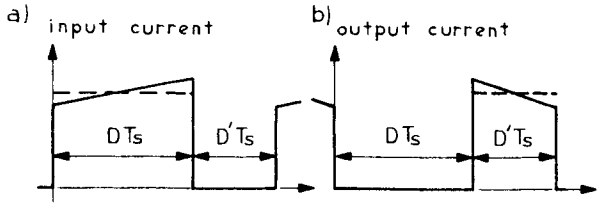

Fig. 2. Input and output current of the buck-boost converter operating in the continuous conduction mode are both pulsating.

It can easily be verified that the buck converter has the same *pulsating input current* as shown in Fig. 2a. Severe electromagnetic interference (EMI) problems result from the abrupt variation in energy flow, and invariably require the presence of an input filter in front of the buck and buck-boost converter to smooth out the substantial current ripple component at the switching frequency f_s drawn from the line supply.

On the other hand, the boost converter of Fig. 1 has the same *pulsating output current* as does the buck-boost converter in Fig. 2b, which is primarily responsible for the *much higher* output voltage ripple of these two converters compared to the buck power stage consisting of the same storage elements and under the same operating conditions. The small output voltage ripple in the buck power stage is a consequence of the nonpulsating output current.

Thus, it becomes a desirable objective to synthesize a switching dc-to-dc converter which possesses, like the buck-boost converter, the general dc conversion property (both increase or decrease of input dc voltage), but which also has *both* input and output currents *nonpulsating*, unlike the buck-boost converter of Fig. 1.

As another motivating factor, consider now the modelling of switching dc-to-dc converters. By use of the general modelling technique [2,3,4], *any switching dc-to-dc converter* (even those yet to be invented), regardless of its detailed configuration, can be represented in the *canonical equivalent circuit form* shown in Fig. 3, as long as the converter operates in the continuous conduction mode. Different converters are represented simply by appropriate sets of formulas for the four elements e(s), j(s), μ, $H_e(s)$ in the general equivalent circuit. Thus, by use of these formulas, the results for the known switching converters, such as those in Fig. 1, may be tabulated. Moreover, from the general formulas, frequency dependence was anticipated also in the duty-ratio-dependent current generator j of Fig. 3, even though for the particular converters of Fig. 1 and for a number of other known converters (Weinberg, Venable), the frequency dependence reduces to a constant and $f_2(s) \equiv 1$. As also discussed in [2,3], for some switching converters which effectively involve more than two storage elements, higher order polynomials are to be expected in $f_1(s)$ and for $f_2(s)$ of Fig. 3.

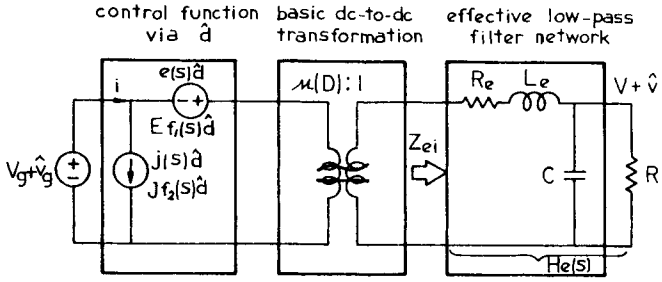

Fig. 3. Canonical equivalent circuit that models the three essential functions of any dc-to-dc converter: control, basic dc conversion, and low-pass filtering (continuous conduction mode).

Therefore, in order to confirm these general modelling predictions, some new switching converter structures had to be devised, since the known converters failed to exhibit such behaviour. Thus, the search for new converters, or for new combinations of existing ones, becomes highly motivated from the modelling and analysis point of view.

While these factors provide a strong motivating force, they do not answer the question of how to approach the design of new converter topologies and what methodology to use in their synthesis. The answer is provided by visualization of a generalized switching dc-to-dc converter as shown in Fig. 4, for which the general modelling technique [2-5] was developed.

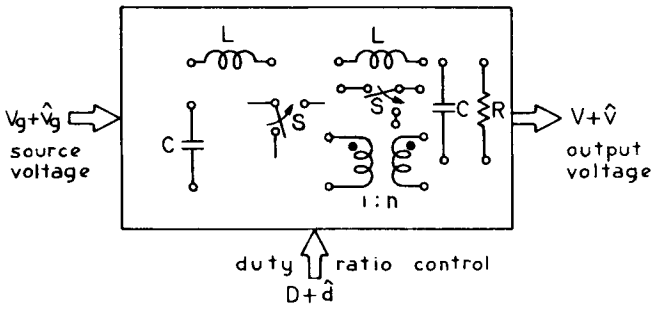

Fig. 4. Generalized switching dc-to-dc converter.

As suggested in Fig. 4, such a switching converter consists of a number of energy storage elements (not necessarily a single inductor and capacitor as in the converters of Fig. 1), transformers and switches (again not restricted to the single switch of Fig. 1) arranged in a certain topology in which periodic opening and closing of switches with fractional closed-time, or duty ratio, D guides the input-power through the network in such a way that dc level conversion dependent on $D(0 < D < 1)$ is obtained at the output.

Because the available elements are not ideal, particularly in the presence of parasitic losses, and owing to the high efficiency requirement, the design objective becomes to use the *minimum number* of switches and storage elements that will permit the required dc level conversion to be realized, and yet to achieve the *maximum performance* (in particular, both input and output current nonpulsating) by their *optimum interconnection*.

3 A NEW OPTIMUM TOPOLOGY SWITCHING CONVERTER

The approach used here to introduce the new optimum topology switching dc-to-dc converter follows quite closely the original line of thought [1,2] employed to arrive at the new converter. The sequence of the proper questions and answers at each stage of its development, together with the underlying principle of *simplification* and *optimum interconnection* (with maximization of performance in mind) emphasized in Section 2, leads quite naturally to the new optimum topology switching dc-to-dc converter. However, before any simplifications can be made, we consider first some fruitful interconnections of the buck and boost converters, which come directly as a result of the revised look at the common converters of Fig. 1.

3.1 Three common converters (buck, boost and buck-boost) revisited

A closer look at the topological structure of the three common converters shown in Fig. 1a reveals that *all* of them could be generated by a *cyclic rotation* of the *series connection* of inductance L and switch S between the input port (source voltage V_g) and the output port (parallel combination of C and load R) as seen in Fig. 5.

This at the same time exhausts all the ways in which inductance is used as an energy transferring device between the input and output ports: either solely in the input circuit, solely in the output circuit, or connecting them. It is then no surprise that the basic dc conversion functions for these three converters are different from each other, both qualitatively and quantitatively, as was demonstrated previously.

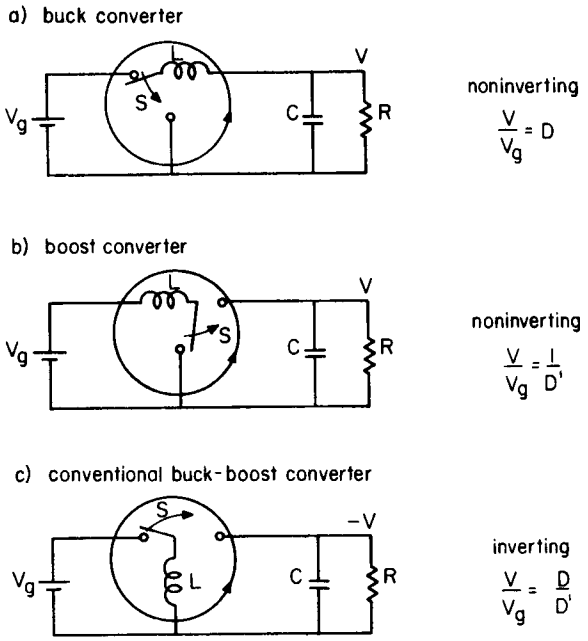

Fig. 5. Generation of the buck, boost and buck-boost converters by cyclic rotation of the series connection of inductance L and switch S.

These dc conversion properties and their method of generation depicted in Fig. 5 tend to suggest that all three converters are completely independent of each other, and are *nonlinear circuits* in their own right. This is probably why they are often referred to as "*basic*" power stages, meaning they cannot be derived from each other by some sequence of well-defined steps.

However, they are not so unrelated and independent as it may seem at first sight, since a strong *correlation* exists among their basic dc conversion relations. Namely, the ideal dc gain for the buck-boost converter $V/V_g = D/D'$ is just the product of the dc gains for the buck ($V/V_g = D$) and the boost converter ($V/V_g = 1/D'$). In fact, it becomes obvious that the same dc gain would be achieved by cascading the buck power stage with the boost power stage. Let us therefore investigate in more detail this particular connection.

3.2 Generic properties of cascade connection of buck and boost converters

When the buck power stage is cascaded by the boost power stage the converter in Fig. 6 is obtained. In Fig. 6 switching action is represented by the ideal switches S_1 and S_2, which can be replaced by bipolar transistors and diodes as in Fig. 1b. Here ideal switches are used to facilitate discussion and enhance the converter topology.

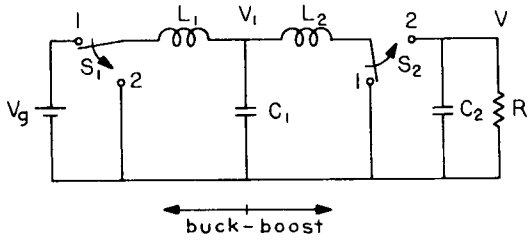

Fig. 6. Buck power stage cascaded by a boost power stage.

Since the emphasis in this and the remaining parts is on the converter topology and *not* on its particular mode of operation, it will be assumed throughout, unless otherwise specified, that all converters operate as two-state converters, hence also in a *continuous conduction mode* (inductor currents never fall to zero). Consequently the switches S_1 and S_2 in Fig. 6 operate synchronously such that only two switched networks are distinguished: one for interval DT_s when both switches are at position 1, and the other for interval $D'T_s \equiv (1 - D)T_s$ when they are at position 2. Also by definition $f_s \triangleq 1/T_s$ is the switching frequency and T_s the switching period. Note that even though the first (buck) power stage does not contain explicitly the load R, it is effectively loaded by the dc input resistance $R_1 = R/M^2$ (M = dc gain of the boost stage) to the second (boost) power stage. The overall dc gain is, of course, the product of the two elementary gains, or $V/V_g = D/(1 - D)$.

An interesting observation about the energy transferring mechanism of the converter in Fig. 6 can now be made. The T-shaped network consisting of storage elements L_1, L_2 and C_1 is, through the switching action, first *completely* switched into the input network (to source voltage V_g), and then during the subsequent interval $D'T_s$ *completely* transferred to the output network thus feeding the load R with the energy stored in the previous interval. Hence in this converter the energy transferring role is assigned to the complete T network (L_1,C_1,L_2) while in the conventional buck-boost this role belonged to the single inductor. We have here, therefore, the case of a mixed energy transferring mechanism consisting of both inductive and capacitive energy storage.

By use of the general modelling technique [3,4], the basic circuit-averaged model of the converter in Fig. 6 is obtained as shown in Fig. 7.

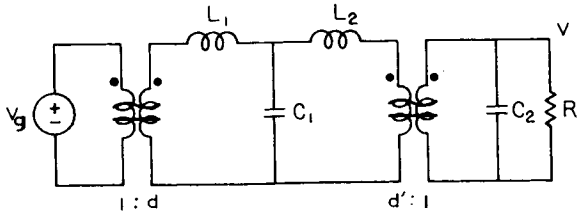

Fig. 7. Basic circuit averaged model for cascade connection of buck and boost converter shown in Fig. 6.

From the circuit model in Fig. 7 the dc conditions are obtained as usual by considering the inductances short and capacitances open, and hence the converter dc gain D/D' and noninverting property are easily established.

Since the capacitance C_1 does not affect the dc conditions, let us now simplify the converter in Fig. 6 by simply taking it out of the circuit (or $C_1 = 0$) to obtain the converter in Fig. 8a.

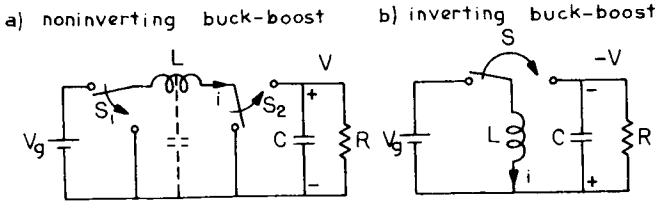

Fig. 8. Reduction of the two switches S_1 and S_2 in the noninverting converter in a) to a single switch S in the corresponding inverting converter (conventional buck-boost) in b).

A significant simplification has been achieved, since the original converter of Fig. 6 with *four* storage elements has been transformed to the converter of Fig. 8a with only two storage elements, and yet the basic dc conversion relations are preserved. The mixed energy transferring network (L_1,C_1,L_2) has been reduced to a single inductance with $L = L_1 + L_2$. This then stresses the importance of *the way* in which the energy storage network is switched between input and output circuits in determining the dc conversion relation, and diminishes the importance of the particular storage element content. In essence, we have achieved the same basic dc conversion function but with a smaller number of storage components (only two) and simpler dynamics, when this special choice ($C_1 = 0$) is used in the general cascade connection of the buck and boost power stages. With this specific choice, the circuit model in Fig. 7 becomes the same as for the conventional buck-boost converter except for the difference in polarity of the second d':1 ideal transformer.

Even though the obtained converter in Fig. 8a is already greatly simplified, let us see if it can be still further reduced. Namely, the converter in Fig. 8a still has *two* switches which in terms of hardware realizations with transistors and diodes means higher switching and dc losses, hence lower efficiency. The important question then becomes how these two switches could be reduced to a single one, and yet the dc conversion properties preserved.

As seen in Fig. 8a inductor L appears to be "floating" and switching action (through S_1 and S_2) periodically grounds one and then the other inductor lead, thus producing an output voltage of positive polarity. If one of the inductor leads is grounded as in Fig. 8b, then single switch S performs the same action as previously S_1 and S_2, except that now inversion of the output voltage is obtained owing to the direction of inductor current. Therefore, if one is willing to sacrifice the noninverting property of the converter in Fig. 8a, the reduction of two switches S_1 and S_2 to a single switch S can be achieved as illustrated in Fig. 8b. In fact, the converter in Fig. 8b is the conventional buck-boost converter of Fig. 1.

This has now brought us to an important conclusion: the conventional buck-boost converter is not an independent circuit, but rather may be considered as a *special case* of the cascade combination of the buck and boost power stage (special case with $C_1 = 0$) in which the inversion of output voltage allowed reduction of the number of switches to one.

Note, however, that this sequence of steps is not to be understood in the usual linear circuits and linear dependence sense. Namely, even though the cascade combination in itself is a linear combination (provided the elementary circuits themselves are linear), the elementary circuits here (buck and boost converters) are extremely nonlinear as also is their cascade connection. However, this difference is alleviated since we are using *linear circuit models* for both dc and ac small-signal models of the converters, as shown in Fig. 7, for example. It is therefore the last step, that of replacing a number of switches for the inverting property of the converter which is highly *nonlinear* (and, of course, cannot be linearized!), which distinguishes this process from the conventional linear equivalent circuit transformation steps, for example. However, despite that, the linear circuit models (both dc and ac small-signal) of the two converters in Fig. 8 are the same (compare the model in Fig. 7 for $C_1 = 0$, with that of the conventional buck-boost [3]), except that one is inverting while the other (Fig. 7) is not.

This may even appear to be a general result (of course assuming that all the switches are ideal, zero on-resistance and infinite off-resistance).

This view of the conventional buck-boost converter as being just a special case of one kind of cascade connection of buck and boost converters, as opposed to the generic view of Section 3.1 and Fig. 5, might seem artificial at present. Nevertheless, this view is later in Section 3.2 shown to be a very *fruitful* one, since it led naturally to the discovery of the new optimum topology switching converter and completion of the general theory of buck-boost converters.

It may seem now that, with the conventional buck-boost converter of Fig. 8b, the ultimate goal of optimum topology (minimum complexity with maximum performance) has been achieved. This is, however, *not so* since the conventional buck-boost converter has two important drawbacks as demonstrated in Section 2 and illustrated in Fig. 2. Its *input current* is *pulsating*, which causes severe EMI (electromagnetic interference) problems, while its *pulsating output current* produces a significantly larger output voltage ripple compared, for example, to the buck power stage (which has continuous, nonpulsating output current): This was to be expected, since at the very beginning (Fig. 6) we combined only the *undesirable* properties of the two original converters, the pulsating input current of the buck converter with the pulsating output current of the boost converter.

However, with maximization of the performance in mind, we can easily alleviate these problems by putting the *boost* power stage *first*, and then cascading it by the *buck* power stage as shown in Fig. 9. In this way, the same dc conversion function is produced, but now the *desirable* properties of the two elementary converters are combined: the *continuous input current* of the boost converter and the *continuous output current* of the buck converter.

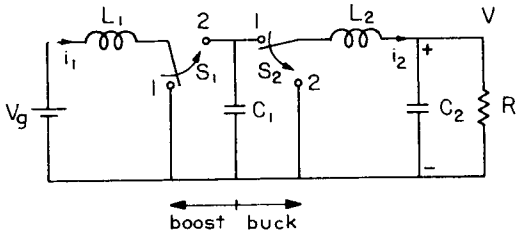

Fig. 9. Boost power stage cascaded by a buck power stage.

This converter will be referred to as a boost-buck non-inverting converter, in distinction to the converter of Fig. 6 which will be termed the buck-boost noninverting converter.

Let us now see how the energy transferring mechanism is affected by this particular choice of cascade connection. As seen in Fig. 9 the switches S_1 and S_2 are now embedded inside the T-shaped network consisting of L_1, L_2, and C_1, while in the buck-boost configuration (Fig. 6) they are outside of this T network of storage elements. It now becomes obvious that the capacitance C_1 is *the only* energy transferring device. Namely, during the interval $D'T_s$ the capacitance C_1 enters the input circuit (series connection of source voltage and inductance L_1) and accumulates energy in the form of stored charge. For the subsequent interval DT_s, capacitance C_1 is completely transferred to the output circuit to which it then releases the energy stored in the previous interval. Therefore, in distinction with the previous two cases, we have now a purely capacitive energy transfer, since a *single capacitance* has taken the role of the energy transferring network, as did the *single inductance* in the conventional buck-boost converter employing purely inductive energy transfer.

It is now clear that we cannot simplify the energy transferring network in this case, (as we did for the buck converter cascaded by the boost converter (Fig. 8), since it is *already* in the simplest possible form, consisting of a single storage element, capacitance C_1. Therefore we cannot reduce the number of storage elements as we could before and all *four* storage elements are necessary.

However, one *fundamental question* still remains to be answered for this favorable cascade connection:

Is it possible to reduce the number of switches in the converter of Fig. 9 from two to one, and at the same time achieve inversion of the output dc voltage?

The answer to this question may be surprising, since it is affirmative as will now be demonstrated. The same question, when slightly rephrased, leads easily to the answer: we ask what actually should be done in the converter of Fig. 9 to cause inversion of output dc voltage. Both boost and buck power stages are by themselves inherently noninverting and therefore *the only way* the output voltage could be inverted is that the switching action causes the polarity of the energy transferring capacitance C_1 to be inverted when presented to the output (buck) circuit, and then inverted back to positive polarity when in the input (boost) circuit. Therefore, if we concentrate only on the capacitance C_1 and the two switches S_1 and S_2 in the converter of Fig. 9, we quickly realize that the stated goal can easily be obtained as shown in Fig. 10.

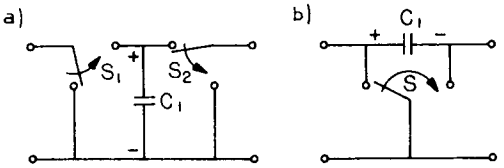

Fig. 10. Topological reduction of the number of switches: a) two switches and noninversion of capacitance voltage; b) single switch and inversion of capacitance voltage.

Hence, at the same time that the voltage polarity inversion of the capacitance C_1 is obtained, the reduction of the two switches S_1 and S_2 in Fig. 10a to a single switch S in Fig. 10b has been achieved.

In this capacitive energy transfer, the originally grounded capacitance C_1 and the two switches (Fig. 10a) have been transformed into the "floating" capacitance C_1 and single switch S (Fig. 10b), which periodically grounds one and then the other end of the capacitance. Note, however, that the opposite is true for the inductive energy transfer configuration in Fig. 8. There, the originally "floating" inductance with two switches (Fig. 8a) is transformed into a grounded inductance with a single switch (Fig. 8b). This comparison can be carried even further. For inductive energy transfer, inversion of the *inductor current* (but not the polarity of the inductor) is necessary to achieve output voltage inversion (Fig. 8), while for capacitive energy transfer, inversion of the *capacitor voltage* is necessary to realize the same goal. Furthermore the

capacitance C_1 and switch S in Fig. 10b can be considered to be *in parallel*, while in Fig. 8b the inductance L and switch S are in series. A general principle, the *dual nature* of the two storage elements, capacitors and inductors, and even the duality of the accompanying switching network, has been once again confirmed on the example of Fig. 8 and Fig. 10.

Let us now introduce the topological transformation of Fig. 10 into the converter of Fig. 9 to obtain finally, the *new switching converter* shown in Fig. 11.

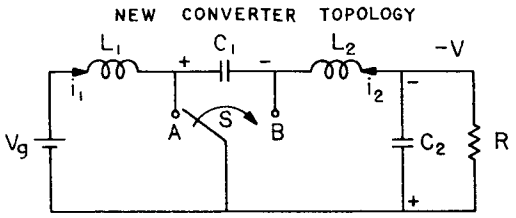

Fig. 11. The new switching topology, employing capacitive energy transfer and independent of any particular hardware realization of the switch S.

A closer look at the interconnection of the storage elements in this new converter (Fig. 11) might for a moment cause a concern that the *low-pass* nature of the storage element interconnections postulated for the generalized switching converter and represented by the low pass filter network in Fig. 3 is being violated here. However, this is not so, even though the capacitance C_1 appears in a series branch (in series with inductances L_1 and L_2) because it *effectively acts* as a *parallel branch* either in the input circuit (for interval $D'T_s$) or in the output circuit (for interval DT_s). This is further confirmed later, by the canonical circuit model (Fig. 21) of this new converter, which clearly exhibits low-pass nature, or by the experimental converter which *does* perform the basic dc conversion function.

The representation of the new converter topology in Fig. 11 with the ideal switch S is essential, since it is independent of any particular realization of switch S. However, for practical implementation, nonideal hardware realization of the switch is used. Let us now investigate one such practical converter realization.

3.3 Physical realization and basic operation of the new converter

We now pose the task of implementing the switch S in Fig. 11 by a bipolar transistor and diode combination in a way analogous to that used in Fig. 1 for the three common power stages. The transistor is once again used in the switching mode, and the diode is used to supplement its switching action and in turn works in synchronism with it: when the transistor is on, the diode is off, and vice versa. It is, then, now not difficult to see that the switch S in Fig. 11 can be substituted by the bipolar transistor and diode combination as shown in Fig. 12.

Let us now describe the operation of the circuit in Fig. 12. During the interval $D'T_s \equiv (1 - D)T_s$ when the transistor is off, the diode is forward biased and capacitance C_1 is charging in the positive direction as seen in Fig. 13b (switched network for interval $D'T_s$ assuming negligible diode drop). The collector-to-emitter voltage of the transistor is therefore positive, and it can be turned on for the subsequent interval DT_s.

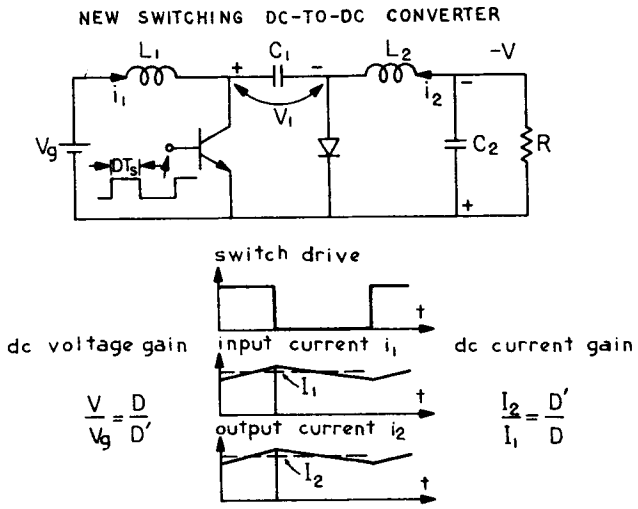

Fig. 12. Hardware realization of the new switching converter using a bipolar transistor and diode to replace switch S in Fig. 11.

However, as soon as it turns on, capacitance C_1 becomes connected across the diode, thus reverse-biasing and effectively disconnecting it from the circuit as in Fig. 13a (switched network for interval DT_s assuming negligible saturation voltage of the transistor). During this interval DT_s, the capacitance C_1 discharges through the load R and inductance L_2, thus charging the output capacitance to a negative voltage as shown in Fig. 13a. Finally, to close the complete cycle, when the transistor again turns off, the diode conducts again, thus providing the path for current i_2 to charge the output capacitor C_2, using stored energy in the inductance L_2 as the energy source. This is the reason why this converter, owing to its continuous output current (Fig. 12), has inherently much smaller switching ripple than the converters with pulsating output current (such as the boost or buck-boost converters of Fig. 1).

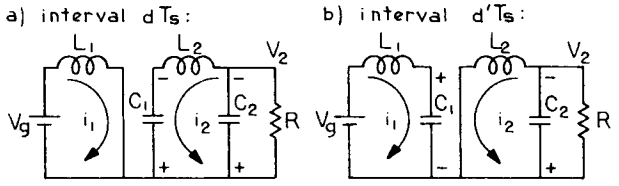

Fig. 13. Two switched circuit models of the new converter.

The synchronous action of the transistor and diode can be compared with a *see-saw*. Namely, when the transistor is turning on, it is *pulling down* the capacitor end (potential) on its side, while at the same time *pulling up* (in magnitude) the other capacitor end (on the diode side). The opposite is true when the transistor is turning off. Thus, owing to this automatic see-saw action, the danger in having both transistor and diode on at the same time is eliminated. Note also that the symmetry does not hold any more, and that interchange of the diode and transistor in Fig. 12 would not function in the required see-saw manner.

Even though the new converter in Fig. 12 contains only one transistor switch, Figs. 12 and 13 reveal how it effectively behaves as a cascade combination of a boost stage followed by a buck power stage, in which

output voltage inversion is obtained at the same time. The energy transferring capacitance C_1 plays a double role: it is the output capacitance of the input boost-like circuit (consisting of transistor, V_g, L_1, C_1 and diode) and also the negative voltage supply to the second stage (consisting of diode, C_1, L_2, C_2, and R) which acts as a buck power stage. The same is true for the diode D, which performs the function of the diode in both power stages.

It looks as though during the interval DT_s, the *second nonexistent transistor switch* of the buck power stage connected the voltage source (here capacitance C_1) to its L_2, C_2 filter and load R, while at the same time the real transistor switch connected inductance L_1 to ground as is usual in a boost converter. Then, during the next interval, it looks as though the nonexistent transistor switch of the buck power stage turned off, thus disconnecting the voltage source (capacitance C_1) from its L_2, C_2 filter and connecting L_2 through the diode to ground as is always the case in a buck power stage. It appears as though two switches are functioning, even though in reality only a single transistor and diode are used. This is probably why, owing to this merging of functions, it is not easy to recognize directly from Fig. 12 that the new converter is effectively working as a cascade of boost and buck converters. As a matter of fact, the canonical circuit model in Section 4.1 will confirm that the new converter has, except for the inversion, the same dc and dynamic (ac small-signal) properties as does the converter in Fig. 9 (assuming of course ideal transistors and diodes).

Let us now, before the extensive theoretical and experimental comparison with other converters in the next Sections, review first some of the outstanding features and advantages of the new converter that are immediately apparent.

3.4 Advantages of the new optimum topology converter

As seen in Fig. 12, this converter employs a *new circuit topology* which enables it to have both input and output current continuous. Hence, none of the problems present in the conventional converters (buck, boost, buck-boost) due to pulsating of either input or output current (or both) are present in the new converter. The new converter actually combines the desirable input properties of the boost power stage and the desirable output properties of the buck power stage (without acquiring any of their undesirable properties), and yet performs the general conversion function (increase or decrease of input voltage) of a conventional buck-boost power stage with considerably higher efficiency, as will be proven in the next Section.

Even though there is no such thing as a dc-to-dc transformer (not physically realizable), the new converter can be *functionally* considered as a true dc-to-dc transformer, since both its input and output voltages and *currents* are very close to true dc quantities, owing to the negligible switching ripple.

The new converter uses *capacitive energy transfer*, which will be shown later in Section 3.5 to have much better energy storage and transfer capabilities than the conventional inductive energy transfer mechanism.

So far these were the same advantages brought by the favorable cascade connnection of a boost followed by a buck converter (see Fig. 9 also). However, the new converter of Fig. 12 has a number of additional advantages over it. First, the number of switching components has been cut in half (one transistor and diode less). This immediately eliminates the need for the additional "floating" drive circuitry for the buck part of the converter in Fig. 9, and leaves only the transistor referred to ground in Fig. 12 which does not need any special "floating" drive circuitry. Moreover, the switching losses, which represent an important part of the overall losses, are cut in half in the new converter, hence boosting the efficiency of the converter operation significantly. Hence the switching losses in the new converter become even equal to or lower than (as demonstrated in the next section) the losses in the single-switch converters of Fig. 1.

Once again, the new converter of Fig. 12 has acquired a desirable property of the boost converter in not requiring special drive circuitry, since its transistor is with grounded emitter, and not the unfavorable one of buck and conventional buck-boost converters in requiring "floating" drive circuitry.

From the analysis in Section 2, it follows that the continuous input and output currents are the most desirable characteristics, and lead alone to outstanding converter performance. Thus, the following conclusion can be made.

The new dc-to-dc converter (Fig. 11 or 12) has an optimum topology (maximum performance for the minumum number of components). Namely, to have both input and output current continuous, one needs two inductances, one in series with the input source, the other in series with the load. To obtain a dc level conversion, an energy transferring network with storage capabilities must be used. Here it is a single capacitance. To enable it to serve as an energy transferring device, at least one switch is necessary. Here it is the single switch S in Fig. 11 or the bipolar transistor and diode combination in Fig. 12. Finally, an output capacitance, even though not essential for proper operation of the converter, is put across the load further to reduce output voltage ripple.

It is rather surprising that just this new optimum topology switching converter (Fig. 11 or Fig. 12) was the only one missing in the complete structure of the buck-boost converters. Let us therefore now review the structure of all converters performing the buck-boost function and generated by two different cascade connections of basic buck and boost power stages, and include the new converter.

3.5 General theory of buck-boost converters

With the invention of the new converter, the previously incomplete picture of buck-boost and boost-buck switching converters can be completed as shown in Fig. 14.

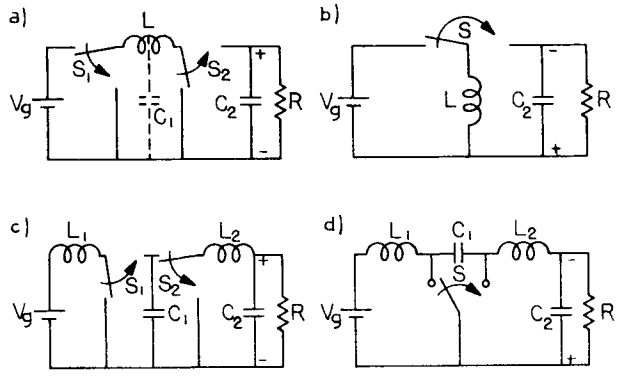

Fig. 14. Complete topological structure of buck-boost and boost-buck converters: a) buck-boost noninverting; b) buck-boost inverting; c) boost-buck noninverting; d) boost-buck inverting (new converter).

Fig. 14 shows all four possible different topologies to realize the buck-boost function, either in noninverting or in the inverting form. The new converter in Fig. 14d has filled in the gap previously existing, and has completed the topological view of these converters.

A useful summary of the three possible energy transferring mechanisms is also transparent in Fig. 14, which shows mixed energy transfer employing both inductive and capacitive energy transfer (Fig. 14a with $C_1 \neq 0$), purely inductive (Fig. 14a with $C_1 = 0$ and Fig. 14b) or purely capacitive (Fig. 14c and d).

It now becomes apparent that for achieving the general dc conversion function, the particular storage-element content of the energy transferring network is not so important as the *way* the complete network is switched between input and output circuits: being *completely* in the input circuit during one interval (DT_s), and then *completely* in the output circuit during the subsequent interval. Hence, ideally at no time is it connecting the input and output circuits. This is in clear distinction with the ordinary buck and boost power stages in which the energy transferring network *connects* the input and output circuits for a portion of the switching period.

It seems now appropriate to compare the inductive energy transfer principle which is used in all so far known converters (such as the Weinberg, Venable, and a number of others), with the *capacitive energy transfer* first encountered in the boost-buck converter of Fig. 9 and the new converter of Fig. 11. While in the first kind the energy is accumulated in the inductor in the form of a magnetic field, in the second the energy is stored on the capacitor in the form of an electric field. We can now compare easily their storage capabilities. Electrostatic energy stored in capacitance C with voltage V is $E_c = CV^2/2$, while the electromagnetic energy stored in inductor L with current I is $E_L = LI^2/2$. For example, for C = 1μF and V = 50V, E_c = 1.25mJ, while for L = 2.5mH and I = 1A, it is also E_L = 1.25mJ. However, the physical size and weight of a 1μF, 50V capacitor are negligible compared to those of a 2.5mH, 1A inductor. Therefore, capacitive energy storage has much better storage capability per unit size or weight than does inductive energy storage. This becomes of prime importance for switching converters, since their weight and size reduction is sometimes the primary goal (aerospace applications, for example).

Comparison of the complexity of these converters shows those with inductive energy transfer to be of second-order (two storage elements), while those based on capacitive energy transfer are of the fourth order (four storage elements). Nevertheless, their higher complexity is outweighed by their superior performance, since the converters in Fig. 14a and b require at least one section of input L,C filter and still have a much worse output characteristic because of pulsating output current (as discussed in Section 2 and in the extensive comparison of Section *5*).

Since the resulting dc and ac small-signal circuit models of all the converters in Fig. 14 are *linear* models, a close analogy with linear vector fields can be made as shown in Fig. 15, which also emphasizes the generic properties of the cascade connection of buck and boost converters.

As seen in Fig. 15, the basic buck and boost converters are considered as abstract entities: the elementary vectors are defined along coordinates representing the first and second stage of the cascade connection. Then, the noninverting converters (buck-boost and boost-buck) of Fig. 14a and Fig. 14c are obtained

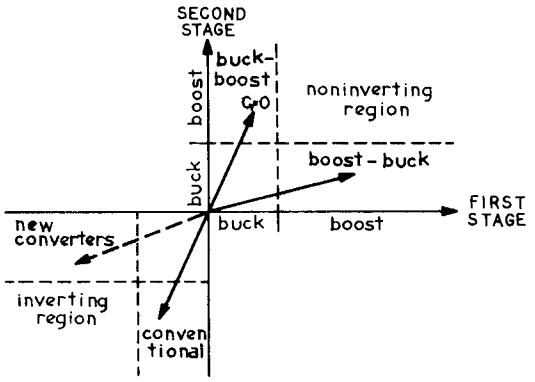

Fig. 15. Linear vector analogy of the generation of converters in Fig. 14 by cascading the basic buck and boost converters.

as their linear combination, while the corresponding inverting converters (Fig. 14b and Fig. 14d) are defined as vectors of the same magnitude but opposite sign (direction), thus in the third quadrant on Fig. 15. In particular, a previously missing link establishing the new converters of Fig. 14d is shown in Fig. 15 by a dotted line vector.

Note, however, that this analogy even becomes accurate if the *converter models*, instead of the converters themselves, are considered as abstract vectors in Fig. 15. Namely, both inverting converters (Fig. 14b and d)have the *same dc and dynamic (ac small-signal) models* as their noninverting counterparts, except for the inversion property. The same fact is clearly marked on Fig. 15 in having the same *magnitude* but *opposite sign*, for their abstract representations. The fact that the new converter (Fig. 14d) has the same dc and dynamic properties as its counterpart (Fig. 14c) except for the inversion property is demonstrated later in Section *4.1*.

The region defining the general buck-boost function in Fig. 15 is shown shaded. The remaining unshaded region in the first quadrant defines specialized functions: buck (obtained by buck-buck cascade connection) and boost (obtained by boost-boost cascade connection). Besides their special function, they also *do not have* their corresponding inverting counterparts as does the buck-boost connection. For these and some other combinations to be practically useful, they have to be related to a rather specialized problem. Just recently and concurrently with this work, such cascade connections have been studied for the first time, [9] and [10], but in a quite different context, in connection with one specialized problem — reduction of the surge current in switching regulators for color television applications.

3.6 Correlation among buck, boost and new converter topologies

We now recall that the three common converters (buck, boost and buck-boost) of Fig. 1 may be considered as generated by cyclic rotation of the series connection of the energy transferring inductance L and a single-pole double-throw switch S, between input (source) and output (load) circuit, as was explained in Section 3.1 and shown in Fig. 5.

Let us now find a similar interpretation for the generation of the new converter topology, along with that for the two basic converters, the buck and the boost. But in distinction with the previous method, and in order to enhance common features of the latter

three converters, we now look at: the buck converter with input filter, the boost converter with output filter, and the new converter, as shown in Fig. 16.

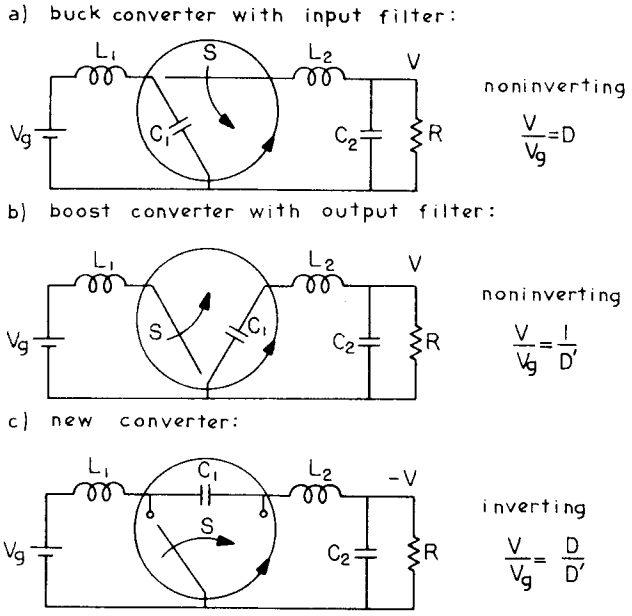

Fig. 16. Generation of the three converters: buck with input filter, boost with output filter, and new converter by cyclic rotation of the parallel connection of capacitance C and switch S.

It now becomes apparent that all three converters in Fig. 16 may be generated by cyclic rotation (counterclockwise) of the *parallel* connection of *capacitance* C_1 and single-pole double-throw *switch* S between the input circuit (now consisting of a voltage source in series with inductance L_1) and the output circuit (now consisting of inductance L_2 in series with load R). Once again the striking dual nature of the two generating procedures becomes transparent: the cyclic rotation of the *series* combination of inductance and switch is substituted here by the *parallel* combination of the capacitance C_1 and switch S.

When comparing the new converter with the buck or boost converter, it seems appropriate to make the comparison with their versions in Figs. 16a and 16b. This way, all three converters in Fig. 16 have the same number of storage elements (four), and similar performance characteristics in that both input and output currents are nonpulsating. However, the new converter is still superior in that it is capable of both increasing and decreasing the input dc voltage, while the other two converters are not. In a practical realization with a transistor and diode, there could be some additional advantages. For example, the buck converter, unlike the new converter, needs special drive circuitry, and the boost converter may have less favorable frequency response than the new converter.

In addition to these advantages, some useful extensions [6] are applicable only to the unique topology of the new converter. For example, coupling of the inductors in the new converter substantially reduces both the output current and voltage switching ripple [6], but such coupling is *not feasible* for the other two converters in Fig. 16a and b. Similarly, the new converter topology permits a hardware realization of switch S such that both positive and negative regulator functions are obtained in a single unit [6], a feature not present in any other switching dc-to-dc converter. Moreover, the desirable properties of isolation and multiple outputs can be directly incorporated into the unique structure of the new converter [7], while in the buck or boost this is not possible by such simple means.

Because of the general dc conversion property (increase or decrease of input dc voltage), it is appropriate to compare the new converter (Fig. 16c) with the conventional buck-boost converter (Fig. 8b) to which an input LC filter has been added. Then, both converters have the same number of storage elements (four) and switches, and possess a nonpulsating input current. The detailed comparison of Section 5, however, shows that the new converter, for the same storage elements and switching components, leads to the significantly higher efficiency and smaller switching ripple owing to its *optimum interconnection* of the components.

The representation of the converters in Fig. 5 and Fig. 16 provide an interesting correlation among the generation of the buck, boost, conventional buck-boost, and the new converter topologies. However, a slightly different topological view of the converters of Fig. 5 and Fig. 16, shown in Figs. 17 and 18 respectively, still calls for further revision of the look at the two "*basic*" converters, the buck and the boost converter, initiated earlier in Section 3.1.

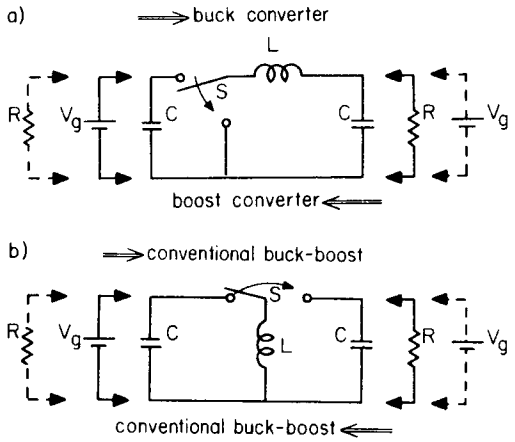

Fig. 17. Bidirectional view of the converters of Fig. 5: a) both buck and boost function originate from single topology; b) conventional buck-boost is symmetrical both topologically and functionally.

As seen in Fig. 17a, there is only *one basic* converter topology, which realizes either the buck or the boost *function* depending upon where the input is applied and the output taken (heavy line: buck function; dotted line: boost function). The particular hardware realization of the switch S, by use of the bipolar transistor and diode combination, differs in function in the two directions. Hence, the importance of the structural representation in Fig. 17a via ideal switch S.

This now explains why the cascade connection of the buck and boost converters in Fig. 6, and its derivative, the conventional buck-boost converter of Fig. 17b, are symmetrical topologies having the same general dc conversion function in both directions. Namely, in the converter of Fig. 6, the output boost stage is actually working as an input buck stage in the opposite direction. Similarly, its input buck stage becomes an output boost stage in the opposite direction.

In an analogous manner, the *single* topology of Fig. 18a leads to the buck converter with input filter in one direction (heavy lines) and to a boost converter with output filter (dotted lines) in the other direction. Again in the new converter of Fig. 18b, the output buck-like circuit becomes an input boost-like converter in the opposite direction, thus producing the same general dc conversion function and resulting in the symmetrical topology. The same is, of course, also true for the straightforward cascade connection of a boost converter followed by a buck of Fig. 9.

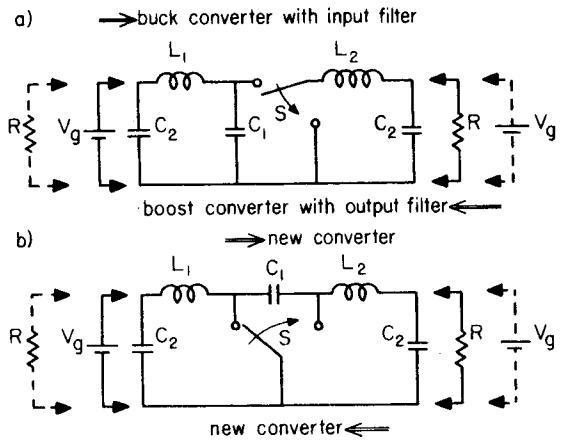

Fig. 18. Bidirectional view of the converters of Fig. 16: a) buck converter with input filter and boost converter with output filter originate from single topology; b) new converter is symmetrical both topologically and functionally.

Thus, an important conclusion can be made: there is only one single switching converter topology, that of Fig. 17a, which is the foundation for the development of other *basic* converters: buck, boost, conventional buck-boost and new optimum topology switching converters.

4 MODELLING AND EXPERIMENTAL VERIFICATION OF THE NEW SWITCHING CONVERTER

In order experimentally to verify both steady state (dc) and dynamic (ac small-signal) properties of the new switching converter, equivalent circuit models and particularly the canonical circuit model of Fig. 3 are developed first, following the general method of modelling described in [2,3,4].

4.1 Modelling and analysis of the new switching converter

By use of the two switched circuit models for the new converter (Fig. 13) and the hybrid modelling or the circuit averaging technique for the continuous conduction mode [2,3,4], the basic circuit averaged model of the new converter results as shown in Fig. 19.

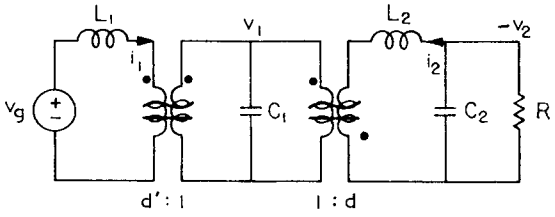

Fig. 19. Basic circuit averaged model of the new switching converter

The usual perturbation and linearization steps [2,3] lead to the linear circuit model (both dc and ac small-signal) in Fig. 20.

From the circuit model in Fig. 20 one can easily obtain the complete dc relations as

$$\frac{V_2}{V_g} = \frac{D}{D'}, \quad \frac{V_2}{V_1} = D, \quad \frac{I_2}{I_1} = \frac{D'}{D}, \quad \frac{V_2}{I_2} = R \qquad (1)$$

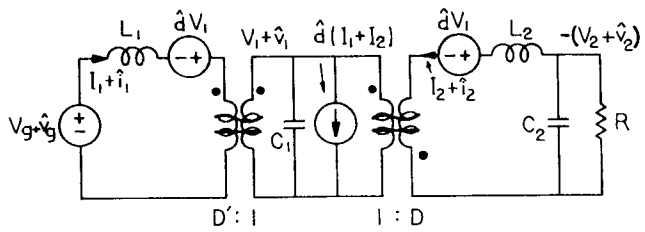

Fig. 20. Linear circuit model (both dc and ac small-signal) of the new switching converter in Fig. 11.

By use of the equivalent circuit transformations and with help of dc relations (1), the circuit model of Fig. 20 can be transformed into the canonical circuit form shown in Fig. 21.

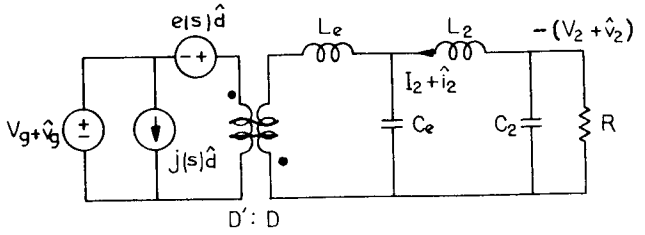

Fig. 21. Canonical circuit model of the new switching converter in Fig. 11 with none of the parasitic elements included.

The element values in Fig. 21 are defined as

$$L_e = \left(\frac{D}{D'}\right)^2 L_1; \qquad C_e = \frac{C_1}{D^2} \qquad (2)$$

$$e(s) = \frac{V_2}{D^2}\left(1 - s\frac{L_e}{R} + s^2 L_e C_e D'\right) \qquad (3)$$

$$j(s) = \frac{V_2}{D'^2 R}\left(1 - sC_e R D'\right) \qquad (4)$$

Let us now discuss the significance of this result. First, the effective filter network $H_e(s)$ postulated in Fig. 3 consists now of *two low-pass* LC filter sections, whose element values are now duty ratio dependent as seen in (2). It demonstrates that the effective filter network is of *low-pass* nature (even though capacitance C_1 appeared to be in series in the new converter of Fig. 11) as required to pass the basic dc signal, and that it could be of higher order (not only of order two as in canonical models of the converters in Fig. 1).

Second, *for the first time* a frequency dependence appears in the current generator $j(s)\hat{d}$ (4) of the canonical circuit model (Fig. 20), while the voltage generator $e(s)\hat{d}$ (3) exhibits a *second-order* frequency dependence in contrast to the first-order dependence in a number of other converters [2,3]. Both of these results, (3) and (4), directly confirm the general modelling predictions made earlier [3] by use of canonical circuit model formulas. In fact, the canonical circuit model of Fig. 21 could have been obtained *directly* by use of only these formulas and the state-space description of two switched networks in Fig. 13 as demonstrated in [2].

Note that the boost-buck noninverting converter of Fig. 9 would result in the same model given by Fig. 21 and equations (1) through (4) except for the noninverting polarity of the transformer in its model. Thus, assuming negligible effect of the nonidealities of the transistor, switches, and diodes used in their hardware realization, the same steady state (dc) and dynamic (ac) response would be obtained.

In order to determine the frequency response, $H_e(s)$ and $e(s)$ are needed to find the open-loop line to output and duty ratio to output transfer functions $G_{vg} \triangleq \hat{v}_2/\hat{v}_g$ and $G_{vd} \triangleq \hat{v}_2/\hat{d}$. By use of either the general formulas [2,3] or from the circuit model in Fig. 21, we obtain

$$H_e(s) = \frac{1}{P(s)} \tag{5}$$

where

$$P(s) = 1 + \frac{L_e+L_2}{R}s + (L_eC_e+L_2C_2+L_eC_2)s^2 + \frac{C_eL_eL_2}{R}s^3 + L_eC_eL_2C_2s^4 \tag{6}$$

It is now of some practical interest (as will be demonstrated on the experimental test circuit) to find what conditions should be satisfied that this 4th order polynomial can be *analytically* separated in terms of two second-order polynomials.

Suppose that $P(s)$ is approximated by the product of two second order polynomials as

$$P(s) = (1 + \frac{L_e}{R}s + L_eC_es^2)(1 + \frac{L_2}{R}s + L_2C_2s^2) \tag{7}$$

Comparison of (6) and (7) reveals that (6) is well approximated by (7) if the following inequality conditions are satisfied

$$C_e >> C_2$$
$$C_e >> L_2/R^2 \tag{8}$$

If, in addition, the inductances L_e and L_2 are of the same order of magnitude, the two pairs of complex poles of $H_e(s)$ resulting from (7) are *well separated*, with their respective corner frequencies and Q factors given by

$$f_{c1} = \frac{1}{2\pi\sqrt{L_eC_e}}, \quad Q_1 = \frac{R}{\omega_{c1}L_e}$$
$$f_{c2} = \frac{1}{2\pi\sqrt{L_2C_2}}, \quad Q_2 = \frac{R}{\omega_{c2}L_2} \tag{9}$$

Therefore, if the conditions (8) are met, the frequency response of the open-loop transfer functions G_{vg} can easily be sketched by inspection with the help of (9), since the two pairs of complex poles of (5) are well separated.

Note that the switching action now introduces into the duty ratio to output transfer function G_{vd} a pair of complex zeros given by (3), in addition to the poles of the effective filter network $H_e(s)$ given by (7), since $G_{vd}(s) = e(s)\, G_{vg}(s)$. Moreover, the complex zeros are in the *right half-plane*, owing to the *negative* linear term in s in e(s) given by (3). This should be compared with the single real *right half-plane* zero for the conventional buck-boost converter (see [2,3] for example).

As discussed in [2,3], even only a single right half-plane zero (nonminimum phase network) poses significant problems in stabilizing the loop gain T, which directly depends on this open-loop transfer function $G_{vd}(s)$. Then, the complex pair in the right half-plane would even more exaggerate this problem.

Nevertheless, for practical applications the situation is not so unfavorable as it may look at first sight. Namely, in the model of Fig. 21 the inductances have been considered ideal, and their parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ which are always associated with them have not been included. These parasitic resistances, however, being *the only dissipative elements* besides the load R, can significantly affect converter properties. They can have a profound effect upon the dc properties and also a stabilizing effect upon the ac properties, as will be demonstrated.

Inclusion of the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ is easily made in the previously outlined modelling procedure, and leads to the canonical circuit model of Fig. 22.

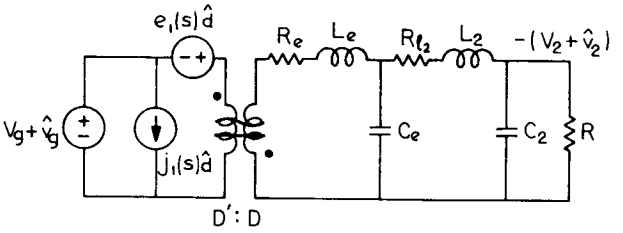

Fig. 22. Canonical circuit model of the new switching converter in Fig. 11 with the series parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ of the two inductors included.

The element values in Fig. 22 are defined as

$$R_e = \left(\frac{D}{D'}\right)^2 R_{\ell 1}, \quad L_e = \left(\frac{D}{D'}\right)^2 L_1, \quad C_e = \frac{C_1}{D^2} \tag{10}$$

$$e_1(s) = \frac{V_2}{D^2}\left\{1 + \frac{R_{\ell 2}-R_e}{R} - s\left[\frac{L_e}{R} - R_eC_eD'\left(1 + \frac{R_{\ell 2}}{R}\right)\right] + s^2L_eC_eD'\left(1 + \frac{R_{\ell 2}}{R}\right)\right\} \tag{11}$$

$$j_1(s) = \frac{V_2}{D'^2R}\left[1 - s\, C_eRD'\left(1 + \frac{R_{\ell 2}}{R}\right)\right] \tag{12}$$

From the circuit model in Fig. 22 and by use of (10) the dc voltage gain, which now includes the effect of parasitics, is obtained as

$$\frac{V_2}{V_g} = \frac{D}{D'}\,\frac{1}{1 + \frac{R_{\ell 1}}{R}\left(\frac{D}{D'}\right)^2 + \frac{R_{\ell 2}}{R}} \tag{13}$$

while similarly as before, the dc current gain is not affected and remains

$$\frac{I_2}{I_g} = \frac{D'}{D} \tag{14}$$

thus leading to the efficiency η defined by

$$\eta = \frac{1}{1 + \frac{R_{\ell 1}}{R}\left(\frac{D}{D'}\right)^2 + \frac{R_{\ell 2}}{R}} \tag{15}$$

Let us now examine more closely what consequences the inclusion of parasitics has upon the frequency response. Since the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ are in reality small compared to the load R, that is

$$R_{\ell 1} << R, \qquad R_{\ell 2} << R \tag{16}$$

their effect upon the position of the two corner frequencies f_{c1} and f_{c2} is negligible and they are still very accurately predicted by (9). However, their Q factors will be appreciably affected. The same is true for the numerator polynomial $e_1(s)$ which is under (16) approximated by

$$e_1(s) = \frac{V_2}{D^2}\left[1 - s\left(\frac{L_e}{R} - R_e C_e D'\right) + s^2 L_e C_e D'\right] \tag{17}$$

As seen from (17) two complex zeros of $e_1(s)$ can now become *left half-plane* zeros if the following condition is met:

$$\frac{L_e}{R} - R_e C_e D' < 0 \tag{18}$$

Therefore, owing to the corrective term $R_e C_e D'$ originating from the parasitic resistance $R_{\ell 1}$, the frequency response may be *qualitatively* changed to a *minimum phase* frequency response and stabilization problems substantially reduced. This is, however, what should have been expected, since the input series resistance $R_{\ell 1}$ effectively adds more damping to the converter.

As before, the corner frequency remains virtually unaffected and the same as in (3), that is

$$f_{z1} = \frac{1}{2\pi\sqrt{L_e C_e D'}} \tag{19}$$

Comparison of (19) and (9) now shows that complex zeros at f_{z1} almost completely cancel the influence of complex poles at f_{c1}, since they are very little separated ($f_{z1} = f_{c1}/\sqrt{D'}$), thus giving a second-order response with effective complex poles at f_{c2} for the G_{vd} transfer function (see computer generated graph in Fig. 26). Note also that the first pole at f_{c1} is dependent on duty ratio D, since $L_e C_e = L_1 C_1 / D'^2$, while the pole at f_{c2} is not.

Therefore, once again it is confirmed that the new switching converter (Fig. 11) has acquired the desirable dynamic properties of the buck converter in having second-order behavior with corner frequency $f_{c2} = 1/2\pi\sqrt{L_2 C_2}$ *independent* of duty ratio D, and in not having any *right half-plane zeros* as do the boost and buck-boost converters. Nevertheless, the line to output transfer function is still of the fourth order (Fig. 25) giving an excellent audio-susceptibility characteristic. Thus, the new converter has a very desirable frequency response, which is easy to stabilize once the feedback loop is closed in switching regulator applications.

Let us now confirm these theoretical analytical predictions with exact computer generated dc gain and frequency plots, and with experimental data obtained from the test circuit.

4.2 Experimental verification of the modelling predictions

A new switching converter (Figs. 11 and 12) was constructed as shown in Fig. 23 with the following switching elements: transistor D44H10 and diode TRW PD9050. Since series parasitic resistances have been shown to have a profound effect upon the converter characteristics, they are measured and included in the model (and circuit description in Fig. 23 as well).

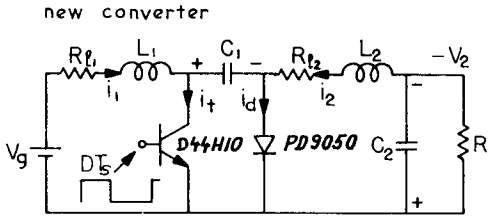

Fig. 23. Experimental test circuit for the new switching converter of Figs. 11 and 12.

For purposes of experimental verification the following values were used:

$$V_g = 5V, \quad R_{\ell 1} = 1.0\Omega, \quad L_1 = 3.5mH,$$
$$C_1 = 100\mu F, \quad f_s = 40kHz \quad R_{\ell 2} = 0.4\Omega, \tag{20}$$
$$L_2 = 6.5mH, \quad C_2 = 0.47\mu F, \quad R = 75\Omega$$

Note that for these experimental values, the converter operates in the continuous conduction mode (for the range of duty ratios D involved), as can easily be checked using the results in [5]. Hence it will behave as a two-state converter, and the modelling results developed directly apply.

DC gain measurements

First, the dc conditions are verified. By use of experimental values (20) in (13), the dc voltage gain is plotted as a function of duty ratio D as shown in Fig. 24. As seen in Fig. 24, the experimental data for the dc voltage gain measured on the circuit of Fig. 23 are in good agreement with the theoretical predictions.

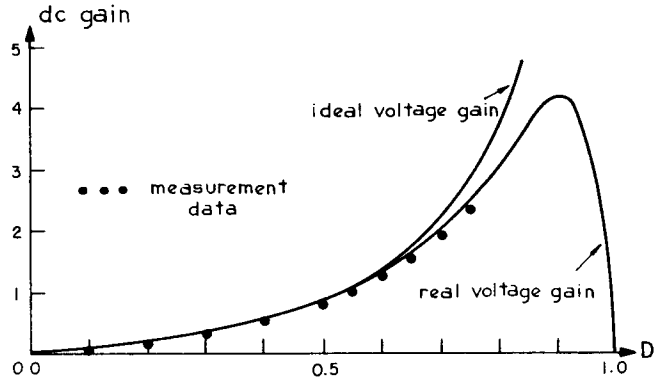

Fig. 24. Theoretical and experimental dc gain characteristics of the boost-buck converter of Fig. 23.

Another verification, of the dc voltage V_1 of the energy transferring capacitance C_1, confirmed that it does change according to $V_1/V_g = 1/D'$, or the same as the gain of the boost converter. This confirms that capacitance C_1 is indeed to be considered as the output capacitance of the boost converter, a fact which may not be so obvious from the converter circuit in Fig. 12.

Frequency response measurements

For ac small-signal frequency measurements, the steady-state operating point was chosen to be at $D = 0.5$. With this and definitions (1), inequality conditions (8) become $400\mu F >> 0.47\mu F$ and $400\mu F >> 1.15\mu F$ respectively, and are well satisfied. Hence the two pairs of complex poles are *well-separated* and can be calculated from (9) as

$$f_{c1} = 133\text{Hz}, \qquad f_{c2} = 2.8\text{kHz} \tag{21}$$

The condition (18) for complex zeros to be in the *left half-plane* is also satisfied since $L_e/R - R_e C_e D' = -154\mu\text{sec}$ is negative, and its corner frequency f_{z1} given by (19) becomes

$$f_{z1} = 190\text{Hz} \tag{22}$$

The computer program NEW was used to generate the exact frequency response for the line transfer function G_{vg} obtained from Fig. 22, and is plotted in Fig. 25 for the experimental values (20). As seen in Fig. 25, the two pairs of complex poles are *well-separated* (more than a decade apart) and the corner frequencies obtained from the plot agree very well with their computed estimates (21).

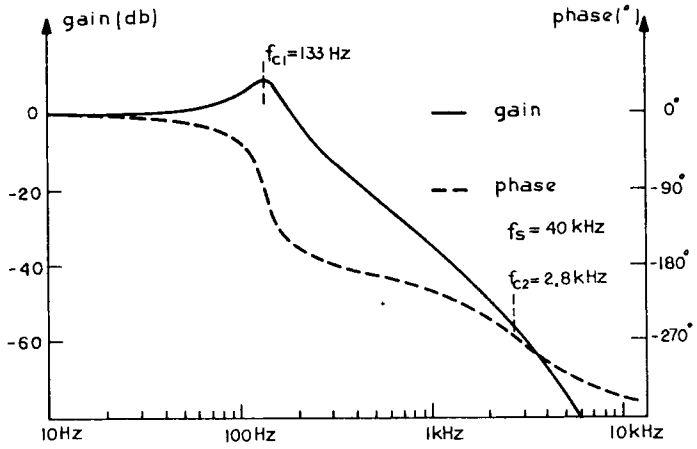

Fig. 25. Theoretical magnitude and phase frequency response of the line transfer function $G_{vg} = \hat{v}_2/\hat{v}_g$ for the new switching converter of Fig. 23.

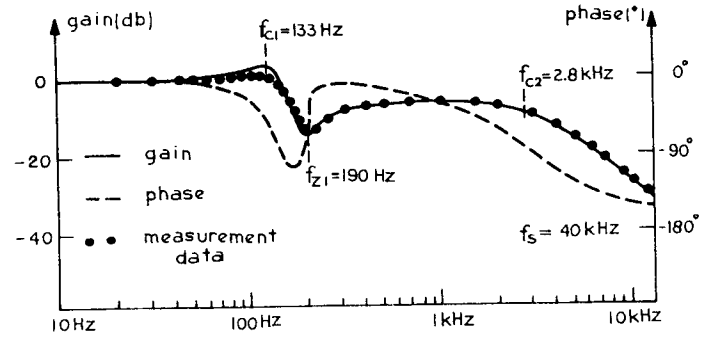

Fig. 26. Theoretical and experimental frequency response of the duty ratio modulation transfer function $G_{vd} = v_2/\hat{d}$ for the new switching converter of Fig. 23.

The same computer program was then used to plot the duty ratio modulation transfer function $G_{vd} = e_1(s)G_{vg}$ as shown in Fig. 26. As seen from the phase plot, the complex zeros are indeed in the *left half-plane* (minimum phase response) as was predicted by the satisfaction of inequality condition (18). In addition, the corner frequency f_{z1}, whose position is accurately predicted by (22), is indeed very close to f_{c1} and causes almost complete cancellation of their effects on both magnitude and phase characteristics. Note, however, that when the parasitic resistance $R_{\ell 1}$ is reduced from 1.0Ω to 0.2Ω, the inequality condition (18) is violated and the complex zeros become *right half-plane* zeros. This fact has also been confirmed on the phase response of G_{vd} by use of the same computer program NEW, but with $R_{\ell 1} = 0.2\Omega$.

Finally, the duty ratio modulation transfer function G_{vd} was measured using the familiar describing function measurements [8], and excellent agreement with the theoretical frequency response is observed (see Fig. 26).

5 COMPARISON OF THE NEW CONVERTER AND CONVENTIONAL BUCK-BOOST CONVERTER

In this Section an extensive theoretical as well as experimental comparison is made between the new converter and the conventional buck-boost converter to which an input filter has been added. This, and the same component element values as well as operating conditions for the two converters, enable a convenient common ground for comparison. The two converters are then compared with respect to the most important performance parameters, namely: switching ripple, efficiency (with separate analysis of transistor switching and dc losses as well as parasitic resistance losses), electromagnetic interference (EMI) problems, complexity of the transistor drive circuitry, effect of the effective series resistances (ESR) of the capacitors, and converter size and weight reductions resulting from potential increase of the switching frequency f_s. At all these comparison points, the new converter is shown to be superior.

After the detailed theoretical and experimental comparisons, the important advantages of the new converter are concisely summarized.

5.1 Experimental test circuits of the two converters

Two experimental test circuits have been built, one employing the new converter topology and the other the conventional buck-boost converter with an input filter as shown in Fig. 27.

The addition of the input L_1, C_1 filter to the conventional buck-boost converter is invariably required to smooth out the input current switching ripple. This then provides a convenient comparison ground for the two converters in Fig. 27. Now both converters have continuous input current in addition to performing the same general dc conversion function with output dc voltage inversion. Moreover, both now consist of the *same components*. They, however, *differ in the way these components are interconnected*. Therefore the effect of two *different converter topologies* upon the performance characteristics can now be extracted.

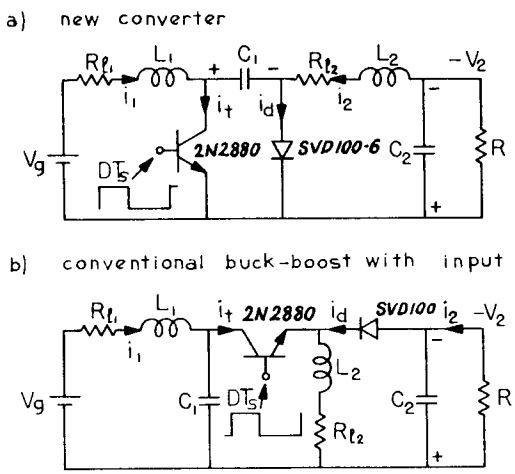

Fig. 27. Two converters used for experimental and theoretical comparison employ the same components but different topologies.

For comparison purposes, the same component element values are used for both converters, and are

$$R_{\ell 1} = 1.0\Omega, \quad L_1 = 3.5\text{mH}, \quad C_1 = 100\mu\text{F}, \quad R = 75\Omega$$

$$R_{\ell 2} = 0.4\Omega, \quad L_2 = 6.5\text{mH}, \quad C_2 = 0.47\mu\text{F} \qquad (23)$$

The same operating conditions are also used:

$$V_g = 5\text{V}, \quad D = 0.6, \quad f_s = 40\text{kHz} \qquad (24)$$

The switching components employed are: transistor 2N2880 and diode TRW SVD100-6. With the two converters now completely defined, we turn to detailed experimental and theoretical comparison.

5.2 Switching ripple comparison

Since the output stage of the new converter in Fig. 27 represents essentially a buck power stage, the output current ripple Δi_2 can be computed as for the buck converter, that is $\Delta i_2 = V_2 D' T_s / L_2$, or for values given in (23) and (24), as $\Delta i_2 = 14.5\text{mA}$. The output voltage ripple Δv_2 is similarly obtained as

$$\Delta v_2 = \frac{V_2 D'}{8 L_2 C_2} \frac{1}{f_s^2} \qquad (25)$$

Numerically, $\Delta v_2 = 95.5\text{mV}$ in close agreement with the actual output voltage ripple shown in Fig. 28a displaying the actual oscilloscope waveforms of the new converter. Again, the new converter has retained the good ripple properties of the buck converter: output voltage ripple is *independent* of the load current, and decreases sharply with increase in switching frequency (as $1/f_s^2$). This is a consequence of the *nonpulsating output current* i_2, also shown in Fig. 28a.

However, the buck-boost converter still has *pulsating output* current i_d (diode current) as shown in Fig. 28b. The immediate consequence is that the output voltage ripple Δv_2 is *load-current dependent* and obtained as

$$\Delta v_2 = D \frac{V_2}{RC_2} \frac{1}{f_s} \qquad (26)$$

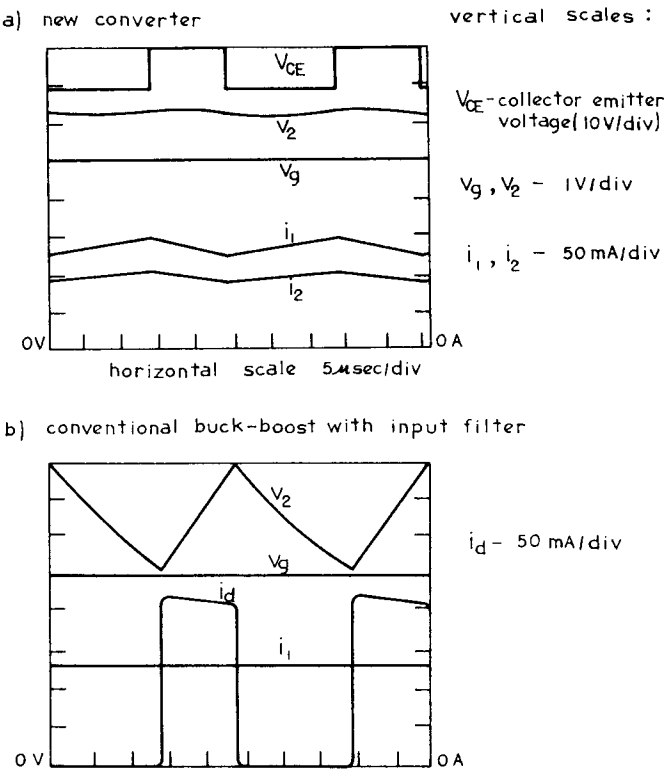

Fig. 28. Comparison of the output voltage and current switching ripple of the two converters of Fig. 27.

For the same element values (23) and (24) as in the new converter, the output voltage ripple from (26) becomes $\Delta v_2 = 3\text{V}$ (here $v_2(0^+) = 7.6\text{V}$ from Fig. 28b is used instead of $V_2 = 6.3\text{V}$ since ripple is large and (26) is strictly applicable only for small ripple). This is quite close to the actual measured ripple of $\Delta v_2 = 2.8\text{V}$ from the output voltage waveform in Fig. 28b.

Therefore, with use of the same element values in both converters, the output voltage ripple was reduced from a totally unacceptable 44% in the conventional buck-boost converter to less than 1.5% in the new converter. Hence a 30:1 ripple reduction has been achieved just by use of the new converter topology. Moreover, this ratio becomes even proportionally much bigger with increased switching frequency f_s, duty ratio D and increased loads ($R < 75\Omega$).

Since the voltage ripple in Fig. 28b is completely unacceptable, one would have to resort to some means of reducing it. As seen in (26) the ripple would be reduced by substantial increase of capacitance C_2, but at the same time size and weight would be proportionally increased. The other possibility, increase of switching frequency f_s, would, because of increased switching losses, degrade further the efficiency of the conventional buck-boost converter in Fig. 27b. Moreover, by increase of switching frequency, the output voltage ripple Δv_2 in the new converter would decrease at a much higher rate, owing to the $1/f_s^2$ dependence in (25) as compared to only $1/f_s$ dependence in (26).

As a conclusion, the new converter (Fig. 27a) outperforms in every respect the conventional buck-boost converter (Fig. 27b) as far as the output switching ripple is concerned.

5.3 Comparison of the transistor and diode dc losses and transistor switching losses for the idealized case ($R_{\ell 1} = R_{\ell 2} = 0$)

A substantial part of the total converter losses is due to the dc losses in the transistor and diode, which come from their nonideal nature. Namely, when the transistor is on, the collector-emitter voltage V_{CE} is *not zero* (as it is for an ideal switch S), but some saturation voltage V_{SAT} on the order of 0.3V-1V. Likewise, the diode has some forward voltage drop V_F of the same order. Since V_{SAT} and V_F increase very little with increase of dc current, the dc losses are approximately proportional to the dc currents. Hence we compare the dc transistor and diode losses of the two converters by comparing their respective dc currents (when they are on, since their dc losses are negligible in the off state). In fact, by assuming V_{SAT} and V_F constant a conservative estimate for the comparison of dc losses will be obtained, since transistor and diode with higher current will have higher V_{SAT} and V_F as well, hence even higher losses.

Let us for the moment assume that the inductors in the two converters of Fig. 27 are ideal ($R_{\ell 1} = R_{\ell 2} = 0$) because we will return to the real case ($R_{\ell 1} \neq R_{\ell 2} \neq 0$) in section 5.5.

At first sight, it seems that the transistor and diode dc losses are higher in the new converter (Fig. 27a), since the *sum* of the input and output currents ($i_1 + i_2$) passes through its transistor when it is on, while in the conventional buck-boost converter (Fig. 27b) only the input current passes through its transistor. Likewise, when the transistor is off, both input and output currents ($i_1 + i_2$) pass through the diode in the new converter, while only the output current passes through the diode in the conventional buck-boost converter. However, this is only *an illusion* as clearly illustrated on the actual oscilloscope waveforms of the four currents i_1, i_2, i_t and i_d shown in Fig. 29 for the new converter, and in Fig. 30 for the conventional buck-boost converter. As a matter of fact the actual comparison of Figs. 29 and 30 shows that the transistor and diode currents *are higher* for the conventional buck-boost converter than for the new converter. This is, however, not a mere coincidence, but a consequence of the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ (which, of course, cannot be excluded from the actual measurements as they can from the analysis) as will be explained in Section 5.5. Let us, now, go back to the ideal case $R_{\ell 1} = R_{\ell 2} = 0$, to clarify this result.

Consider first the conventional buck-boost converter of Fig. 27b. Its transistor current during the interval when the transistor is on must be proportionally higher than the input current i_1 (and its dc value I_1) in order to have the same dc average value I_1 over the whole period T_s (see Fig. 30a). Also, through the action of the inductance L_2, transistor dc current I_t (when it is on) is equal to the diode dc current I_d (when the diode is on) since they are both equal to the dc current of inductance L_2. Hence

$$I_t = I_d = I_1/D = I_2/D' \qquad (27)$$

where I_1 is the dc input current. Note that for the conventional buck-boost converter, I_2 is defined as the *dc load current* (dotted line in Fig. 30b) and *not* as the dc current of inductance L_2, in order to conform with the dc input and output current notation for the new converter.

For the new converter in Fig. 27a, the transistor and diode dc currents I_t and I_d are equal to the *sum* of the input and output dc currents, that is

$$I_t = I_d = I_1 + I_2 \qquad (28)$$

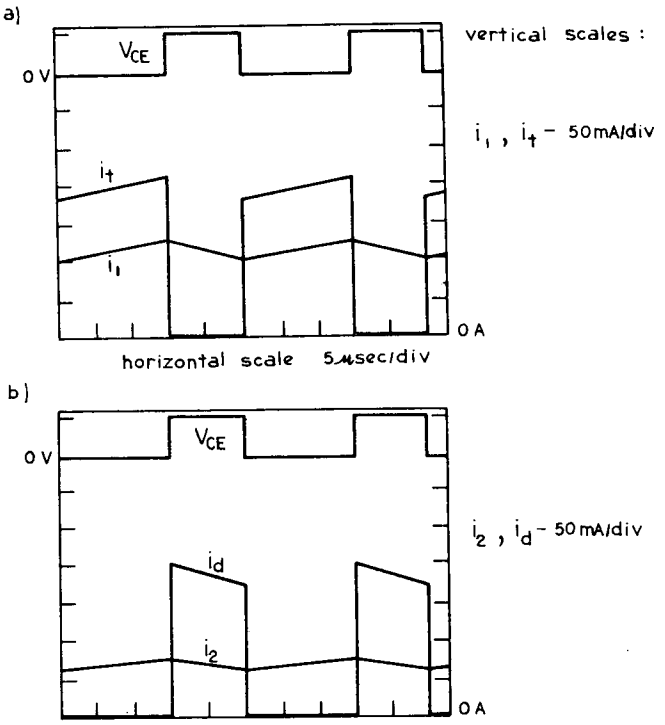

Fig. 29. Comparison of input and output currents with transistor and diode currents for the new converter: a) input current and transistor current; b) output current and diode current

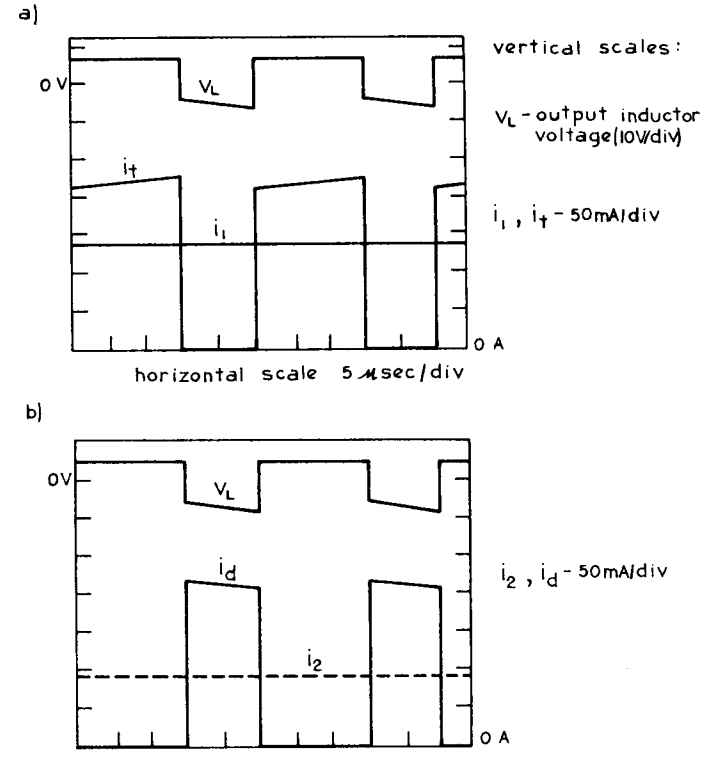

Fig. 30. Comparison of input and output currents with transistor and diode currents for conventional buck-boost converter: a) input current and transistor current; b) output current and diode current

This may be easily seen in Fig. 29, where the *sum* of the input and output currents $i_1 + i_2$ is equal to the transistor current i_t during the on interval (DT_s) and to the diode current i_d during the off interval ($D'T_s$). However, upon substitution of the dc current relations $I_2/I_1 = D'/D$ for this converter in (28), the same result as (27) is obtained. Hence, the dc transistor and diode currents I_t and I_d are the same for both converters in this ideal case ($R_{\ell 1} = R_{\ell 2} = 0$), and consequently their respective *dc losses* are also *equal*.

Since the on currents I_t of the switching transistors are the same for the two converters, so are the corresponding saturation voltages V_{SAT}. From Fig. 27 the collector-emitter voltages of the transistors when they are off (V_{OFF}) are also the same and equal to $V_{OFF} = V_g/D'$. Hence, during switching the transistor operating point traverses the region between the same points (V_{SAT}, I_t) and (V_{OFF}, 0). Therefore the transistor switching losses are also the same for the two converters of Fig. 27 in the ideal case $R_{\ell 1} = R_{\ell 2} = 0$.

5.4 Comparison of the resistive dc losses only

We now make the opposite assumption from the one in the previous section, that is, the transistor and diode are ideal with no dc losses, and instead include the effect of the parasitic resistances only by considering $R_{\ell 1}$, $R_{\ell 2} \neq 0$.

From the canonical circuit models for the two converters (or by solving for the dc conditions using state-space averaging), the efficiency and dc conversion relations are obtained as

new converter:

$$\eta_1 = \frac{R}{R + \left(\frac{D}{D'}\right)^2 R_{\ell 1} + R_{\ell 2}} \; ; \; \left|\frac{V_2}{V_g}\right| = \frac{D}{D'}\eta_1, \quad \frac{I_1}{I_2} = \frac{D}{D'} \qquad (29)$$

conventional buck-boost with input filter:

$$\eta_2 = \frac{R}{R + \left(\frac{D}{D'}\right)^2 R_{\ell 1} + \frac{R_{\ell 2}}{D'^2}} \; ; \; \left|\frac{V_2}{V_g}\right| = \frac{D}{D'}\eta_2, \quad \frac{I_1}{I_2} = \frac{D}{D'} \qquad (30)$$

Comparison of (29) and (30) now reveals that both the dc voltage gain and efficiency are higher in the new converter than in the conventional buck-boost throughout the duty ratio D range because of the difference in terms dependent on $R_{\ell 2}$, the parasitic resistance of inductance L_2.

In order to enhance this difference, the inductances in the experimental models of Fig. 27 have been interchanged such that the inductance with the higher parasitic series resistance is now in the output circuit, or $R_{\ell 1} = 0.4\Omega$ and $R_{\ell 2} = 1.0\Omega$, but $R = 75\Omega$ as before. With these element values and by use of (29) and (30), the dc gain characteristics for the two converters are as shown in Fig. 31, while efficiency is plotted in Fig. 32. As seen in Figs. 31 and 32 both the dc gain and efficiency are substantially higher in the new converter throughout the range of duty ratio D.

Let us now with the help of these graphs illustrate the comparison of the efficiencies between the two converters. Suppose that it is required that the nominal input voltage $V_g = 5V$ is boosted 3 times. This would result in the establishment of the steady-state (dc) duty ratio D = 0.82, or operation at point A in Fig. 31, if the conventional buck-boost converter of Fig. 27b was used. However, the same gain of 3 can be achieved with the new converter by operation at point B, with substantially

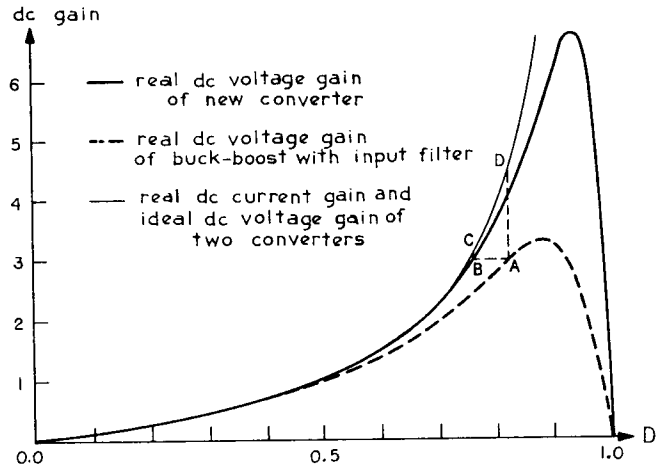

Fig. 31. Steady-state (dc) characteristics for the two converters of Fig. 27.

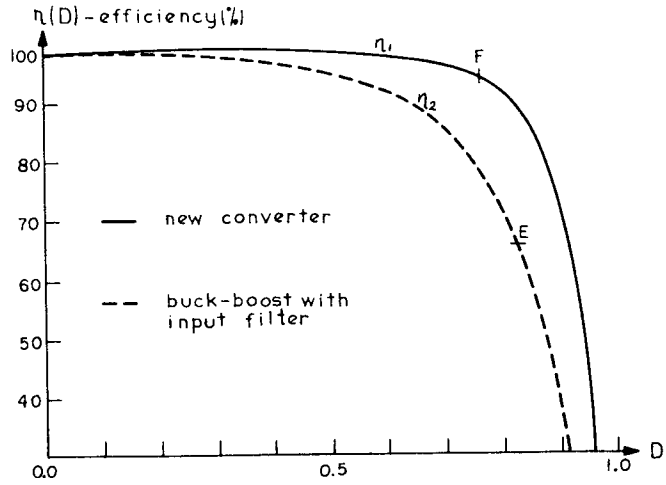

Fig. 32. Efficiency characteristics for the two converters which include effect of parasitic resistances only ($R_{\ell 1} \neq 0$, $R_{\ell 2} \neq 0$).

smaller duty ratio D = 0.76 as seen in Fig. 31. From Fig. 32 we find that operation at point A (D = 0.82) would mean only 65.5% efficiency (point E) while operation at point B would give an excellent 93.5% efficiency (point F). Hence, use of the *same storage element values* (inductors) in the novel circuit topology of the new converter (Fig. 27a) would *boost the efficiency* by 28% over the conventional solution (Fig. 27b). This substantial increase in efficiency is, of course, the result of the *combined* effect of both *higher voltage gain* in the new converter (Fig. 31), which permits operating at lower duty ratios D (hence gain in efficiency already), and also owing to the *higher efficiency* of the new converter in comparison with the conventional buck-boost for the same duty ratio D (Fig. 32). Thus, their *cumulative* effect brings about a much higher overall gain in efficiency as demonstrated in the previous numerical example.

However, it may perhaps seem surprising that the substantial increase in efficiency arose solely from the *single term* difference in the efficiency characteristics for the two converters (compare $R_{\ell 2}$ in (29) with $R_{\ell 2}/D'^2$ in (30)). Let us, therefore, give a qualitative, physical explanation which will emphasize the importance of the *position* of inductor L_2 in the two converters, and throw some light on the effect of the resulting *output current waveforms* upon the converter *efficiency*

As seen in Fig. 30b, in order to pass an average dc current I_2 (shown in dotted lines) to the load of the conventional buck-boost converter, the magnitude of the *pulsating* diode current i_d (when the diode is on) has to be significantly larger than I_2 (since the average of i_d over the whole switching period should result in I_2). However, this sets the dc level of the current $i_{\ell 2}$ through inductor L_2 at a much higher level in the conventional buck-boost than in the new converter, whose *nonpulsating* output current (with dc average value I_2) is also the inductor current $i_{\ell 2}$. This is further demonstrated in Fig. 33 in which the inductor current waveforms $i_{\ell 1}$ and $i_{\ell 2}$ for the two converters are derived by use of Figs. 29 and 30.

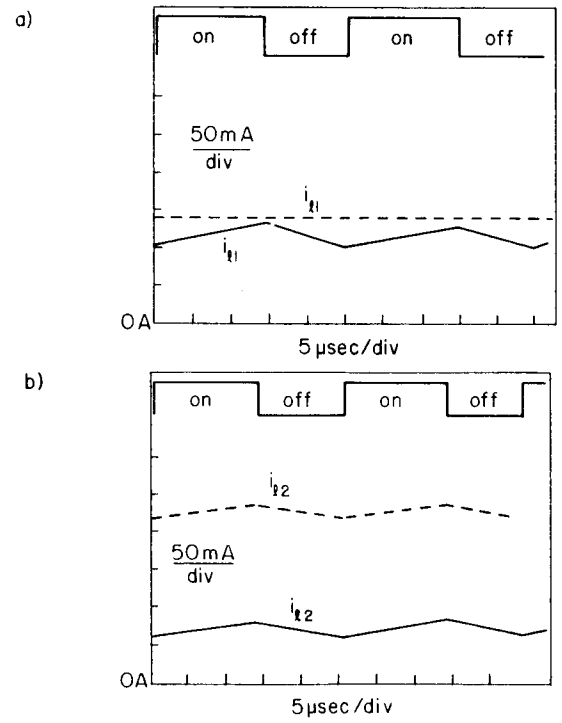

Fig. 33. Comparison of the inductor currents $i_{\ell 1}$ and $i_{\ell 2}$ for the converters in Fig. 27: heavy line - new switching converter (Fig. 27a); dotted line - conventional buck-boost with input filter.

From Fig. 33 it is apparent that the *pulsating output current* (i_d) of the conventional buck-boost converter is the *direct cause* for much higher dc current $I_{\ell 2}$ (dotted lines) through the inductor L_2 than the corresponding current in the new converter (heavy line). For the particular example of Fig. 33b, the dc inductor current $I_{\ell 2}$ is approximately 4 times larger in the conventional buck-boost than in the new converter, which would, of course, result in 16 times larger parasitic losses in the conventional buck-boost converter. Since parasitic resistive losses are an important part of the overall losses, the substantial efficiency degradation demonstrated previously for the conventional buck-boost converter is obtained.

Note that with the increased duty ratio D, this efficiency degradation in the conventional buck-boost converter becomes even more pronounced, since current i_d in Fig. 30b transforms to a narrower pulse with higher magnitude. This qualitative behaviour was quantitatively recorded in Figs. 31 and 32.

This now explains the effect upon the efficiency and gain of the terms dependent on $R_{\ell 2}$ in (29) and (30). From the same expressions one would then expect that the dc losses due to the parasitic resistance $R_{\ell 1}$ are the same. However, as seen in Fig. 33a, the inductor current $i_{\ell 1}$ (dotted line) is slightly larger for the conventional buck-boost converter, owing to its efficiency degradation stemming from parasitic resistance $R_{\ell 2}$.

So far, the significant impact of the *interconnection topology* upon the *overall converter performance* (switching ripple and efficiency) has been established. In particular, the *position* of a single inductance L_2 and *nonpulsating* output current led to these first order improvements. Actually, the estimates obtained are conservative, since some second-order effects still further improve the efficiency of the new converter as demonstrated next.

5.5 Real transistor and diode dc losses and transistor switching losses ($R_{\ell 1}$, $R_{\ell 2} \neq 0$)

We now consider what effect inclusion of the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ has upon the real transistor and diode losses. For the same numerical example as in the previous section, the output dc voltage $V_2 = 15V$ (dc gain of 3) and the output dc current $I_2 = V_2/R = 200mA$ are the same for both converters (operating points A and B in Fig. 31). However, the input dc currents corresponding to these operating points are substantially different, owing to the significant difference in their efficiencies.

For the conventional buck-boost converter we find from Fig. 31 for $D = 0.82$ the dc current gain of $I_1/I_2 = 4.55$ or $I_1 = 910mA$. By use of the expression (27) for the dc transistor and diode current, that is, $I_t = I_d = I_1/D$ we finally obtain $I_t = I_d = 1110mA$.

For the new converter, however, operating at D=0.76 (point C on the dc current gain characteristic in Fig. 31) gives only $I_1/I_2 = 3.15$ or $I_1 = 630mA$. Then, by use of (28) to find the transistor and diode dc losses for this converter we get $I_t = I_d = I_1 + I_2 = 830mA$.

Consequently, when the parasitic resistances $R_{\ell 1}$ and $R_{\ell 2}$ are taken into account the transistor and diode dc currents are not the same but, for the particular example, are about 34% larger in the conventional topology compared to the new converter topology. This now explains very well why the actual measured transistor and diode dc currents for the conventional buck-boost converter (Fig. 30) are higher than those for the new converter (Fig. 29). Hence, in reality ($R_{\ell 1}$, $R_{\ell 2} \neq 0$) the new converter has *lower* transistor and diode dc losses than has the conventional solution.

In addition to the higher dc losses, the switching losses now become higher for the conventional buck-boost converter, since its transistor is operating at a higher (V_{SAT}, I_t) point and traverses, during switching, a region of higher dissipation.

In conclusion, both transistor and diode dc losses and transistor switching losses are substantially higher in the conventional solution, in addition to already higher resistive losses. Hence, for the same element values and output requirements (constant dc voltage) as in the conventional topology, the new converter topology offers unmatched increase in efficiency.

5.6 Comparison of ESR losses of the two capacitances

So far we have considered only the inductors as the nonideal elements, with their corresponding modelling representation which includes their series parasitic resistances. The real capacitors are, likewise, better modelled by inclusion of their effectives series resistance (ESR), which signifies the ac losses present in the real capacitor. Let us, therefore, now find out what consequences its inclusion in the model would have upon the two converters in Fig. 27.

The effect of ESR is particularly pronounced at the output capacitor C_2, so for purpose of numerical comparison we assume that it has ESR = 1Ω. As shown before (Fig. 29) output current ripple (ac) of the new converter is small, at Δi_2 = 14.5mA, hence the capacitance ac losses P_c are $P_c = (\Delta i_2)^2/12$ ESR = 17.5μW = 17.5×10^{-6}W. For the conventional buck-boost, however, the output current is pulsating with Δi_2 = 210mA (Fig. 13.4b), hence the ac losses are P_c = 3.68mW, which amounts to a 210:1 increase in power loss in the conventional solution. This becomes even the *dominant power loss* in the conventional buck-boost at higher load currents. For example when Δi_2 = 10A (much higher load current) losses in the conventional converter becomes P_c = 8.3W, while in the new converter, owing to its ac ripple independence of the load current, they stay the same as before at P_c = 17.5μW. Not only would this still further degrade the efficiency of the conventional solution at higher load currents, but one would have difficulty in finding a capacitor which can dissipate so much power. Moreover, in order to obtain acceptable output voltage ripple, larger capacitances have to be used in the conventional solution and hence ESR problems would be further enhanced. None of these problems is present in the new converter of Fig. 27a.

In order to complete the comparison, one would have to compare the losses in the ESR of the capacitance C_1 in the two converters. However, comparison of the ac current waveforms through their parasitic resistances reveals that they are approximately of the same magnitude owing again to (27) and (28), hence resulting in essentially the same losses.

5.7 Size and weight reduction in the new converter

It has been demonstrated both theoretically and experimentally that the value of the output capacitance C_2 can be very small in the new converter of Fig. 27a (C_2 = 0.47μF) and still achieve reasonably small switching ripple. A small value of output capacitance thus eliminates the need for bulky, electrolytic capacitors of high capacitance value. Moreover, it is very significant that the value of the energy transferring capacitance C_1 does not enter the ripple calculations in (25). Hence it is no surprise that the output voltage ripple remains essentially unaffected (as observed on the scope waveform) even when the capacitance C_1 is reduced 1000 times from C_1 = 100μF, while all other conditions remain unchanged as in (23) and (24). This once again confirms the very significant energy transferring capabilities per unit size and weight of the capacitive storage.

However, the *voltage* across the capacitance C_1 is no longer constant (dc) as for C_1 = 100μF, but has a *triangular waveform* (as observed on the scope) with substantial magnitude. But, according to the duality principle, this is to be compared with the *triangular current* waveform of the energy *transferring inductance* in the conventional buck-boost converter.

In conclusion, for all practical purposes, the physical size and weight of the two capacitors C_1 and C_2 in this new converter (Fig. 27a) can be completely neglected. In addition, the two inductors, which independently control input and output current ripple, can be significantly reduced in size (and weight) by further increase of the switching frequency.

The important advantages of the new converter topology are now concisely summarized.

5.8 Summary of the advantages of the new switching converter

A novel switching dc-to-dc converter (Fig. 11) has been developed which offers higher efficiency, lower output voltage ripple, reduced EMI, smaller size, and yet at the same time achieves the general conversion function: it is capable of both increasing or decreasing the input dc voltage depending on the duty ratio of the switching transistor. This converter employs a *new topology* (Fig. 11) which enables it to have both input and output current nonpulsating. The converter uses *capacitive energy transfer* rather than the inductive energy transfer employed in the other converters. In addition, when it is incorporated into a switching regulator, *stabilization problems are reduced* owing to the favorable frequency response of the new converter (Figs. 25 and 26).

Some of the important advantages of the new converter over the other existing converters are:

1) Provides true general (increase or decrease) dc level conversion of both dc voltage and current.
2) Offers much higher efficiency.
3) Both output voltage and current ripple are much smaller.
4) No dissipation problems in the ESR of the output capacitance.
5) Substantial weight and size reduction due to smaller output filter and smaller energy transferring device (capacitance C_1).
6) Electromagnetic interference (EMI) problems are substantially reduced, thanks to the small ac input current ripple, without need for additional input filters.
7) Excellent dynamic response enables simple compensation in a switching regulator implementation.
8) Much simpler transistor drive circuitry, since the switching transistor is referenced to ground (grounded emitter).

In addition to these advantages, the unique topology of the new switching converter allows some important extensions to be made which are otherwise not achievable in conventional switching converter structures. The additional benefits are:

1) coupling of the inductors [6] in the new converter further substantially reduces both input and output current ripple as well as output switching ripple.

2) implementation of the ideal switch S in Fig. 11 by two VMOS power transistors [6] allows the same converter to achieve a dual function, and to serve as both a positive or a negative regulated voltage supply.

3) insertion of a single transformer in the structure of the new converter [7]results in the highly desirable isolation property, together with multiple inverted or noninverted output capability.

Thus, the new switching dc-to-dc converter is superior to any of the currently known converters in its category, outperforming them in every respect.

6 SWITCHING REGULATOR IMPLEMENTING THE NEW CONVERTER

The recent availability of the complete, signal processing (feedback control) part of the switching regulator in a single integrated circuit (Texas Instruments TL497, Silicon General SG1524 or Motorola MC 3520) makes the closed-loop regulator implementation of the new converter very convenient and further reduces the total size and weight of the regulator.

In Fig. 34 it is shown how this new converter can be incorporated in a closed-loop switching regulator. For a further reduction in size, an integrated circuit incorporating a pulse-width modulator (PWM), feedback amplifier circuitry, power transistor and diode on a single chip (Texas Instruments TL497) is used.

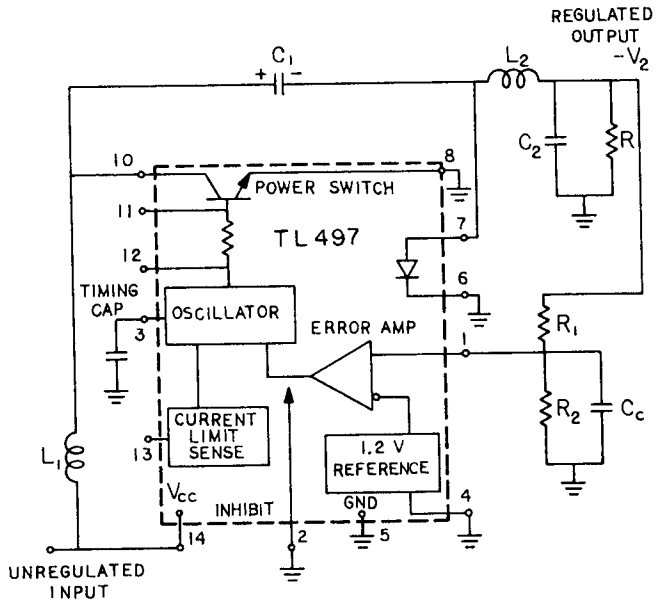

Fig. 34. Closed-loop switching regulator implementing new converter and integrated feedback control circuitry.

The output dc voltage V_2 is determined by

$$V_2 = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$

where V_{REF} is the internal reference voltage of V_{REF} = 1.2V. By use of the modelling technique [2,3,4], the converter canonical circuit model can be obtained and the proper feedback compensation designed with the help of feedback analysis as in [2].

Note also that in the new converter (Fig. 11) several feedback loops become feasible, not only that involving the output voltage as shown in Fig. 34. For example, both inductor currents as well as the capacitance C_1 voltage could be sensed and used to close minor feedback loops. From the converter models in Figs. 21 and 22 these additional transfer functions may be found and proper gains designed into the minor loops to improve the overall converter dynamic performance (transient response, for example).

7 CONCLUSIONS

We now summarize the major results accomplished. First, it has been demonstrated how the topological reduction of the number of switches and the recognition of the duality nature of the storage element networks with switches led to the discovery of the new converter topology (Fig. 11) based upon capacitive rather than inductive energy transfer. The new converter topology in Fig. 11 is independent of any particular hardware realization of the single switch S.

Then, it is shown how a single bipolar transistor and diode can be used in practical implementation of the switching action (Fig. 12), and an in-depth explanation of the physical operation of that circuit is given. A number of advantages of the new converter over other known converters emerge as a consequence of its optimum topology (maximum performance for minimum number of components).

It has also been demonstrated that the new converter topology is the only one previously missing in the complete structure of all buck-boost and boost-buck converters (Fig. 14). In connection with that, an interesting analogy with linear vectors is given in Fig. 15.

Another view of the generation of the new converter, dual to that in Fig. 5, led to the new converter topology by cyclic rotation of the parallel combination of the capacitance and switch S between the input and the output circuit, with buck and boost converters obtained alongside, as shown in Fig. 16. It is suggested that the definition of the buck and boost converters as two distinct basic converters be revised, since they both originate from the same, single topology of Fig. 17a or 18a.

The canonical circuit model for the new converter confirms the general modelling predictions made earlier [3], and the results have been experimentally verified.

In overall performance, the new converter is shown to combine the desirable properties of the buck converter (small output voltage switching ripple and good, stable dynamic frequency response) with the desirable properties of the boost converter (nonpulsating input current, switching transistor referred to ground) without acquiring any of their unfavorable properties.

Finally, the new converter was extensively compared, both theoretically and experimentally, with the conventional buck-boost converter with an input filter. The lower output voltage ripple, substantially higher efficiency, reduced EMI, directly result from the optimum interconnection of components in the new converter topology. Thus, the goal (stated in Section 2) of synthesizing the switching converter with the simplest possible structure and yet maximum performance (nonpulsating input and output currents, highest efficiency) has been achieved in the new switching dc-to-dc converter.

ACKNOWLEDGMENTS

For the generous donation of devices used in the experimental verification, the support of Texas Instruments Inc. and of TRW Semiconductors Inc. is gratefully acknowledged.

REFERENCES

[1] Slobodan Ćuk, "New Dc-to-Dc Switching Converter," Invention disclosure, California Institute of Technology, Pasadena, August 24, 1976.

[2] Slobodan Ćuk, "Modelling, Analysis, and Design of Switching Converters," Ph.D. thesis, California Institute of Technology, November 1976.

[3] R. D. Middlebrook and S. Ćuk, "A General Unified Approach to Modelling Switching-Converter Power Stages," IEEE Power Electronics Specialists Conference, 1976 Record, pp 18-34, (IEEE Publication 76 CHO 1084-3AES). (Also to be published in International Journal of Electronics, London).

[4] R. D. Middlebrook and S. Ćuk, "Modelling and Analysis Methods for Dc-to-Dc Switching Converters," IEEE International Semiconductor Power Converter Conference, 1977 Record, pp 90-111 (IEEE Publication 77 CH 1183-31A).

[5] S. Ćuk and R. D. Middlebrook, "A General Unified Approach to Modelling Switching Dc-to-Dc Converters in Discontinuous Conduction Mode," IEEE Power Electronics Specialists Conference, Palo Alto, June 14-16, 1977.

[6] S. Ćuk and R. D. Middlebrook, "Coupled-Inductor and Other Extensions of a New Optimum Topology Switching Dc-to-Dc Converter," IEEE Industry Applications Society Annual Meeting, Los Angeles, Oct. 2 - 6, 1977.

[7] Slobodan Ćuk and R. D. Middlebrook, "Dc-to-Dc Switching Converter," Patent Application, California Institute of Technology, CIT 1497, June 1977.

[8] R. D. Middlebrook, "Measurement of Loop Gain in Feedback Systems," International Journal of Electronics, 1975, vol. 38, no. 4, pp. 485-512.

[9] H. Matsuo and K. Harada, "The Cascade Connection of Switching Regulators," IEEE Trans. on Industry Applications, vol. IA-3, no. 2, Mar./April 1976

[10] K. Harada and H. Matsuo, "A Method of Surge Reduction in the Switching Regulator," IEEE Power Electronics Specialists Conference, 1976 Record, pp. 303-311, (IEEE Publication 76CH 1084-AES).